Welcome to
7718 semester 1 2022
Mixed Signal Electronic Circuits

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TEL AVIV UNIVERSITY אוניברסיטת תל אביב

7718-grade

Lectures
http://www.gigalogchip.com/lectures.html

# Project suggestions.

**Course Grading:** 70%

| | your target |
|---|---|
| A) 4 bits 2GS/s FLASH ADC | ENOB=3.2bit |
| B) 10 bits 10MS/s SAR ADC | ENOB=9bit |
| C) D) 10gbps CDR | Jitter tolerance "pass" 10khz/10UI |
| D) 10Gbps transmitter with 5cm line | with Z-1 C+1 equalizer 0.1UI ISI |
| E) 10GHZ PLL | Design bw=1MHZ , ckin= 78.125MHz |

- At the university we have a workstation with Cadence and a general 90nm PDK.
- Can use MATLAB/Simulink for the project.
- Can use Cadence Analog-Lib, mixed with its libraries

# Requirements: for A and B Project

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4 deliveries

a) Paper search: review, find at least 4 papers for showing this project: tabulate : Year, Power, FOM, Area, Architecture, type, enob, fs, CLOCK-RATE

( **Delivery 1: List and describe shortly the papers and compose a table to tabulate those parameters ~ 1-2page)**

b) Using Cadence, Excel, Matlab or any software you like : Build your architecture in **high level** . analysis (can be matlab/analoglib sim.) – show that it works (put an input sine Wave show the outputs digital bits (convert them to numbers and plot – DAC them).:

(**Delivery 2 : Build your Architecture, document it, ~ 2-3 pages. Resistors, Capacitors, comparator model, logic gate model**

**Delivery 3: Input a sine wave and show; Time plot input and output, frequency domain plot maximum input and output in frequency domain ) calculate the SNRD,**
(remember for SNR you need to do FFT)

Do only one of the below:

C1) Add to your model at least 1 error (linearity, or thermal noises, jitter) you can skew one resistor.. etc..
Show that it works: SNRD meet project spec
(**Delivery 4: show output and input in frequency domain calculate resulting SNRD )**

**Or:**
C2) Circuit design/analysis: take one block contain transistors (Comparator T&H..all-Logic)
**Delivery4 : Show it in transistor levels.**

# Requirements: for C-D Project

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4 Deliveries

a) Paper search: review, find at least 4 papers for showing this project: tabulate : Power, Area, Architecture type, clock rate

( **Delivery 1: : List and describe shortly the papers and compose a table to tabulate those parameters ~ 1-2page)**

(**Delivery 2 : Build- sketch your Architecture, document it, ~ 2-3 pages. You may use models like inverters VCOs, LPF, etc.**

using CAD: Cadence, Excel, Matlab or any software you like : Build your architecture in **high level** . analysis (can be matlab/analoglib sim.) – show that it works (stable if cdr or pll,or use delivery 3 )

**Delivery 3: Input a random data or clock; show the output/s (data recovered, clock) SHOW EYE DIAGRAMS and time for data few bits.**

Next:
Circuit design/analysis: take one block contain transistors (filip flops, Comparators, vco, phase detector ,charge pump, tx driver-inv+resistors )

**Delivery4 : Show it in transistor levels explain how it works.**

# Basic parameters to choose for skew project



Take a generic sub micron CMOS if you have one if not make your own

For mismatch you can use 1 or more of those numbers

As in lect take capacitor mismatch as for 10 ff 0.8% (C=1.5ff for 1um x1um)

As in lec: Resistor mismatch for 1um x 1um use 1 sigma 2% (400 ohm/square)

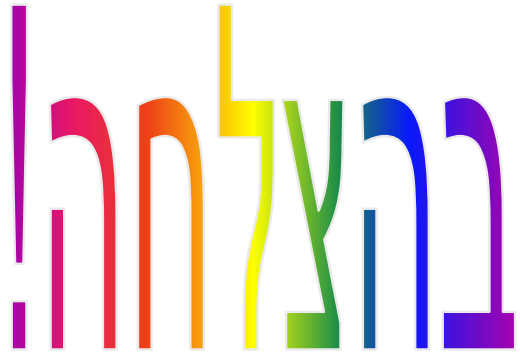
Offset: For transistor use for 1-sigma =4mv for w x l = 1u x 1u

Noise: For transistor noise use 2.7nv/sqrtz for every gm=1e-3

For jitter use 1% of the clock period as jitter

All resistors and capacitors range +/- 15% in absolute value

For project CDR use 512 random date skew the frequency 50000ppm


בהצלחה!