Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

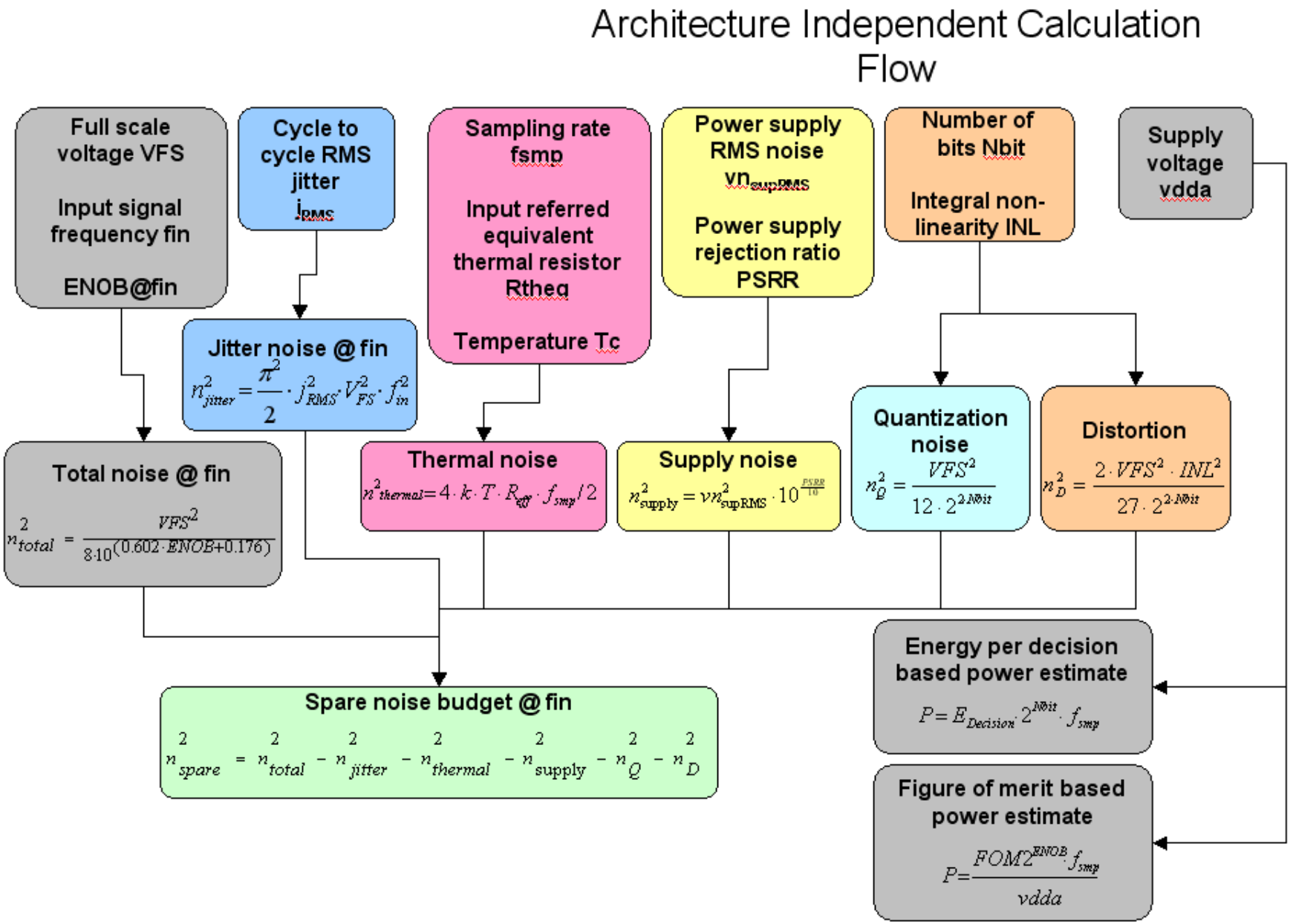
Instructor: Dr. M. Moyal

Lecture 5 (part b)

FLASH ADC Design with error sources.

www.gigalogchip.com

“Error list”


Architecture Independent Calculation Flow
Full scale voltage VFS
Input signal frequency fin
ENOB@fin
Cycle to cycle RMS jitter j_{RMS}
Sampling rate fsmp
Input referred equivalent thermal resistor Rtheq
Temperature Tc
Power supply RMS noise vn_{supRMS}
Power supply rejection ratio PSRR
Number of bits Nbit
Integral non-linearity INL
Supply voltage vdda
Jitter noise @ fin
$n^2_{jitter} = \frac{\pi^2}{2} \cdot j^2_{RMS} \cdot V^2_{FS} \cdot f^2_{in}$
Total noise @ fin
$n^2_{total} = \frac{VFS^2}{8 \cdot 10^{(0.602 \cdot ENOB + 0.176)}}$
Thermal noise
$n^2_{thermal} = 4 \cdot k \cdot T \cdot R_{eq} \cdot f_{smp} / 2$
Supply noise
$n^2_{supply} = vn^2_{supRMS} \cdot 10^{\frac{PSRR}{10}}$
Quantization noise
$n^2_Q = \frac{VFS^2}{12 \cdot 2^{2 \cdot Nbit}}$
Distortion
$n^2_D = \frac{2 \cdot VFS^2 \cdot INL^2}{27 \cdot 2^{2 \cdot Nbit}}$
Spare noise budget @ fin
$n^2_{spare} = n^2_{total} - n^2_{jitter} - n^2_{thermal} - n^2_{supply} - n^2_Q - n^2_D$
Energy per decision based power estimate
$P = E_{Decision} \cdot 2^{Nbit} \cdot f_{smp}$
Figure of merit based power estimate
$P = \frac{FOM2^{ENOB} \cdot f_{smp}}{vdda}$

Agenda- you will get familiar with

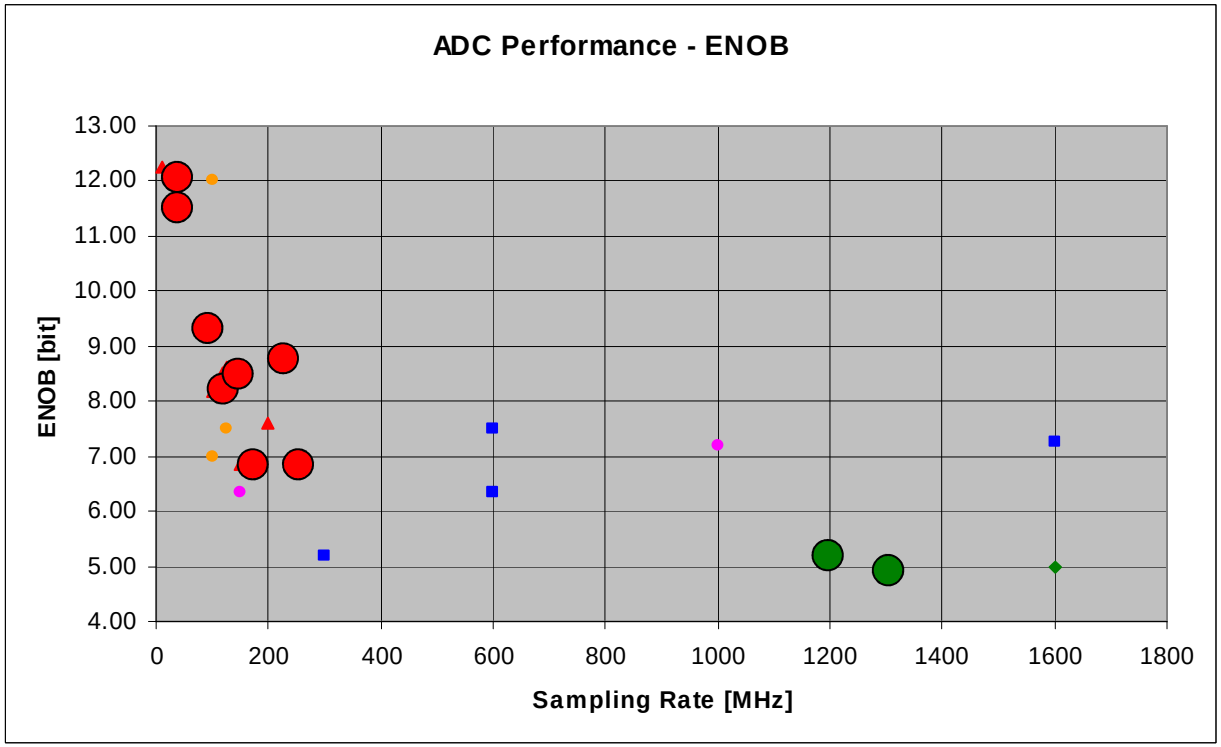
Flash ADC – Design and Error Sources

The ENOB: General trends

ENOB= (SNDR – 1.76) / 6.02

SNRD (AC) Measured Converter S/N
N quantization D Distortions

Green – Flash
Red - Pipe line
Blue Folding
Pink Open Loop Pipe line
Sigma delta ADC ?
(0-200MHz, 9-14bit)



Detail look each element in the FLASH

Comparator Offset
Resistor mismatches
Power
Speed limit first stage
Signal Feed through
Gain
Dynamic Range – Max Vref
Comparator Meta stability (and speed)
Following stages – (bubbles)
Clock distribution

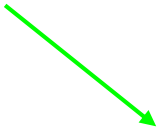
FLASH DESIGN EXAMPLE

A good way to see the errors lets go over flash design

An 8 bits Flash ADC

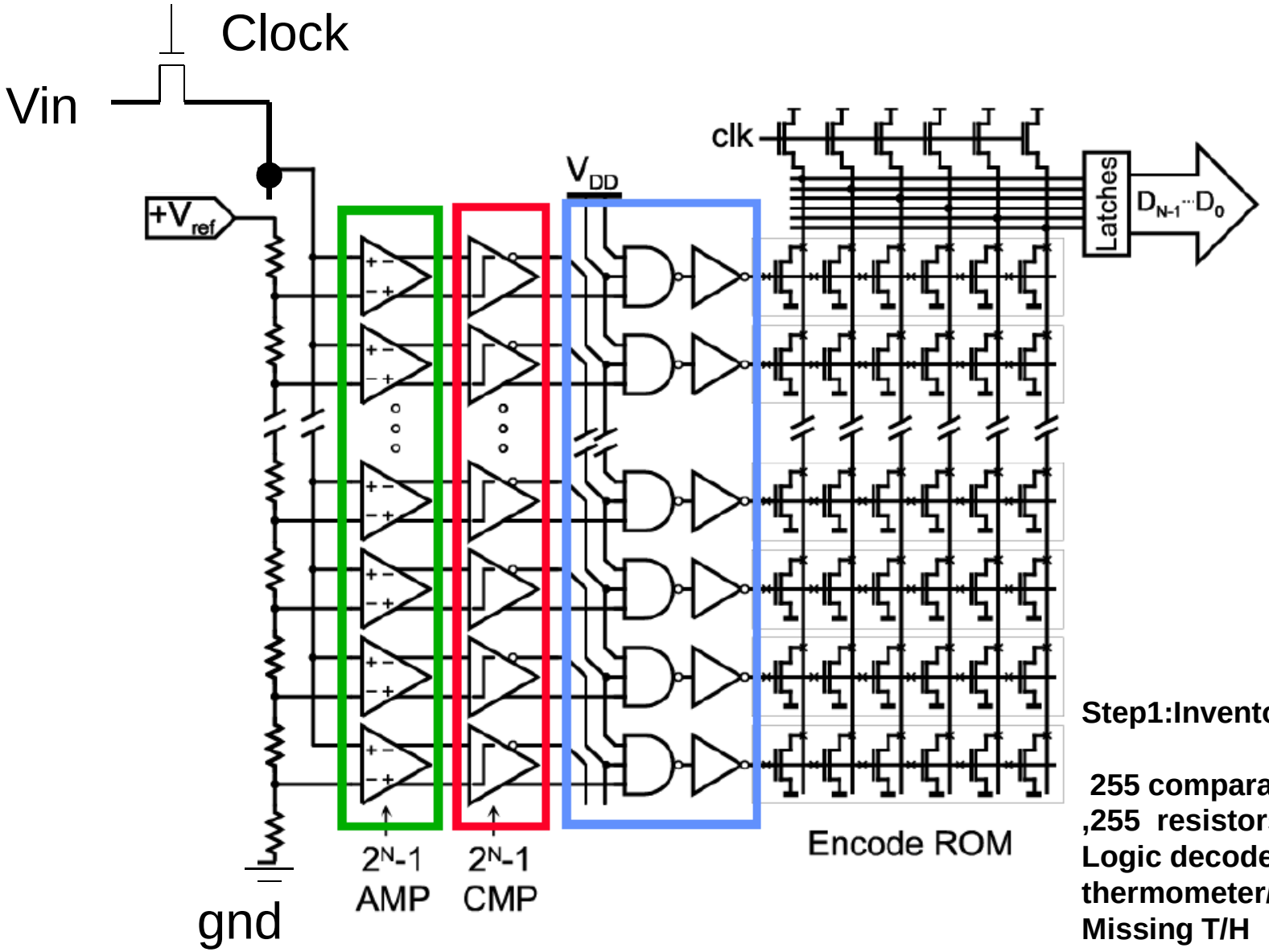
Assuming:

Process 0.18um, Cox~6ff/uu, Kn= 60e-6 Kp=20e-6



Kn =μ***Cox***

Architecture – now to the details.. (from lect. 4)



Source : K.. Leuven

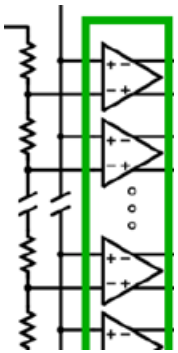
Step1:Inventory:

255 comparators/amp
,255 resistors
Logic decoder
thermometer/binary
Missing T/H
References

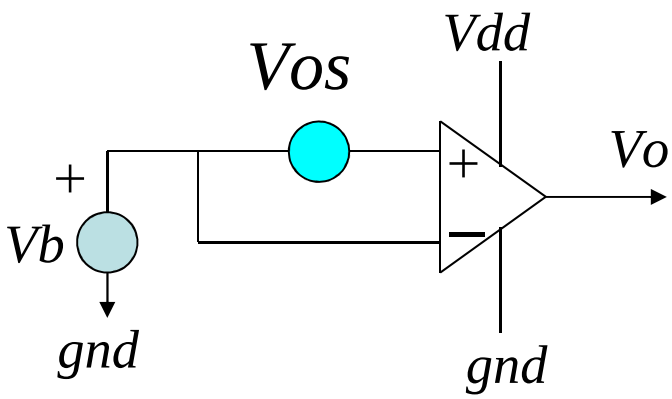
Step 2: Design the converter: (w/l) with correct accuracy:

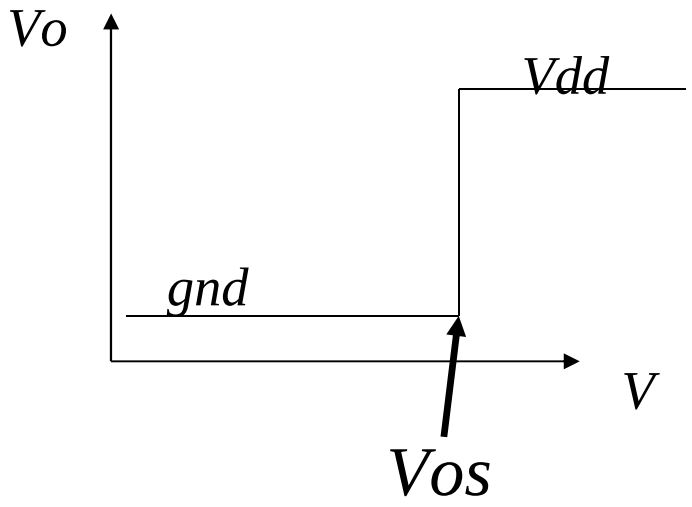
Find/look for:

Accuracy: where in the design non linearties is created
1) Comparator offsets – random mechanism
2) Resistor ladder – random

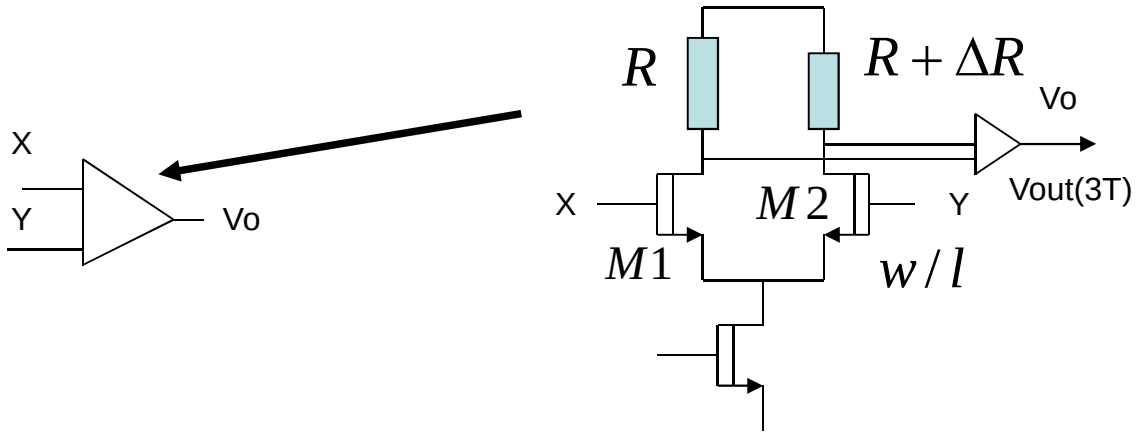


Design example- Comparator Offset find w/l of comparator





Offset- at what voltage (X-Y) the comparator switch



$$Vos1 = \Delta R / R \bullet (I / gm)$$

$$Vos1 = C1 / \sqrt{Weff * Leff}$$

$$=$$

$$M2 \neq M1$$

Comparator Offset

Given process 180nm is C1

$$C1 = 5(mV \bullet \mu)$$

And we use the equation from lect4-5.

$$\sigma(\Delta Vt) = C1/\sqrt{Weff * Leff}$$

But now we need 3 sigma's – so "no" error is created - yield

$$Vos \leq 3 \bullet \sigma(\Delta Vt)$$

Remember:
Could be the biggest problem: bad for low voltage technologies

8bit-Comparator Offset calculations cont.

$$Vos(\max) = 1/2 \bullet LSB$$

$$Vos = 3 \bullet C1/\sqrt{Weff * Leff}$$

½ of 3.9206 = 3 C1/..

$$VFs = 1V \qquad Vlsb = 1/256 = 3.9206mV$$

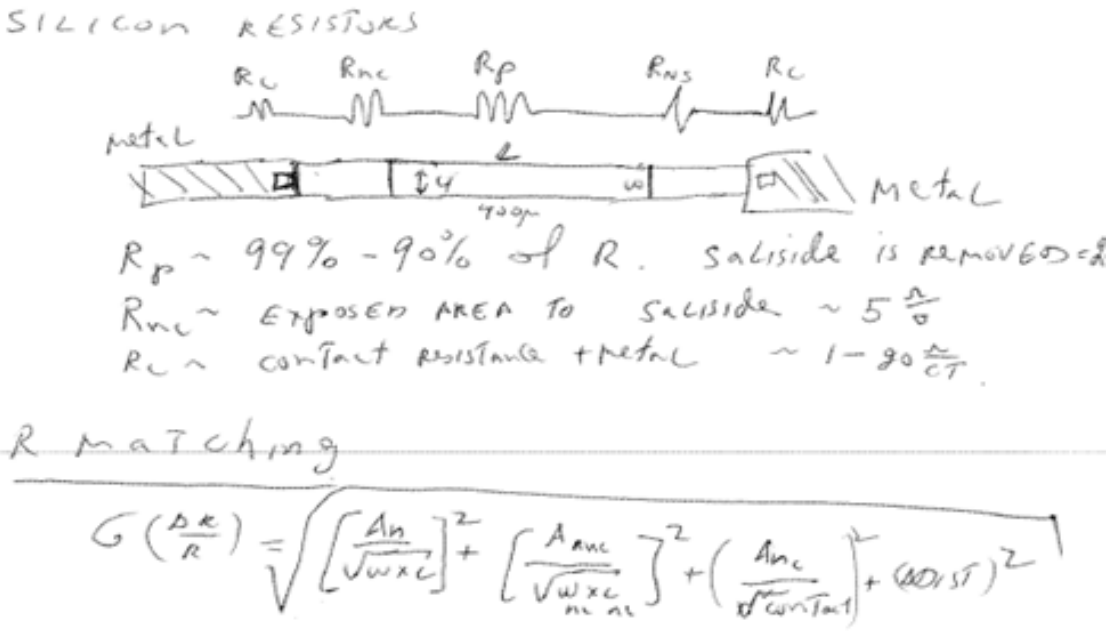
$$C1 = 5(mV \bullet \mu)$$ Process given

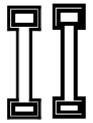
$$\sqrt{Weff * Leff} = 5mv/(1/2(Vfs/256) = 3 \bullet (10mv/3.9206mv)$$

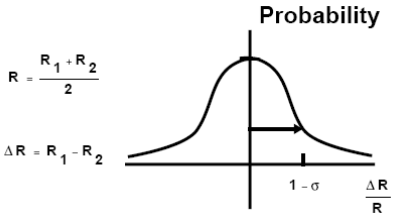
$$Weff \bullet Leff = 58.98$$

Implies L=0.18um W=327um

LADDER MISMATCHES- length determinations







R matching

$$G\left(\frac{\Delta R}{R}\right) = \sqrt{\left[\frac{A_n}{\sqrt{W \times L}}\right]^2 + \left[\frac{A_{RNC}}{\sqrt{W \times L}_{RNC}}\right]^2 + \left(\frac{A_{RC}}{\sqrt{\text{contact}}}\right)^2 + (\text{GRADIST})^2}$$

Need ½ lsb=0.196%

1) Example: Ignore all but poly resistance (see next slide), and
2)If Del-r/r=2% (1um x1um)-process given
3)Take 3 sigma's = 1u x 1u ➔6%. Ratio is 1/30.6 (6/0.196)..

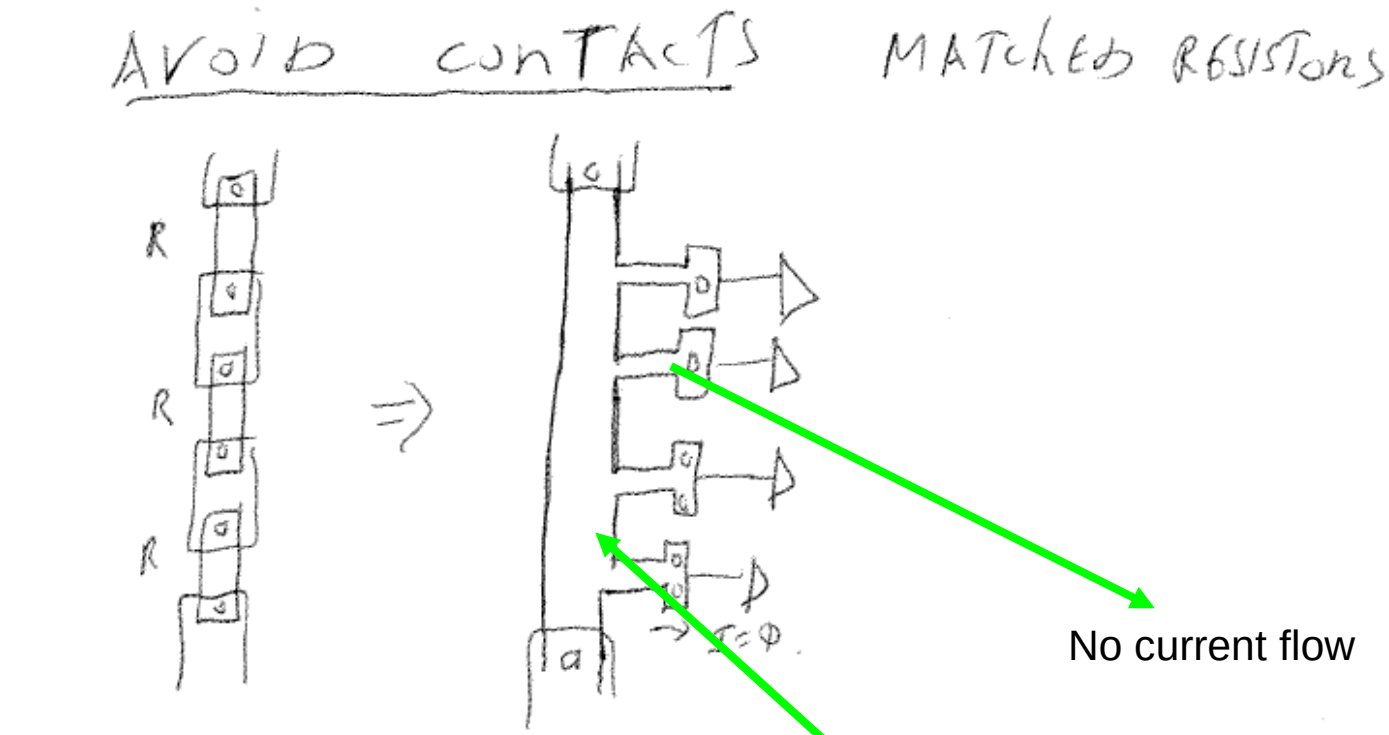
R length =937um

$$\Delta R < \frac{R}{2^{n-1}}\ 0.5$$ Need DelR/R of½ lsb=0.196% 100/510

0.06/((sqrt(Area))=0.00196-→Area=937uu→use 1x937um

Generally: matching possible up to 10-11bit

Get rid of Contact errors



Step 3. power dissipation

POWER- estimate

Power (due to comparators I_{in})

$$P = V_{DD} \times I_{comp} = V_{DD} \times 2 \times k \frac{W}{2L}(V_{GS} - V_T)^2 \cdot [2^n - 1]$$

For Kn=60e-6, l=0.18u w=327un, and if Vgs-Vt=0.1

Ids =μCox(W/2L)(Vgs-Vth) x (Vgs-Vth) x (255)= 541uA x 255 = ~138mA

*P= Without T/H, logic, clock, resistor ladder we re at **248mW***

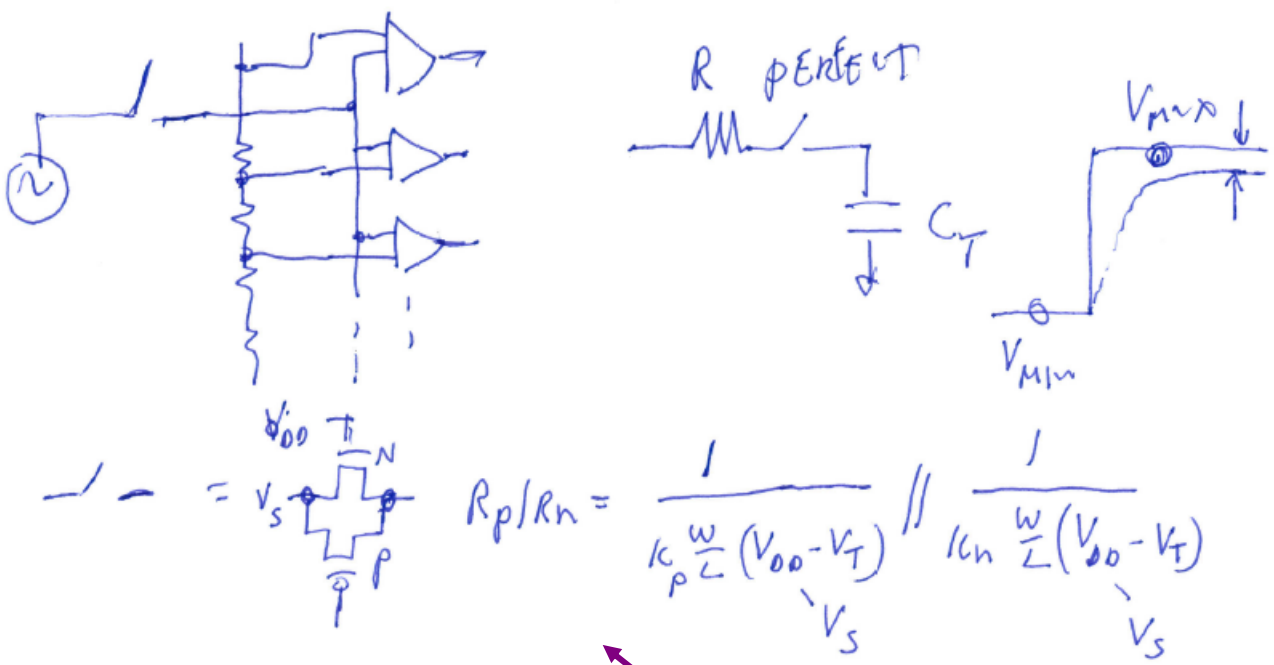
assuming
Remember <78mV
we are not in sat.

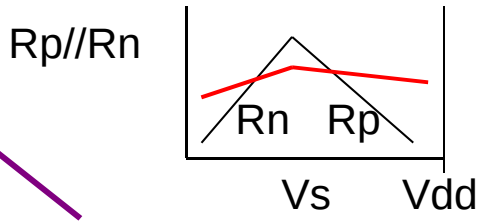
- *Should we increase L ? (keep wxl , drop Power ?)*
- *Should we check real speed to get I*
- *Should we calibrate offset and not increase w/l ?*

Stop and re think:
Isn't power based on I ,
shouldn't we look at speed first ? For min I

Step 4. Meet speed limits

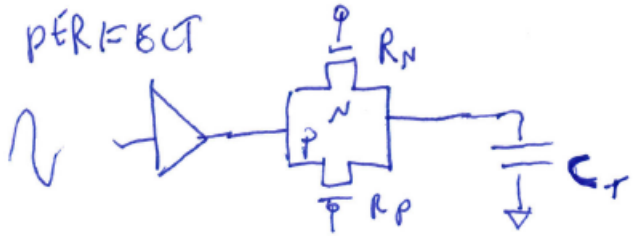
Speed limit due to front stage.- Model





Cin is so large that Rin is important

Speed limit due to front stage.- Acquisition time



$R = R_P // R_N$

$C = C_T$ (ADC)

Vo(t) Vfs

1) $V_{in} = V_o\left(1 - e^{-t/RC}\right)$ (C_T)

2) $V_{in} + \frac{\Delta}{2} = V_o$

3) $\Delta = \frac{V_o}{2^n - 1}$ → Get $\frac{V_{in}}{V_o} = 1 - \frac{1}{2(2^n - 1)}$

Plug into 1. $1 - \frac{1}{(2^n - 1)}\frac{1}{2} = 1 - e^{t/RC}$

IF $\frac{1}{2^n - 1} \simeq \frac{1}{2^n} \Rightarrow t = RC \cdot \ln 2 \cdot (n+1)$

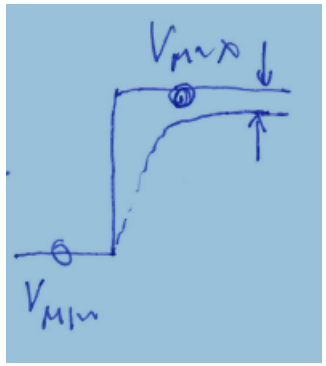
$$t = 0.693\,RC\,(n+1)$$

OR

8bits $\Rightarrow RC \ln[255 \cdot 2]$

need 6.23 RC's.

n	# of RC's
4b	3.46 RC
8b	6.23 RC
10b	7.62 RC



Speed limit due to front stage- Calculation

$C_{ox} = 6\ fF/\mu m^2$, Take $R = 50\Omega$ (example)

From offset calculations W/L=325/0.18 (did not use 327)

$C_T = \frac{2}{3} C_{ox} \cdot 255 + C_{Routing}$ (assure all sat optimistic)

$C_T = 6\ fF \times 325 \times 0.18 \times 255 \times$

$C_T \doteq 59.7\ pF$

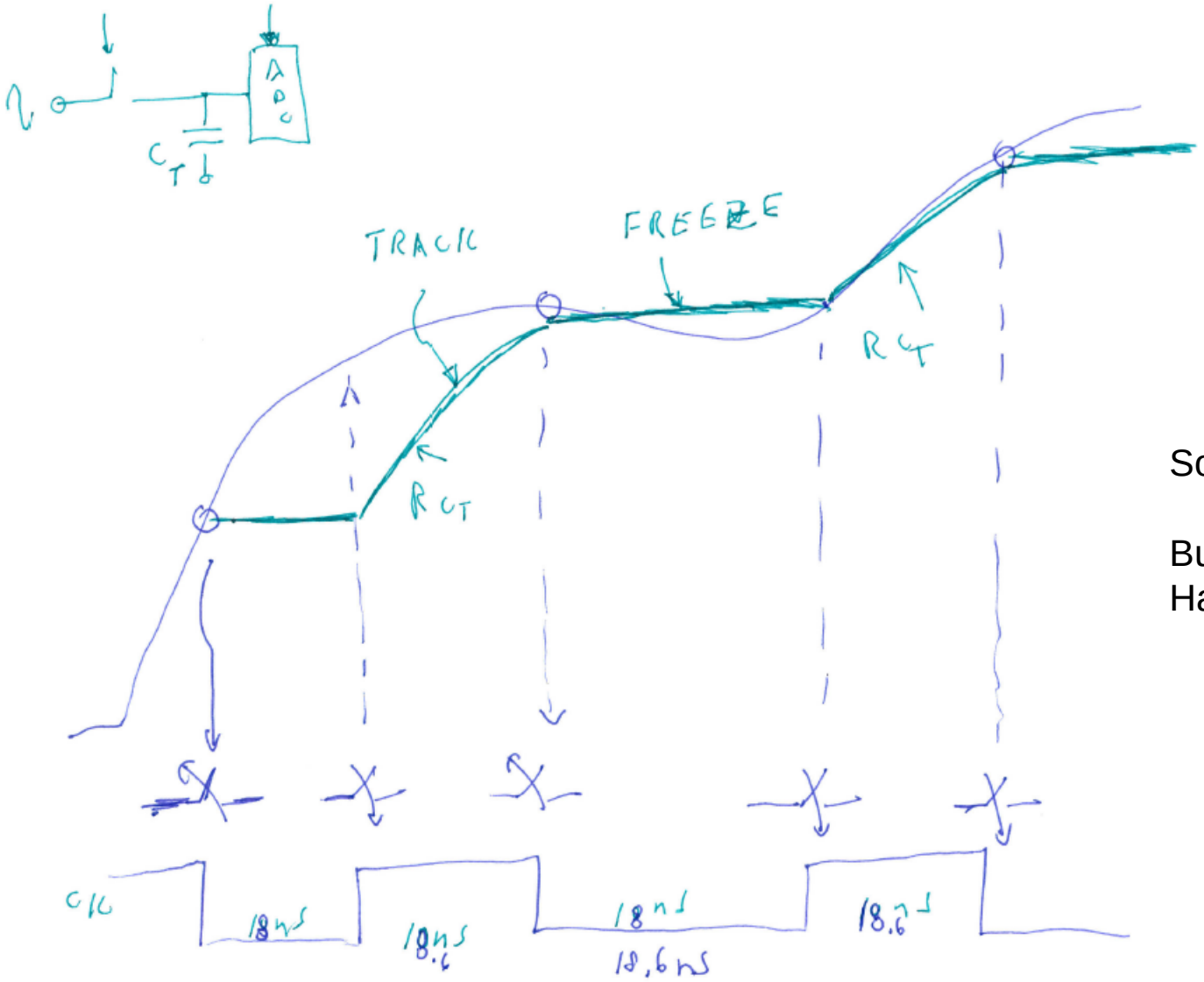
$t\ (8b.T) = 6.23RC = 18.6\ ns$

$\approx 53.7\ MHz$

Disappointing low frequency

Stop and re think:
New buffer to drive low cap ?
Re look at matching – calibrate to reduce Ct ?

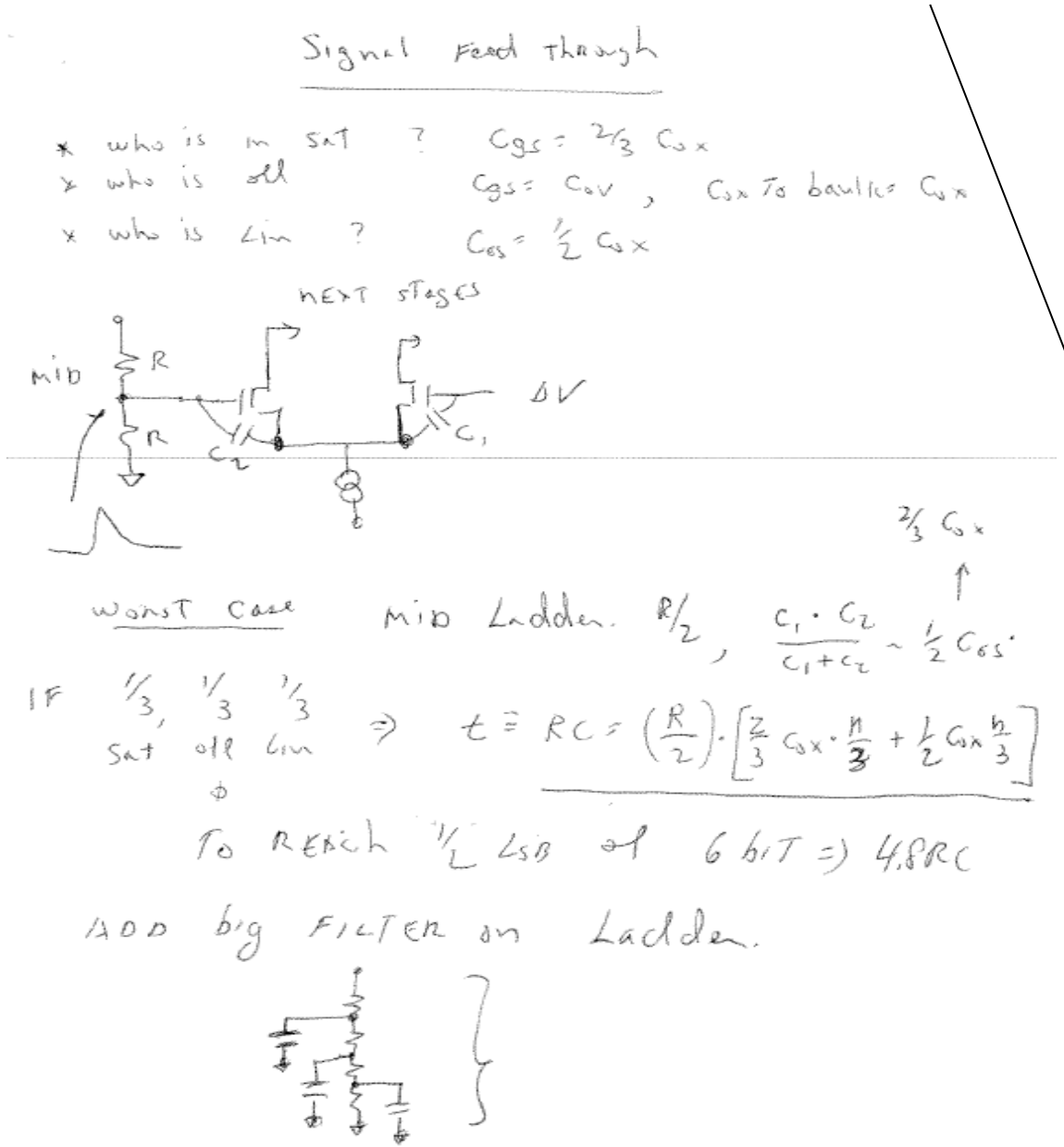
Speed limit due to front stage.- view



So 53.7MHz is too fast

But when is the full scale Happen ?

Speed limit: Feed through speed



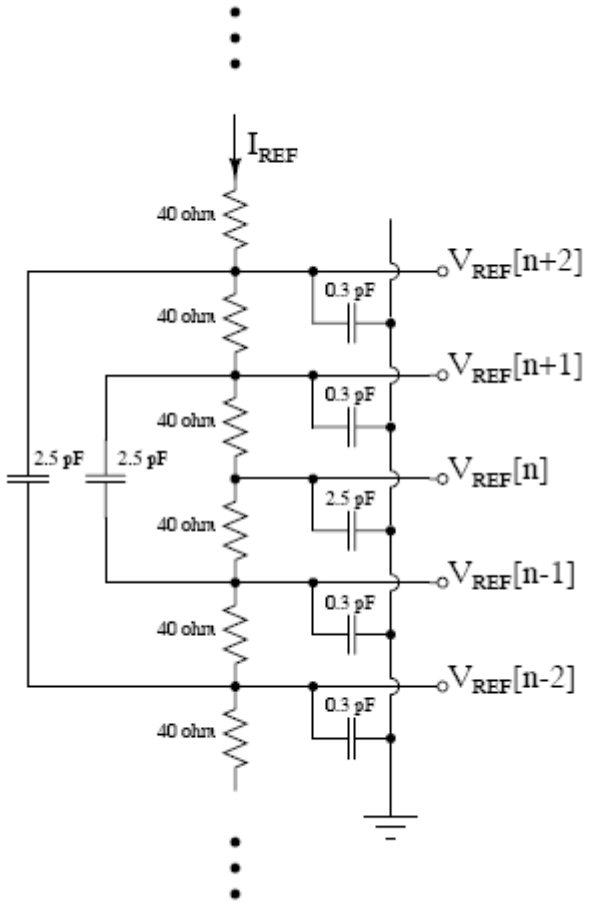
$$\frac{V_{mid}}{V_{in}} = \frac{\pi}{4} \cdot f_{in} \cdot R_{ladder} \cdot C$$

Source : Esscirc 2002. Leuven

C total capacitance
Find max input ladder R.
for no effect
on feed through

(After matching calculations are satisified).

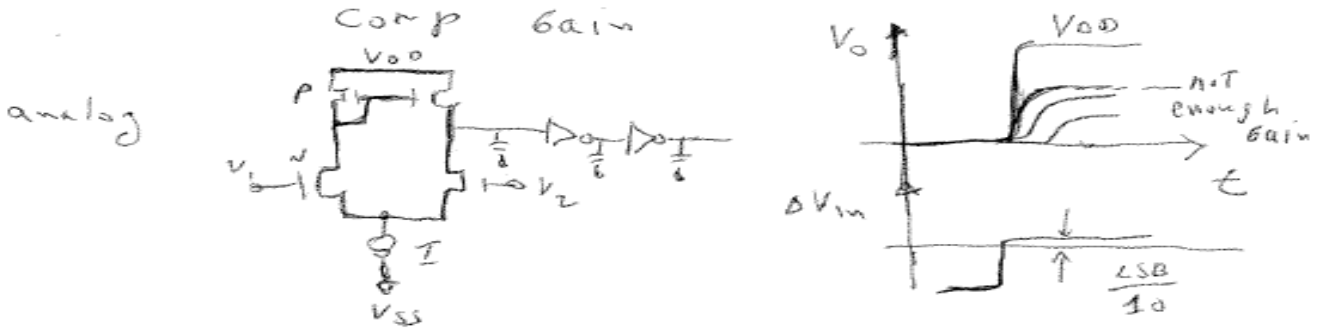
Example removed feed through effect.



Example: Cap stabilization 5b 1GS.s flash
Source: Esscirc 2006 Helsinki univ, Olli Viitala

Step 5. Spec the needed comparator

Comparator Gain- more in comparator design



need enough Gain

① $\Delta V = V_1 - V_2 = \frac{1}{10} LSB$

$V_{DD} \simeq 1.8V$, n bit.

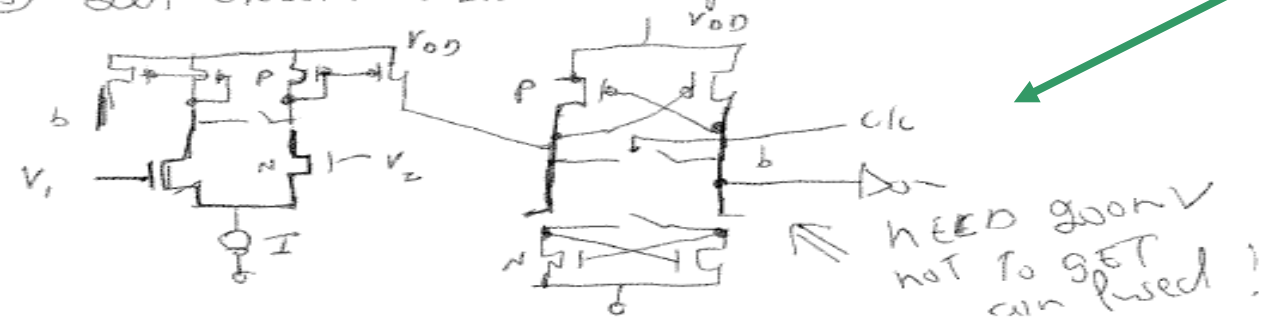
$$A_{o1} = \frac{1.8V}{\frac{V_{FS}}{2^n}} \cdot 10 = \frac{18}{\frac{0.5}{2^8}} = 18 \cdot 2^9 = 9216 \simeq 79\,dB$$

8 bit

one on 2 stages not enough

② & speed ?

③ Let create a Latch on positive Gain

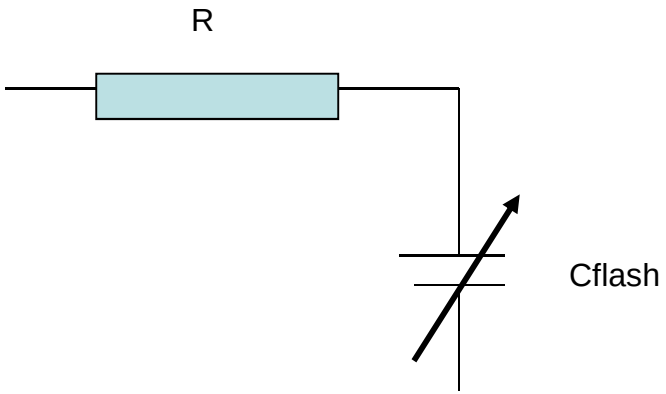


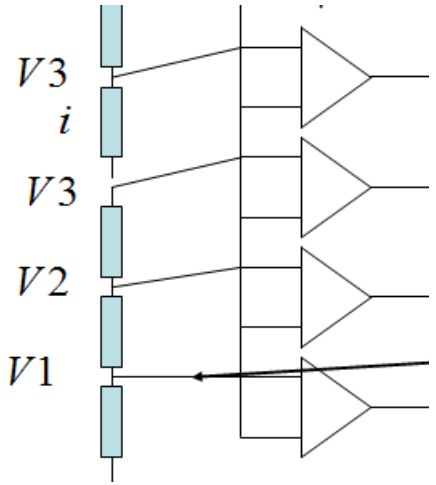
More details in comparator design

capacitors	Saturation	Linear	Off
C gate to S	2/3Cox+Cov	1/2Cox+Cov	Cov
C gate to D	Cov	1/2Cox+Cov	Cov
C gate to B	0	0	Cox//Ccb+..

$$HD_2 = \frac{V_O \omega C_1 R}{2\sqrt{1 + (2\omega C_0 R)^2}}$$

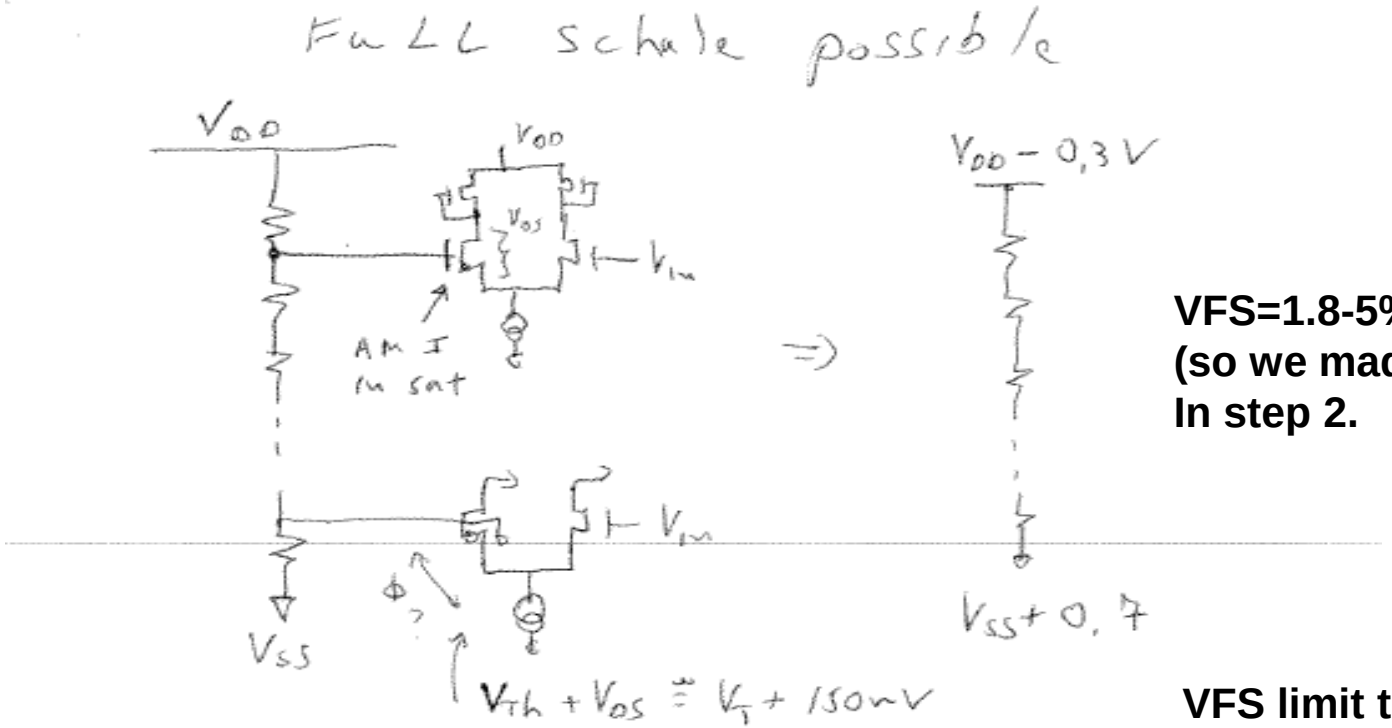
Source : Esscirc 2002 Leuven





Step 6. Set the maximum dynamic range

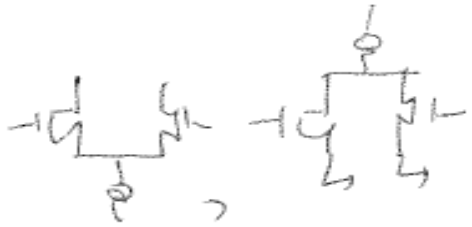
Dynamic Range – Max Vref



VFS=1.8-5%-0.7-0.3=0.71V
(so we made error assuming 1v)
In step 2.

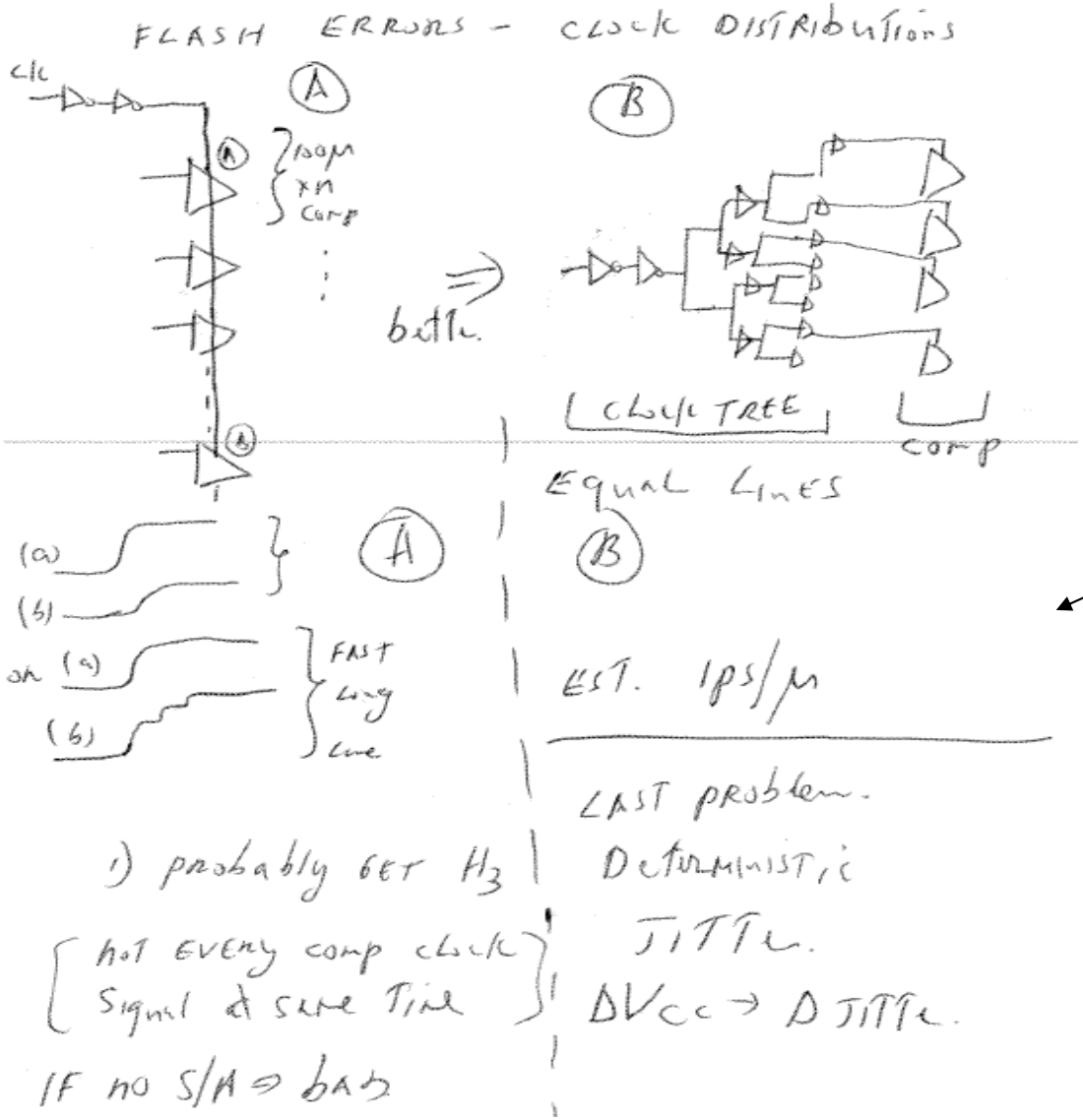
VFS limit the ladder full scale
Limit the SNRD→ VLsb.
Need to be maximized most times

- Limit the Ladder Full Scale
- Limit the SNR
- OR ? & comp type ?



Step 7. Clock- jitter requirement set requirements

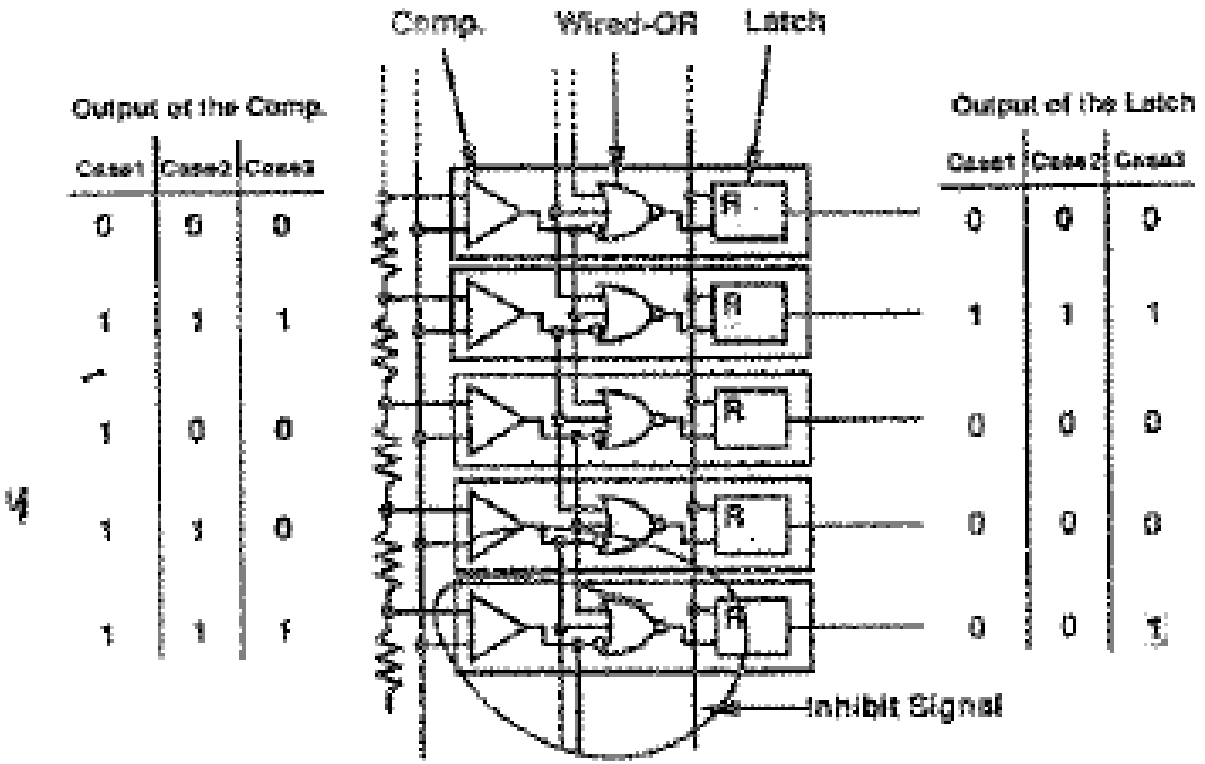
FLASH CLOCK DISTRIBUTION ERRORS



Td=2pi(sgrt(LC)
~2ps/100um

Step 8. Digital design – can we help the analog ? What can we do there..

Error Correction



Bubble error look at your neighbour
Won't correct two errors

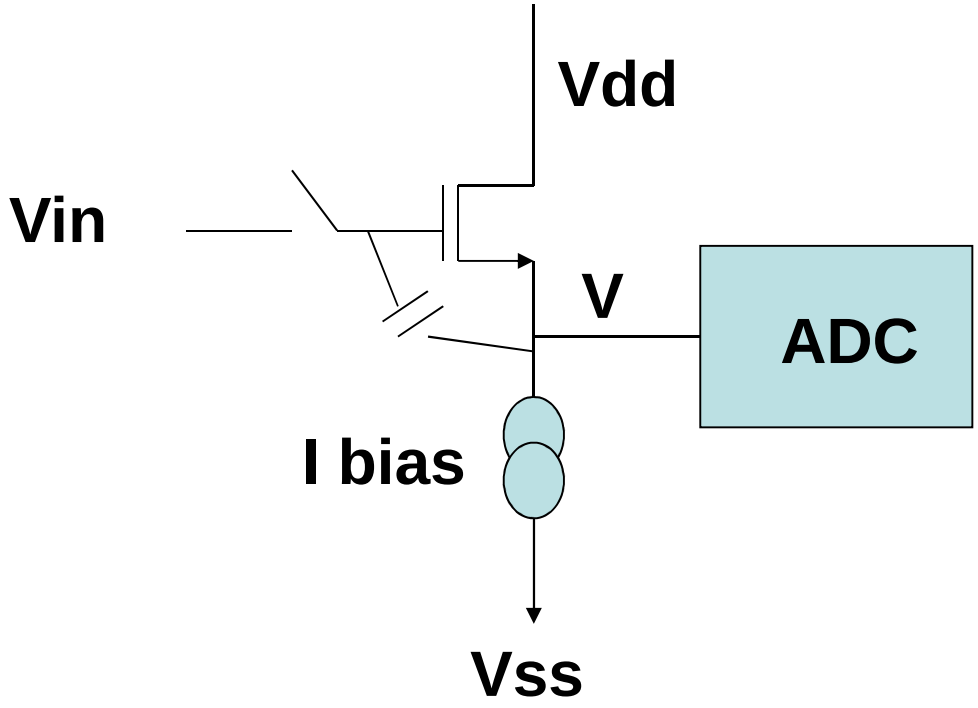
Design check- are we ok ?

Since nothing worked well ..
(FOM = 17 is high→ 10to12 x 248mw / (57e6X255)

How about other architectures..

Assignment

Why does this circuit reduces capacitance of T/H and help drive the large capacitance of the ADC ?



End lecture 05b