Welcome to

0510.7720.01 Winter semester 2021

Mixed Signal Electronic Circuits

Instructor: Dr. Miki Moyal

Lecture 01

1. Course Overview and Requirements

2. Review of CMOS Transistors Basics

What will you get out of this course

1. Mixed Signal design – almost all emphasis on Conversion from Digital to Analog and Analog to Digital domains

2. Basic to detail of Analog circuit (transistor level) design of selected Analog blocks

Understanding of problem flavors and solution/s to mixed signal design

Course lectures: weight=2

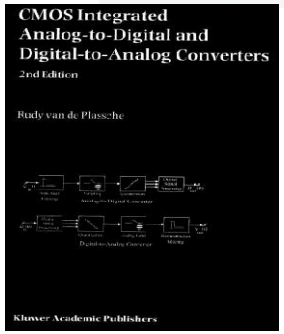
Lecture 1: Overview - Analog transistors basics

<u>Mixed Signal QUANTIZERS/Circuit design of selected blocks</u>

Lecture 2: ADCs- Basic Theory and Definitions, Jitter
Lecture 3: Mismatches and noises in Mixed signal IC** circuits**.
Lecture 4: DAC Architectures
Lecture 5: Over sampling Techniques in DACs
Lecture 6: ADC- Flash Architectures
Lecture 7: SAR ADC and Circuit Design of Comparator for ADCs
Lecture 8: High Speed: Pipe lines
Lecture 9: Circuit Design of Sample and Hold
Lecture 10: Over Sampling ADCs : Sigma Delta - Loops and Architectures
Lecture 11: Sigma delta Switch capacitors ADCs
Lecture 12: Sigma delta design examples
Lecture 13: Advance topics: Time interleaved architecture

Course Overview

Perquisite:
Knowledge in Linear Circuits design and Feedbacks systems.



Book Listing: The link below lists the recommended textbooks for your course in the upcoming academic year.

1) CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters by Rudy van de Plassche, 2nd Edition 2003 Kluwer Academic Publishers

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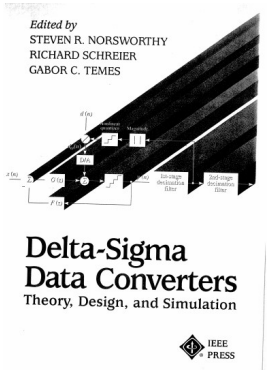
2) Oversampling Delta-Sigma Data Converters Theory Design and Simulations. James C. Candy and Gabor C. Temes, 1992 IEEE press Order num. PC0274-1

Book Listing - Option

Design of Analog Integrated Circuits and Systems, Kenner R. Laker and Willy M.C. Sansen, 1994 McGraw-Hill Series in Electrical and Computer Engineering

Recommended Supplemental Material:

IEEE Journal of Solid State Circuits and ISSCC from 1990-2020, and Lecture's notes.



Grading

Course Grading:

Project:	40%
Homework	60 % - 3-4 questions..

Class Hours:

Wed. 18:00 – 20:00 10 min break/hr.

Lectures are placed in my site:
http://www.gigalogchip.com/lectures.html
My whatsapp 0547885707
Email: miki@gigalogchip.com

Requirements: Project- design in mixes signal arena

I will choose 2 to 3 projects ideas for you to work on.
You may under special case bring your idea but it will need to be approved by me.

Area Topics Area Suggestions:
ADC (sigma delta, Flash, SAR others)

Delivery :
Project:

I will Define spec:
Bits/frequency/Process/voltage range/Power

You will do:
a) Paper Search: What exists lately – at least 3 paper listing.
b) Architecture Analysis (can be Matlab/AnaLib sim.) – show that it works
c) Mismatch Analysis add imperfections – show that it works.
d) Circuit Simulation/design – Take one block contain transistors

Project suggestions..

next lecture….

simulations tools

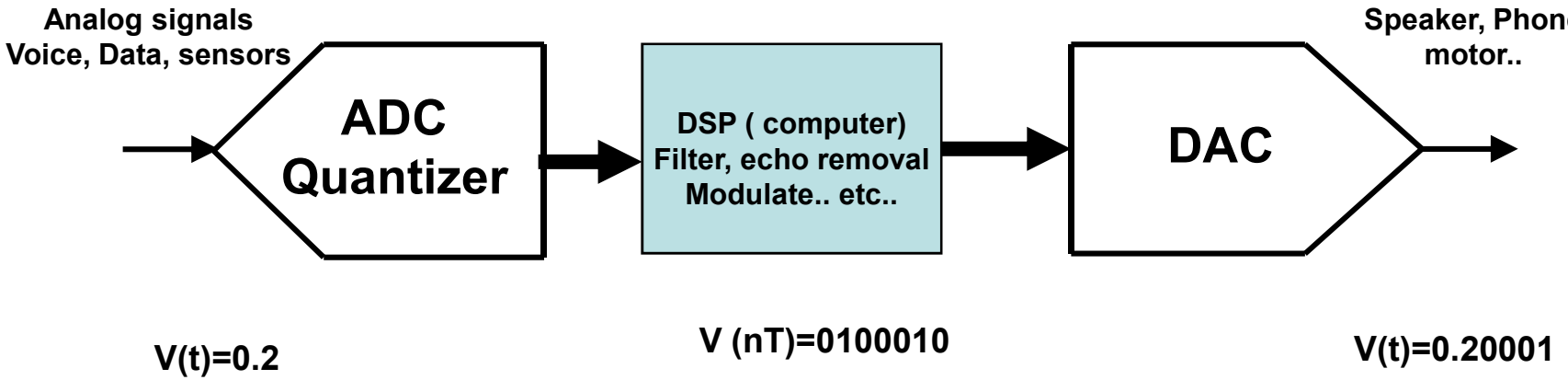
- At the university we have a workstation with Cadence and a general 90nm PDK.
- Can use Matlab for the project.

Example of Mixed Signal systems

Review of CMOS Transistor Basics

Example of Mixed Signal Systems

Converters



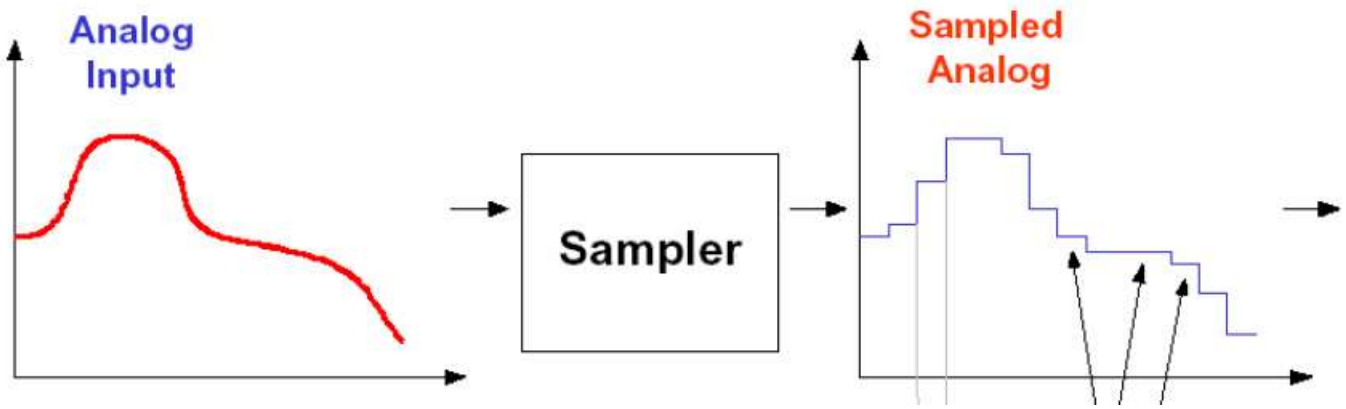
ADC –> DSP –> DAC

- It's a "Language" translator to do work. With fixed known boundary conditions **Vinmax and Minimin, maximum frequencies of throughput,**

- The process burn power, produces inaccuracies, creates bad artifacts- Folding, distortions - but allow communications to exists and to be stored.

In this course we will learn how converters works and how those errors are generated. And more precisely why/when we can let the error exists.

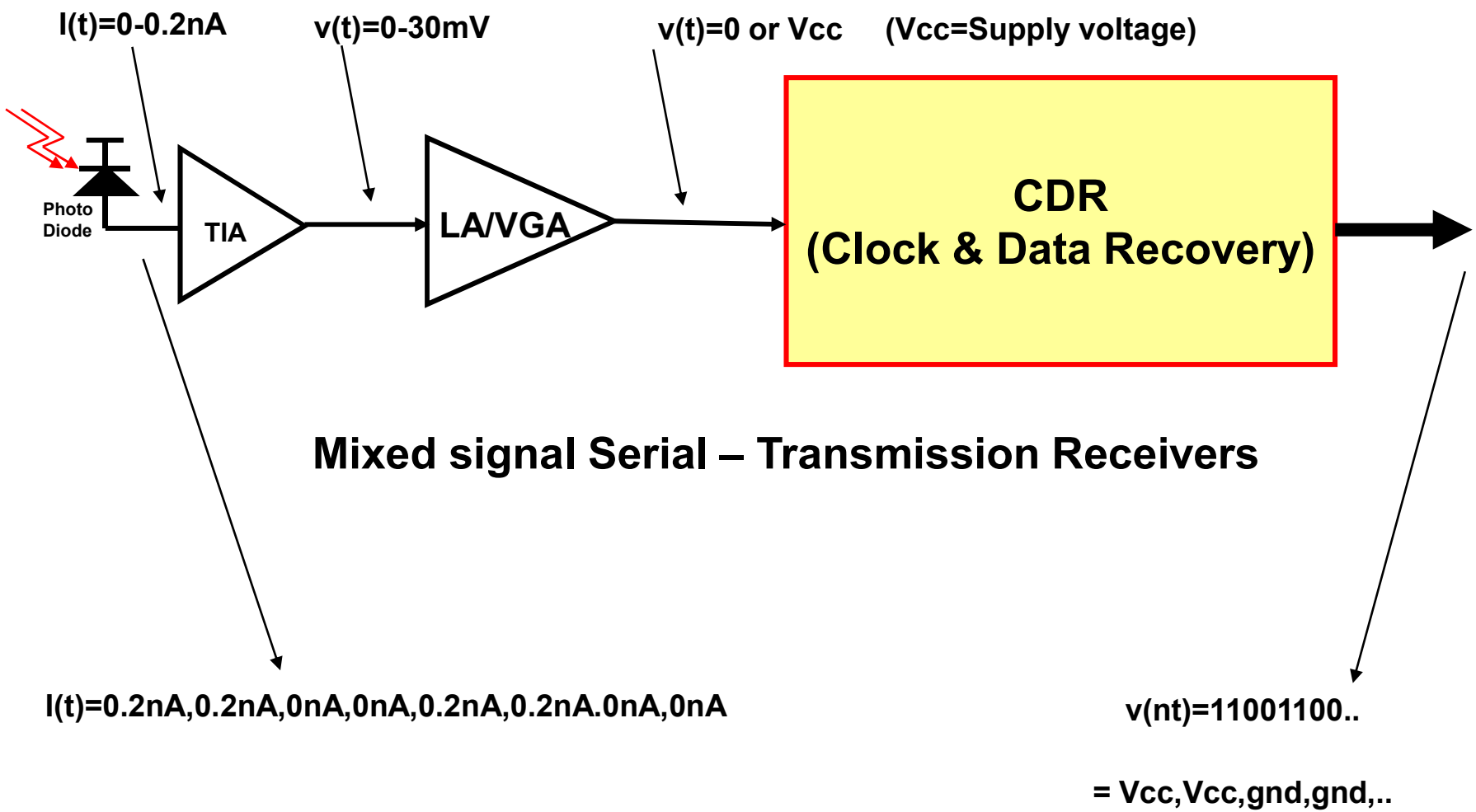
ADC representation



output is digital codes.

Sample at fixed time interval

Example of Mixed Signal systems



1. Review of Silicon based passives elements

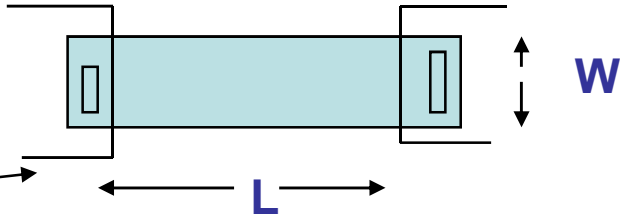
2. Review of CMOS Transistor Basics

Si Passive Elements Used in Mixed Signal - more in mismatch (lect4)

Silicon Resistors:

In Silicon **R** = Sheet resistance x Number of square. 6Ω -1KΩ /square

$$R = R_s \cdot squares(1 + \alpha T/T_0)$$

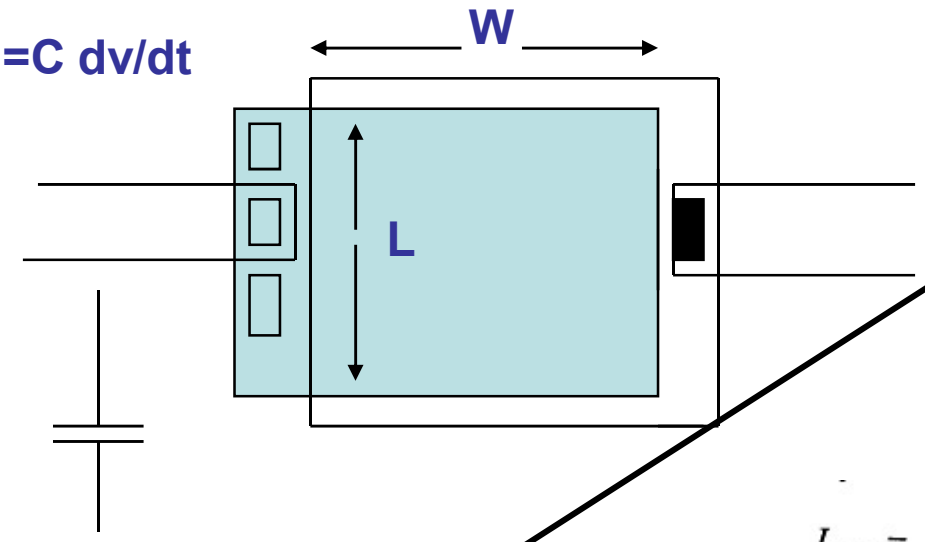


Si Top view

Capacitors

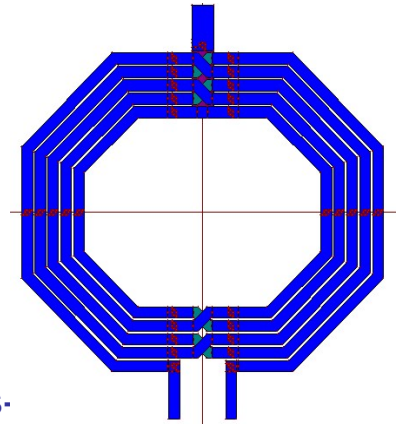
C= Ca x Area = Ca x W x L (W and L are dimension of plates)0.1-4 ff/uu

i=C dv/dt



Inductors

Inductors are also becoming a common elements.



$$L_{self} = \frac{\mu_0}{2\pi}\left[l \ln\left(\frac{2l}{w+t}\right) + \frac{l}{2} + 0.2235(w+t)\right] \quad (1)$$

Transistors : (CMOS in this example)

- 4 terminal device, mostly 3 terminals are used, the 4th is default connection - not always.
- CMOS works so nice because it is possible to build and repeat it: it is an efficient and dense element (~1.6million/mm^2 in 45nm tech.)
- Transistor can change its “function” and become R, C, or a voltage controlled current source(VCCS).
- Applying mostly the control voltage to the gate to source voltage.

Key is to understand which control does what!

$$i_{ds} = f(V_{gs}, V_{ds}, W, L, V_t, U, C_{ox})$$

CMOS Transistor Basics

Large Signal Equations for NMOS/PMOS transistor

Linear Region – A “resistors”

Strong Inversion – A current source (v-c-c-s)

Moderate Inversion – “transition region”

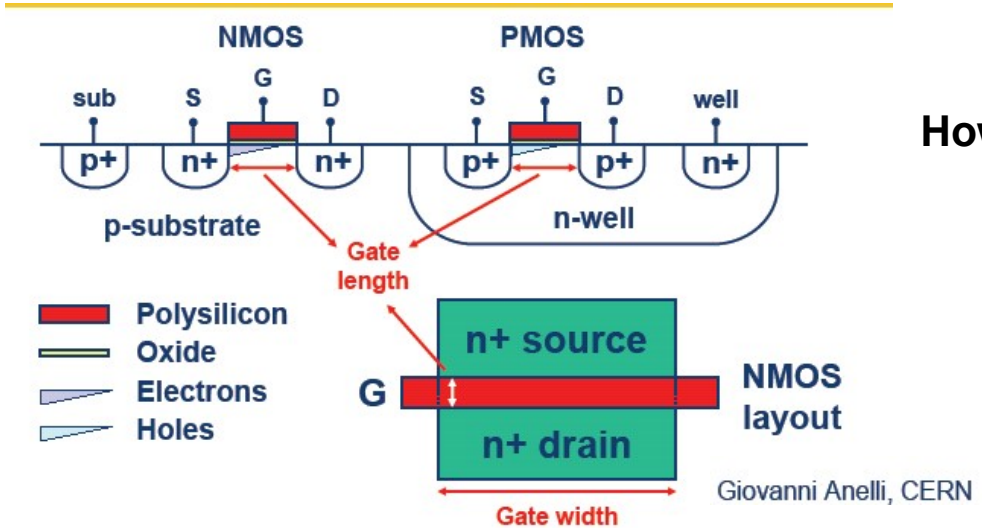
Weak Inversion – A “bipolar device” (Exponential i/v)

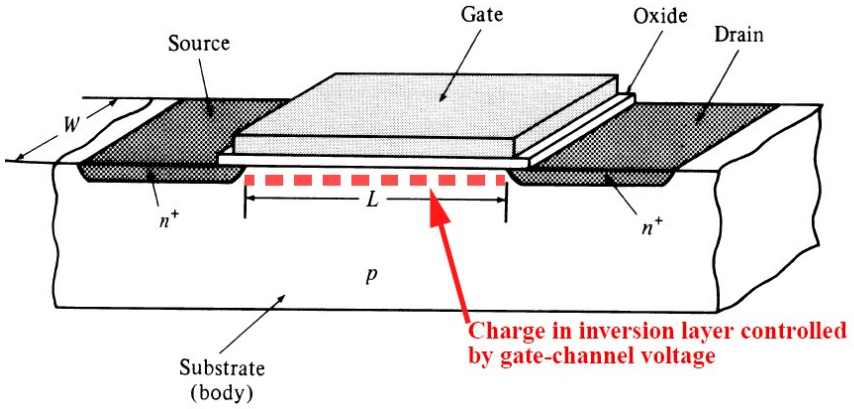
Off (Accumulation) – Open Switch

Velocity saturation, and Breakdown regions !
– important in sub um logic devices..!

Example:
A “digital cell” transistors could switch through all those regions

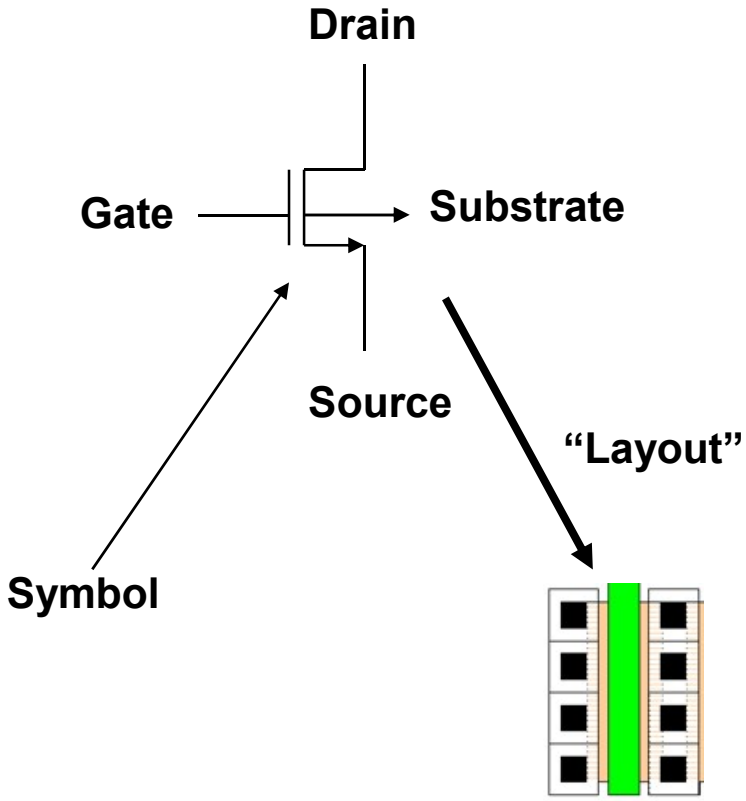
Physical Structure of NMOS / PMOS Transistor





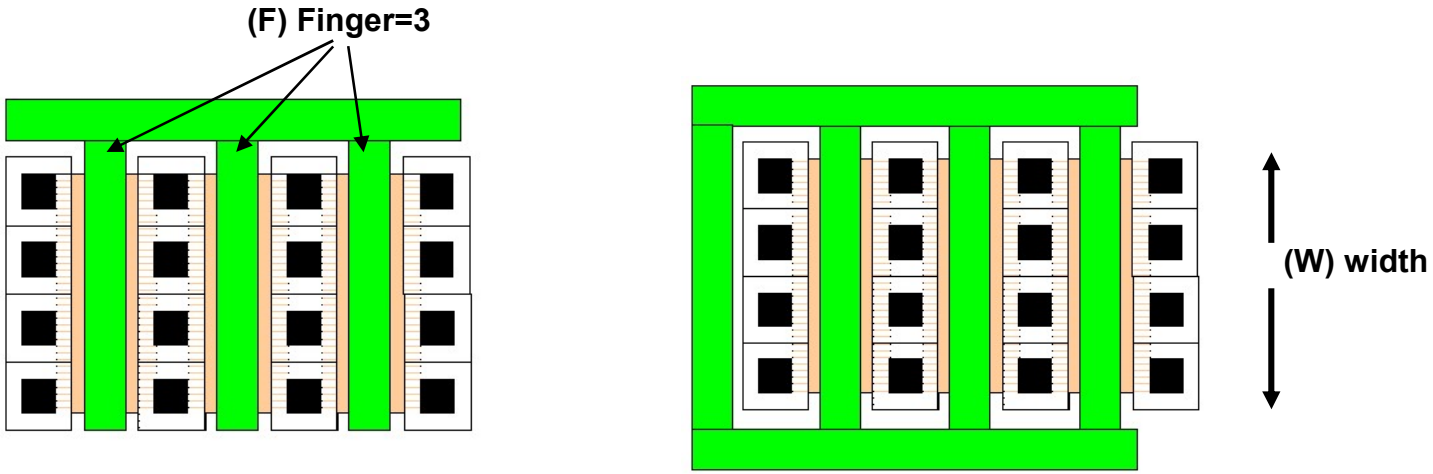
Source: IEEE & T.H. Lee.

How do we define W, L, Multiplier, Finger..?



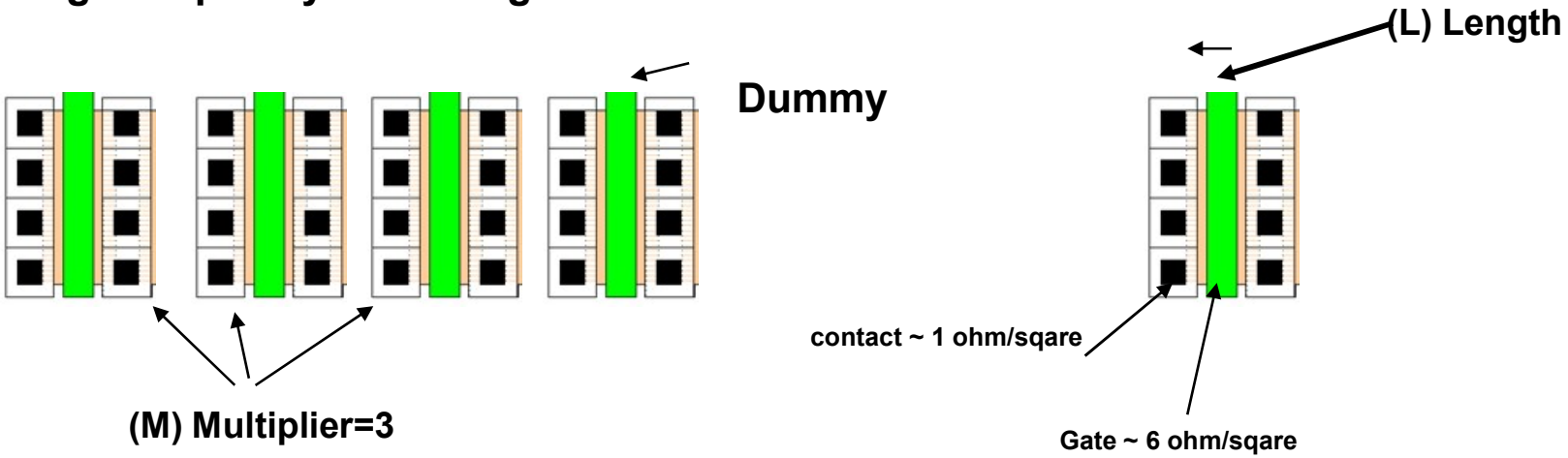
Transistor layout view

A very important part of Mixed Signal is placement and layout of the elements.



Now we have added errors:

Contacts resistance, metal routings and capacitance they can make difference at high frequency and at high currents



CMOS Transistor why we like them ?

- Technology Enhancement
  - Enhanced 28nm CMOS with 13 metal layers
  - 3 billion transistors on 588mm^2

~ 5.million transistors /1mmsquare.

Linear Region

- **Linear Region the Drain current is mobility time electric field (surface)**

$$I_D - W Q_n(y) \mu_n E$$

$$\int_0^L I_D dy = I_D L = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{DS} - V(y) - V_t] dV$$

Source: IEEE & T.H. Lee.

$$I_{ds} = \mu C_{ox} \left(\frac{W}{L}\right) [(V_{gs} - V_{th}) \cdot V_{ds} - \frac{1}{2} {V_{ds}}^2 \qquad V_{gs} - V_{th} > V_{ds}$$

- In this region electron are attached to the surface creating a conductive surface R which is Vds dependent (for small Vds)

- Mobility:

  how a charge carriers responds to an induced electric field, the mobility in Silicon MOSFET is roughly 400 cm^2/Vs

Saturation Region

If $V_{gs}-V_{th} < V_{ds}$ and $V_{gs}-V_{th} > \frac{3kT}{q} \sim 78mV$

Then: $$I_D = \frac{\mu \cdot Cox}{2} \cdot \frac{W}{L}(V_{GS} - V_T)^2 = \frac{\beta}{2}(V_{GS} - V_T)^2$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L}$$

Or we can define $V_{gs}-V_{th} \equiv Vsat$

- **Strong Inversion region**

  The inversion channel does not extend all the way to the end ”pinched off”

$$I_d = \mu C_{ox}\left(\frac{W}{L}\right)\left[(V_{gs} - V_{th}) \cdot V_{dsat} - \frac{V_{dsat}^2}{2}\right]$$

- **Strong Inversion, large Vds, transistor do not respond to drain movement – Great place to make a current element or to make an amplification… or an ADC, DACs**

Mobility in Silicon MOSFET is roughly 400 cm^2/Vs

In most design, to keep the transistor in saturation we always watch for Vdsat, and keep in mind that Vdsat is lower than Vds

Weak Inversion (sub threshold) Region

IF $V_{gs} - V_{th} < \frac{3KT}{q} \sim 78mV$ $\qquad Vds > \frac{4KT}{q}$

Then: $Ids = Ido\left(\frac{W}{L}\right) e^{\frac{Vgs}{nKT/q}}$

Keys:

- **Can happen at any Vds (above ~ 100mv)**
- **Transistor is Very large or has very small current!**
- **Slope: ~70mV per decade of current**

Where:

n (sometime k) is called Kappa around 0.7 and represents the coupling of gate to source potential

$$n = \frac{C_{ox}}{C_{ox} + C_{depl}}$$

Other Regions

Moderate Inversion – V_{gs}-V_{th} ~30-50mV
same as Sub threshold (transition place)

Off region – V_{gs}~0 leaky region I_{dss} and I_{gate}

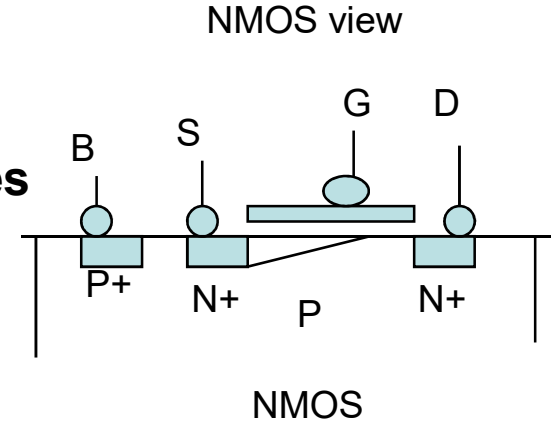
Mobility saturation – Large V_{gs} - V_{th} ~V supply or more.

Snap back – Very large V_{ds} exceed supply, a bipolar action

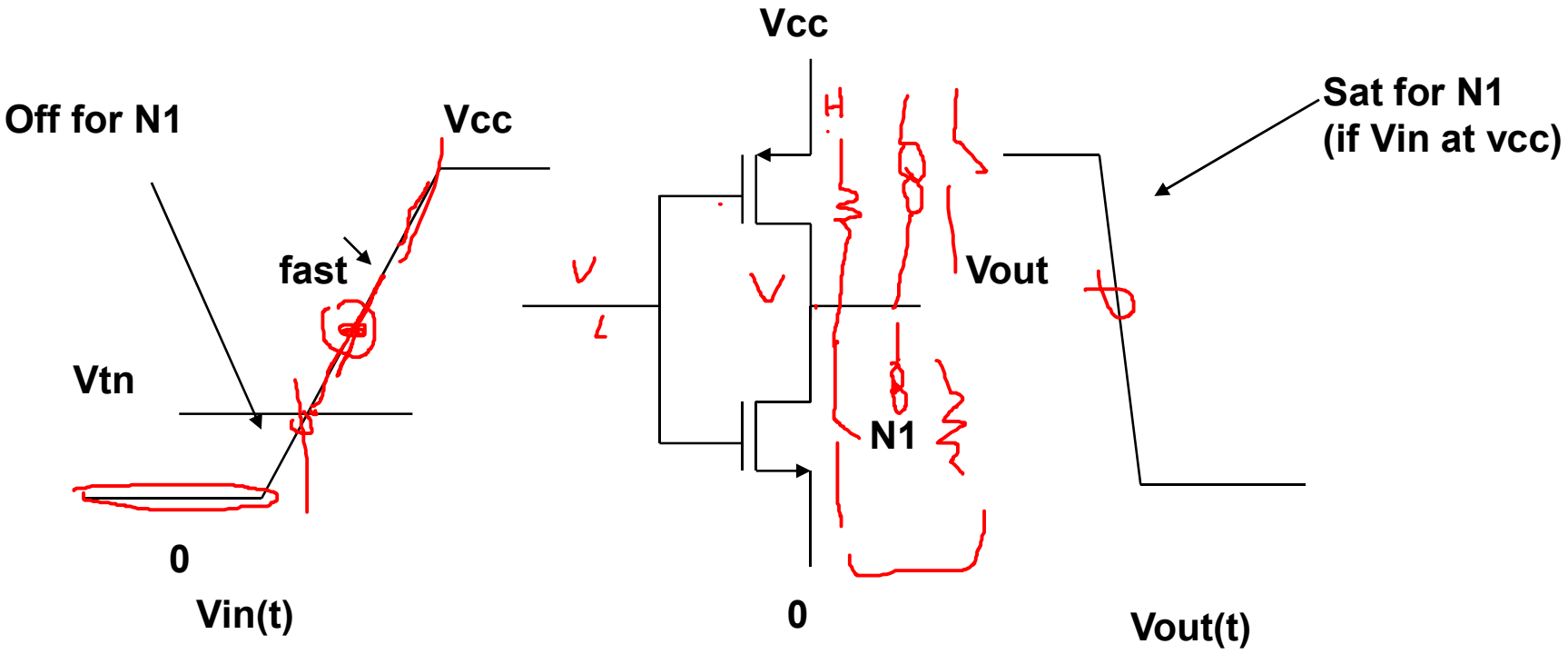
Off region is an interesting design parameter

it's a function of how big V_{th} is! And all leakages of all parasitic diodes

Source: IEEE & T.H. Lee.



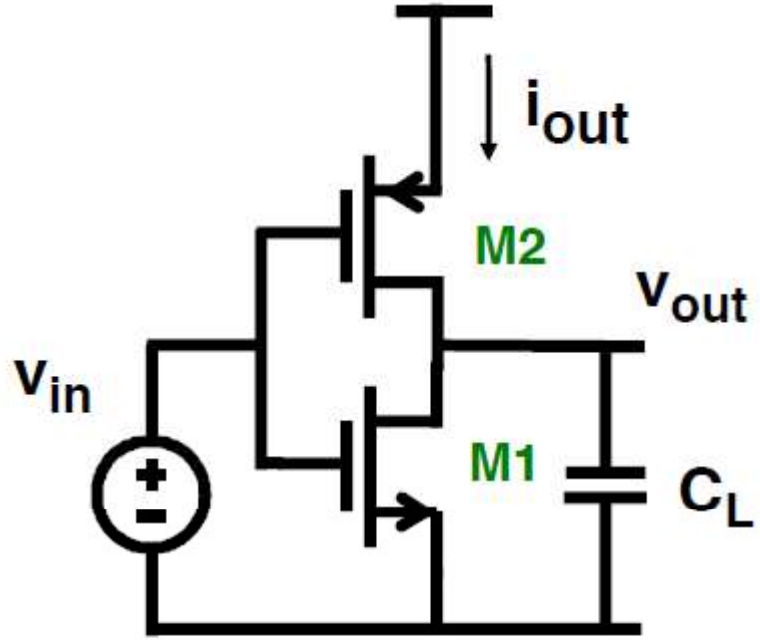
Inverter example- operate as Large Signal..



Example: In class analysis..
An inverter will switch through all those regions

But in most Analog/Mixed signals most transistors will stay in one region or will switch from Off to one of those region.

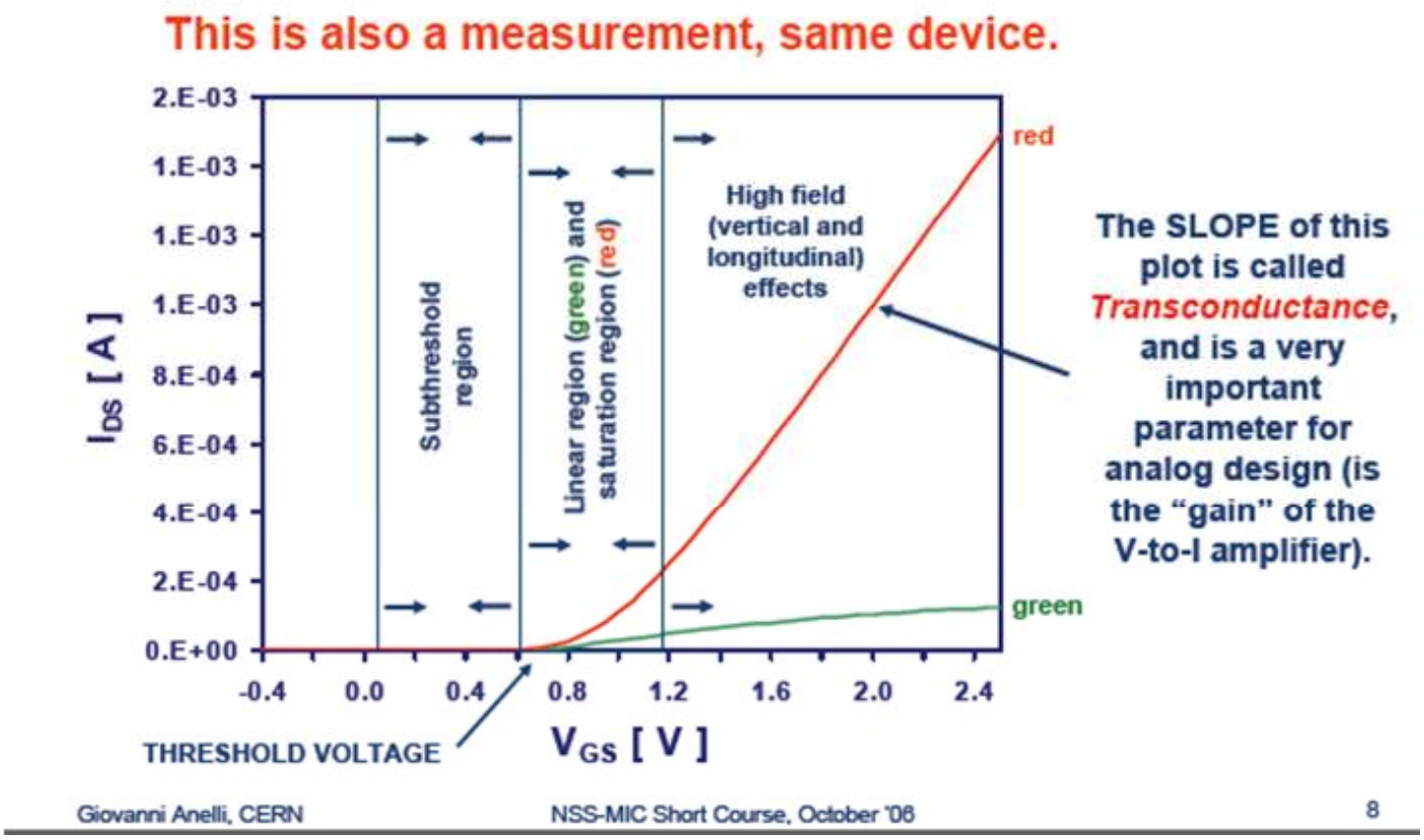
Inverter example- operate as small signal=all in sat....



$$v_{out} = A_v\, v_{in}$$

Class AB stage

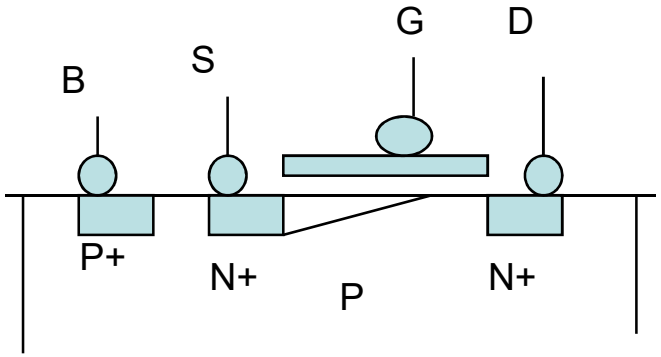
An Example: I_{DS} Vs. V_{GS}



gm~400e-6 is a typ number..

Good (for better understand) to convert the transistor to passive and active elements.

NMOS view



NMOS

Small Signal Transistor Parameters: g_m and G_{ds}

- Lets take the saturation region and assume the transistor V_{gs}-V_{th} does not change a lot. The current is set DC wise but fluctuate as we 'slightly' (small signal), move the Gate voltage.

Its important because the "quality" of the transistor in term of amplifications and output impedance is measured. (ignoring g_{msb})

$$V_{gs} - V_{th} < V_{ds}$$

$$I_{ds} = \mu C_{ox} \left(\frac{W}{2L}\right) (V_{gs} - V_{th})^2$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{th})$$

$$g_m = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right) I_{ds}}$$

$$\Delta I_{ds} = g_m \cdot \Delta V_{gs}$$

- **we want large gm but it cost:**
  Squaring the I_{ds}.
  Large W and small L – can helps

Tricky: what about V_t ?

Gds= Small Signal Transistor Parameters: g_m and G_{ds}

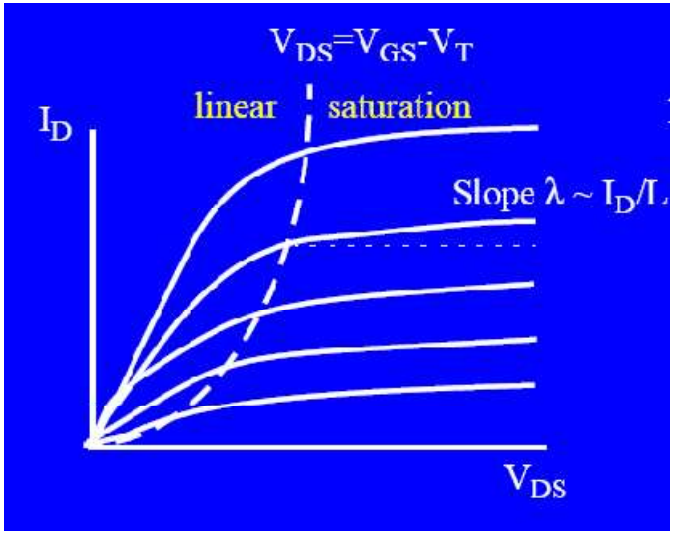
$$V_{gs} - V_{th} < V_{ds}$$

- At a fixed V_{gs}, I_{ds} is not constant in term of V_{ds} (replace sat current equation with- channel modulation)

$$I_{ds} = \mu C_{ox}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th}\right)^2 + (1 + \lambda V_{ds})$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \equiv \frac{1}{r_o}$$

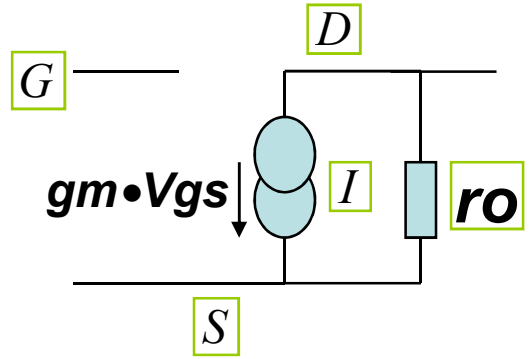
$$g_{ds} = \lambda \cdot \mu C_{ox}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th}\right)^2 = \lambda \cdot I_{ds}$$



Keys:

- r_o is proportional to L! And $1/I_{ds}$
  Slope: $1/r_o$
- Make long L if you like large r_o!
- Don't use much current
- Large r_o means current is unaffected W. V_{ds} changes

Gm= Model for Small Signal (no capacitors-DC)

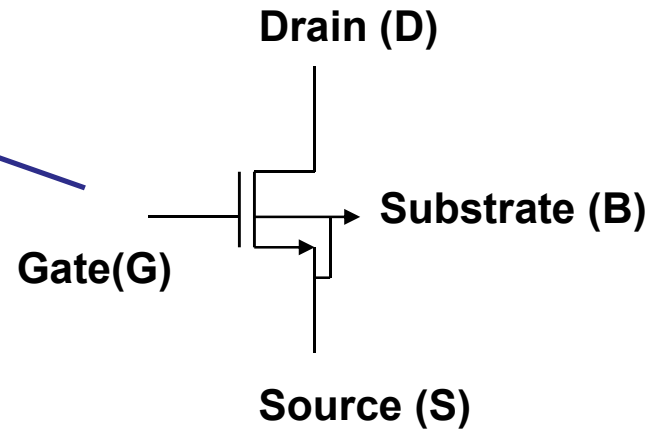


Model

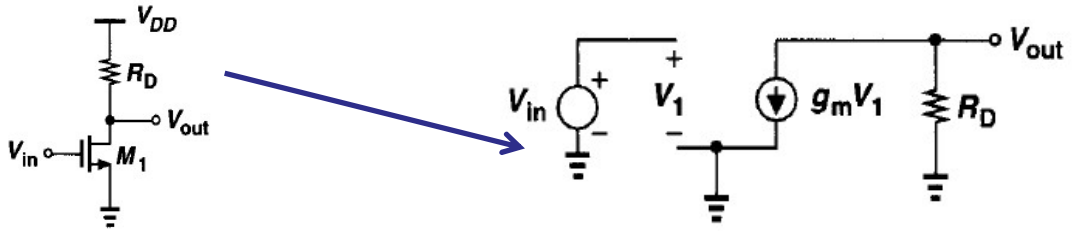
$$g_m \equiv \frac{\partial I_{ds}}{\partial V_{gs}} \qquad I_{ds} = g_m \cdot V_{gs}$$

$$g_{ds} \equiv \frac{\partial I_{ds}}{\partial V_{ds}} \qquad r_o = \frac{1}{\lambda \cdot I_{ds}}$$

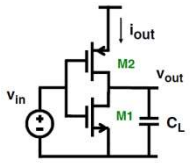
in small signal model Vgs, ids, ro, gm all are derivatives.. saturation



$-gm \bullet Vgs$ For Pch



on lecture 2 examples



$v_{out} = A_v\, v_{in}$

Class AB stage

Small Signal Transistor Parameters: g_{msb}

g_{msb} (an additional gain path)
Because V_t changes as a function of source to baulk:
(See V_{th} equation)

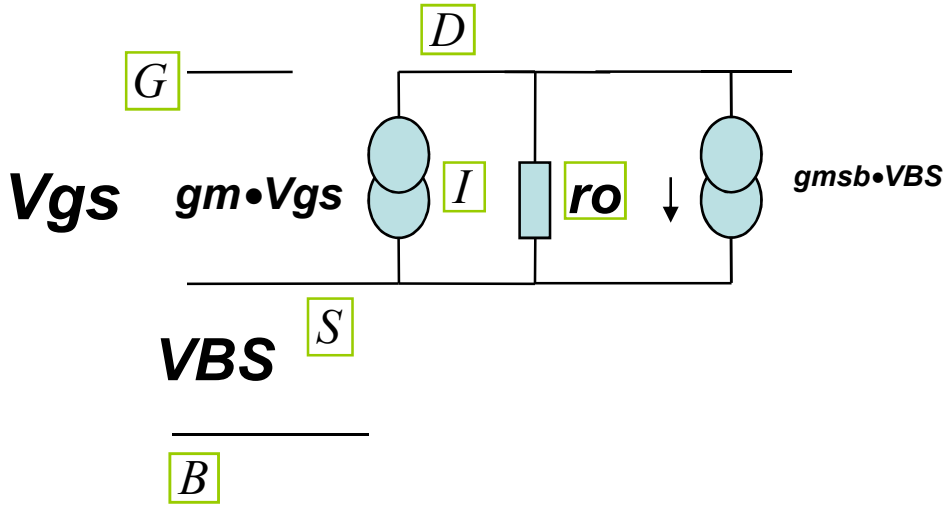
In many cases to avoid this gain path it is good to tie source to baulk !

$$V_t = V_{t0} + \gamma \cdot \left(\sqrt{2 \cdot \phi_f + V_{SB}} - \sqrt{2 \cdot \phi_f} \right)$$

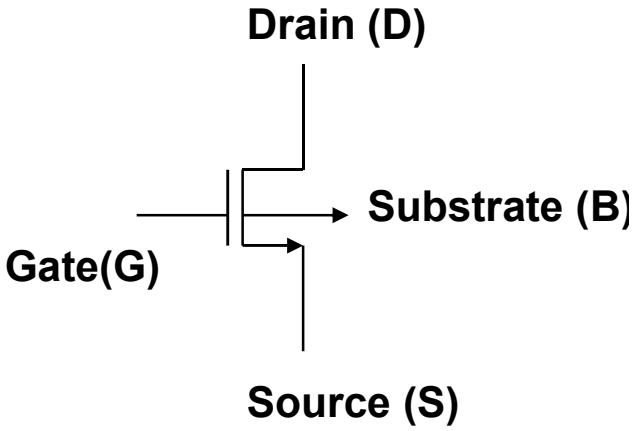
$$\frac{gmb}{gm} = \frac{\gamma}{2 \cdot \sqrt{2 \cdot \phi_f + V_{SB}}} = \chi$$

$$g_{msb} \equiv \frac{\partial I_{ds}}{\partial V_{sb}} = \eta \cdot g_m$$

η is In the range of $0.2g_m$ (every technology has an η)



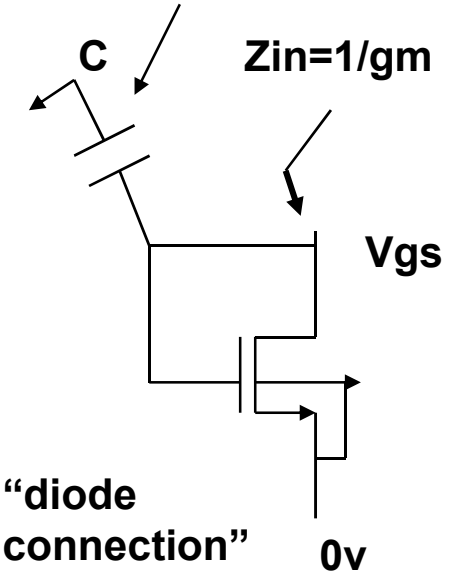
Model – with _ baulk



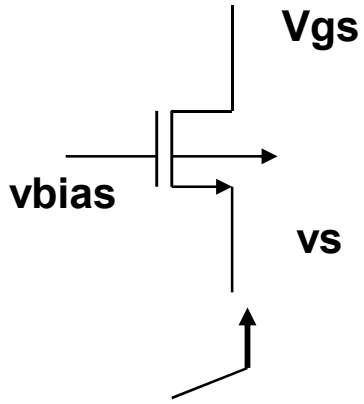
Convince yourself..

- Use the small signal model derive the impedance of n channel transistors below.

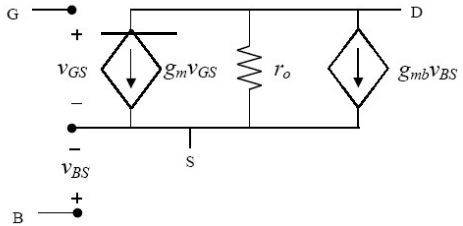
And what about C



"low Z"

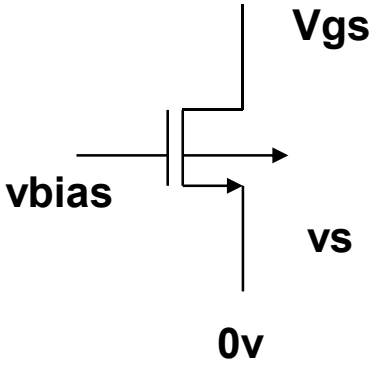


Zin=1/(gm+gmsb)



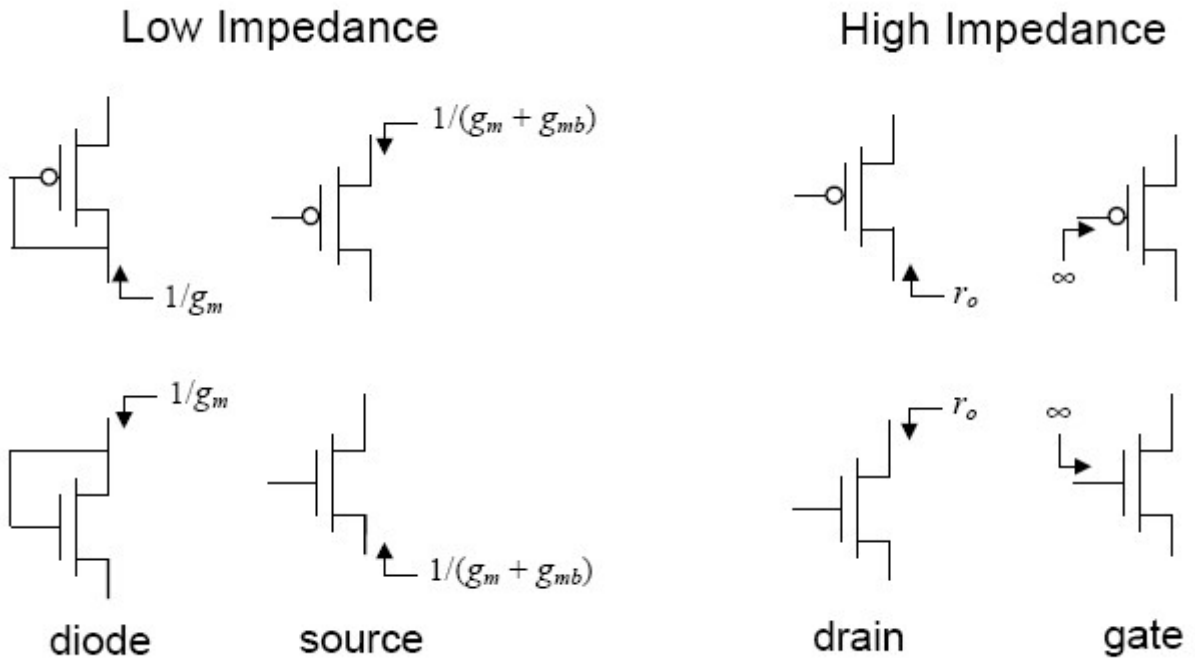
"high Z"

Zin=1/(gds)



An Example: Transistor Impedances:

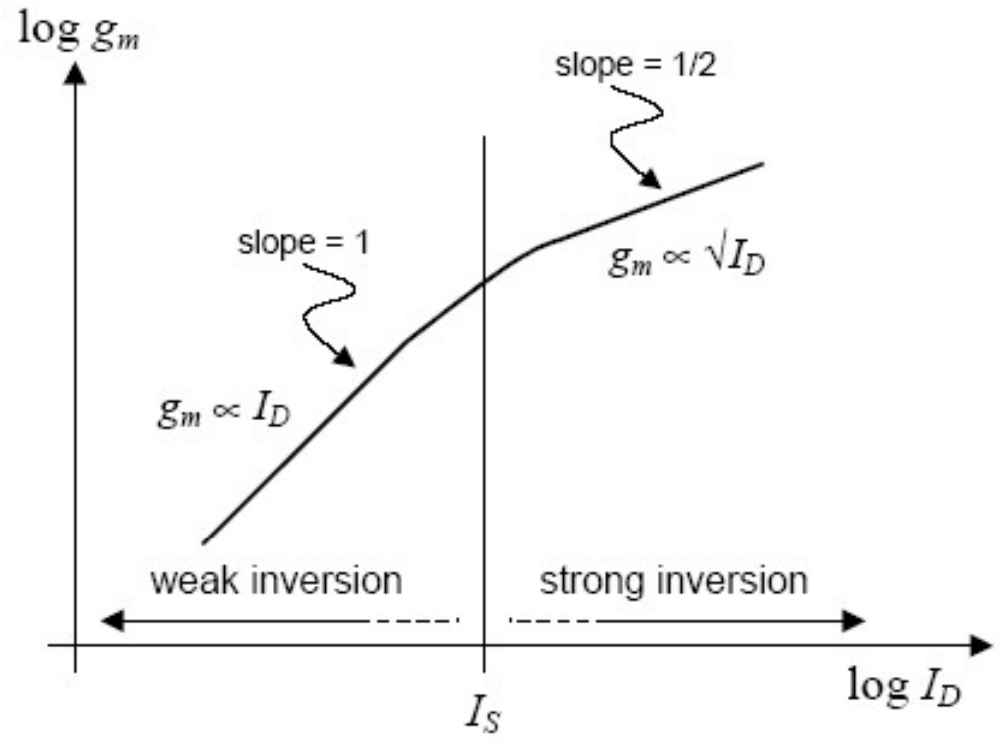
- MOS is a source device you move the drain nothing happen at the source but once you move the source the drain follow with gain!
- In NMOS source potential is lower than the drain And.. You can exchange source and drains- symmetrically.



Source: IEEE & T.H. Lee.

Gate impedance in thin gates is not infinite
Ig is becoming significant for L below ~ 65nm. (thin oxide) conventional CMOS

How g_m Behaves with at Different Regions



Source: R Harrison, Uof Utah

Source: R. Harrison.

Keys:

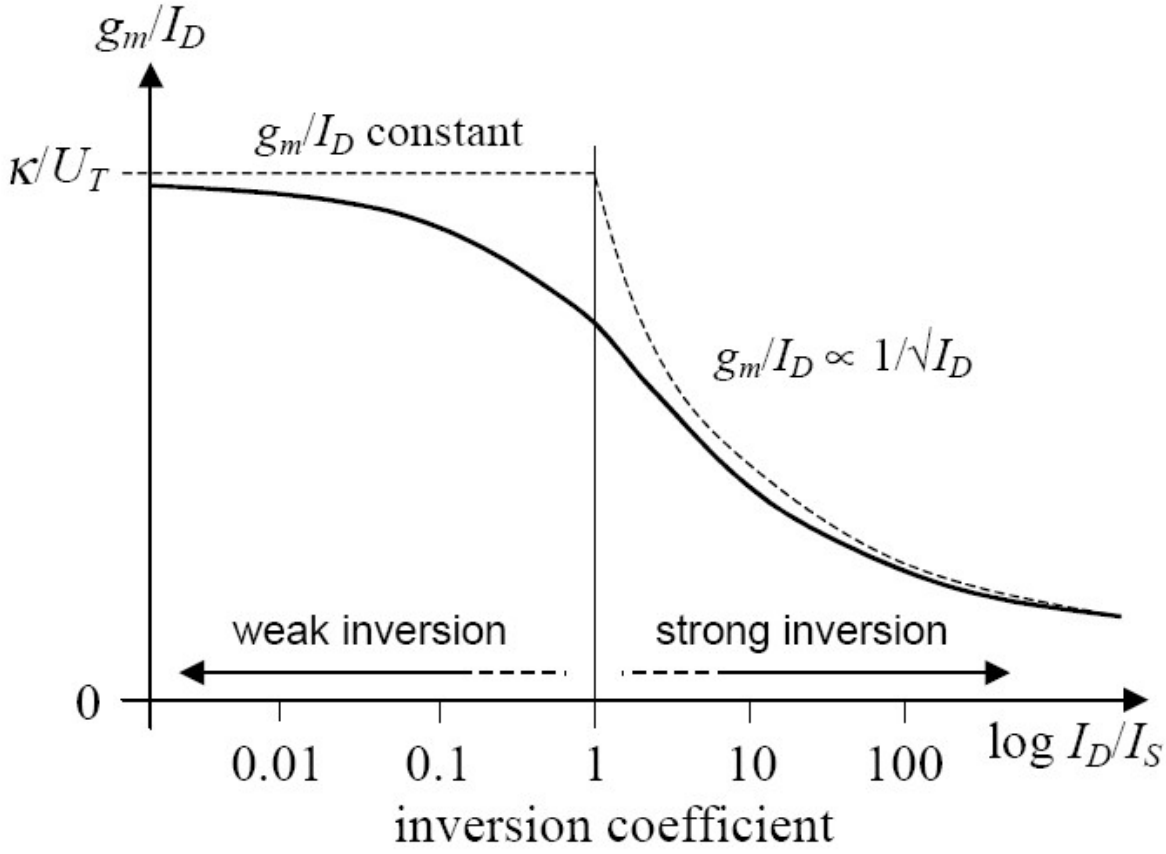
- g_m increases faster in weak inversion
- In moderate V_{ds}=30-80mv – g_m = ~ I_{ds}
- Small absolute g_m - Slow device

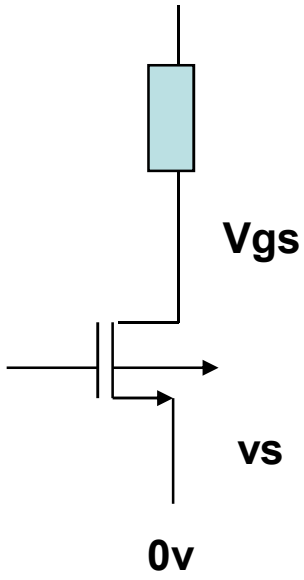
$$g_{msat} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{ds}}$$

$$g_{mwk\_inv} = \frac{I_{ds}}{KT/q}$$

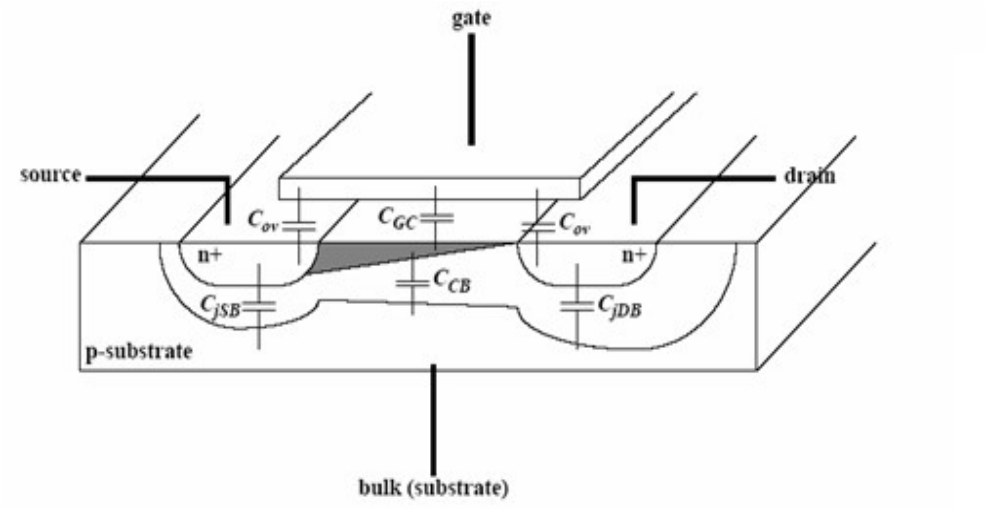
Gain => $-g_m \times r_o$

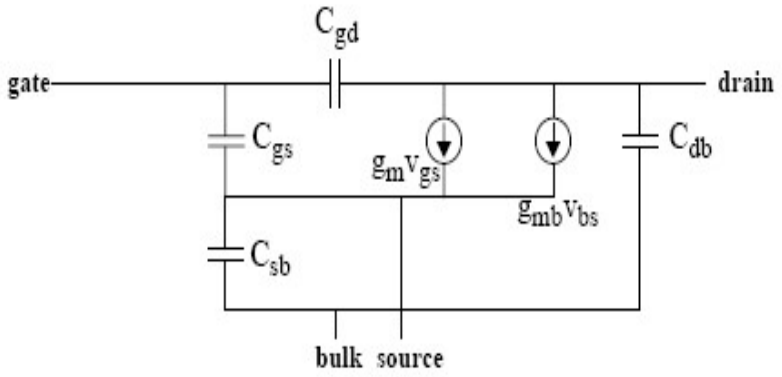
- **Another look** is relative g_m defined as g_m/I_{ds} (for low I design)
  But also the "gain" is
  $$g_m r_o = \sim g_m/I_{ds}$$





Capacitor of CMOS

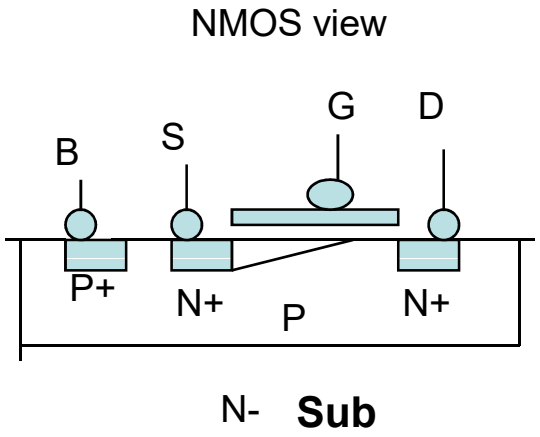


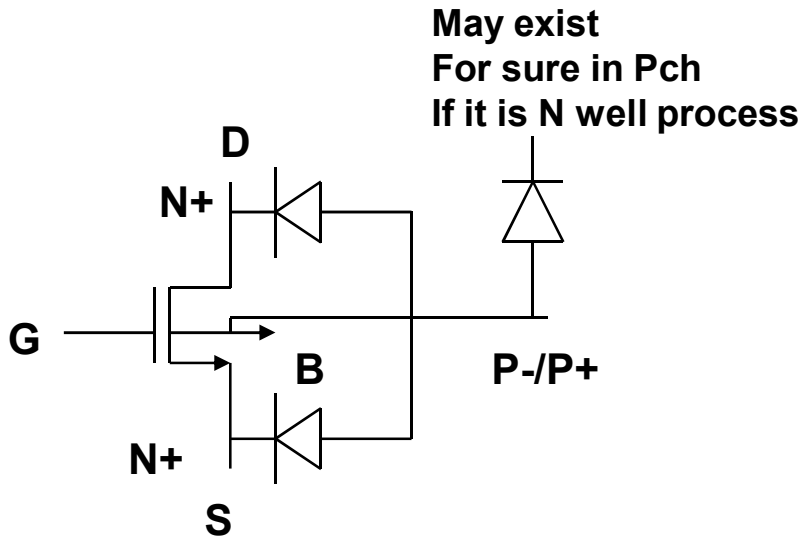


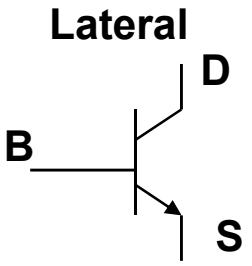
capacitors	Saturation	Linear	Off	
C gate to S	2/3Cox+Cov	1/2Cox+Cov	Cov	
C gate to D	Cov	1/2Cox+Cov	Cov	
C gate to B	0	0	Cox//Ccb+..	
C drain to B C source B	Cj(diode) CJ	Cj Cj	Cj CJ	Voltage dependance

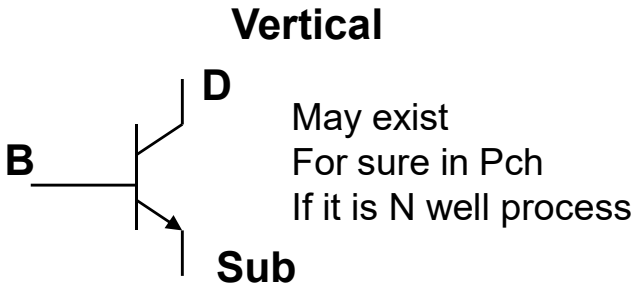
Source: IEEE & T.H. Lee.

❑ CMOS Model – Never forget the Parasitic Bipolar/diodes !

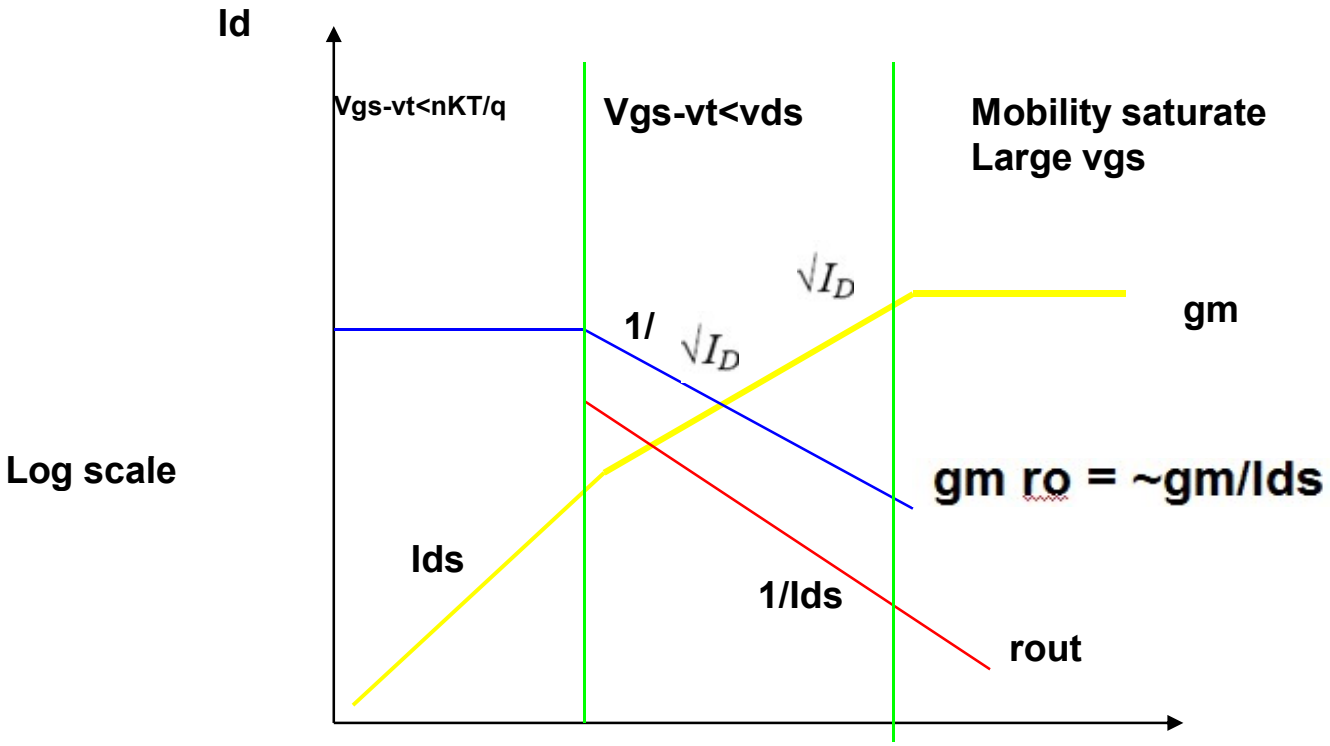








Summary



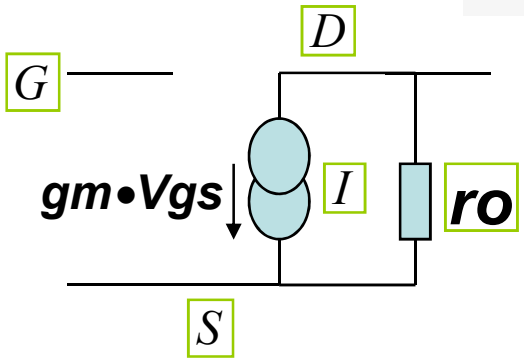
Region dependency on Ids

Source: R Harrison, Uof Utah

Summary

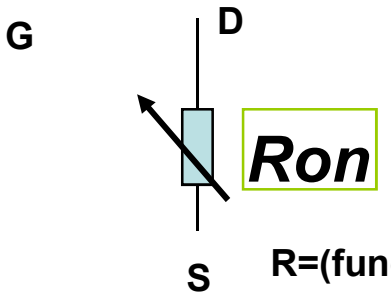
Saturation

$$I_{ds} = \mu C_{ox}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th}\right)^2(1 + \lambda V_{ds})$$



Linear

$$I_{ds} = \mu C_{ox}\left(\frac{W}{L}\right)\left[\left(V_{gs} - V_{th}\right)\cdot V_{ds} - \frac{1}{2}{V_{ds}}^2 \qquad V_{gs} - V_{th} > V_{ds}\right.$$



R=(function of vgs,vds)

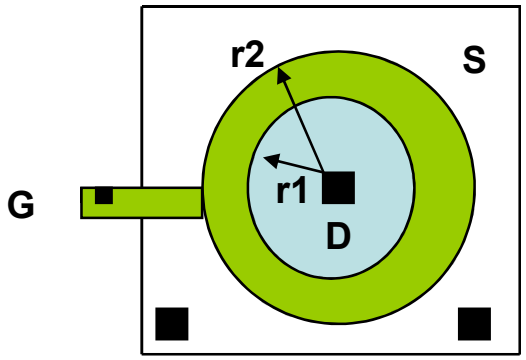
Sub Threshold

$$Ids = Ido\left(\frac{W}{L}\right)e^{\frac{Vgs}{nKT/q}}$$

"Rule of thumb" : 70mv/decade of I

Now add capacitance according to Mode of operation on table provided

optional

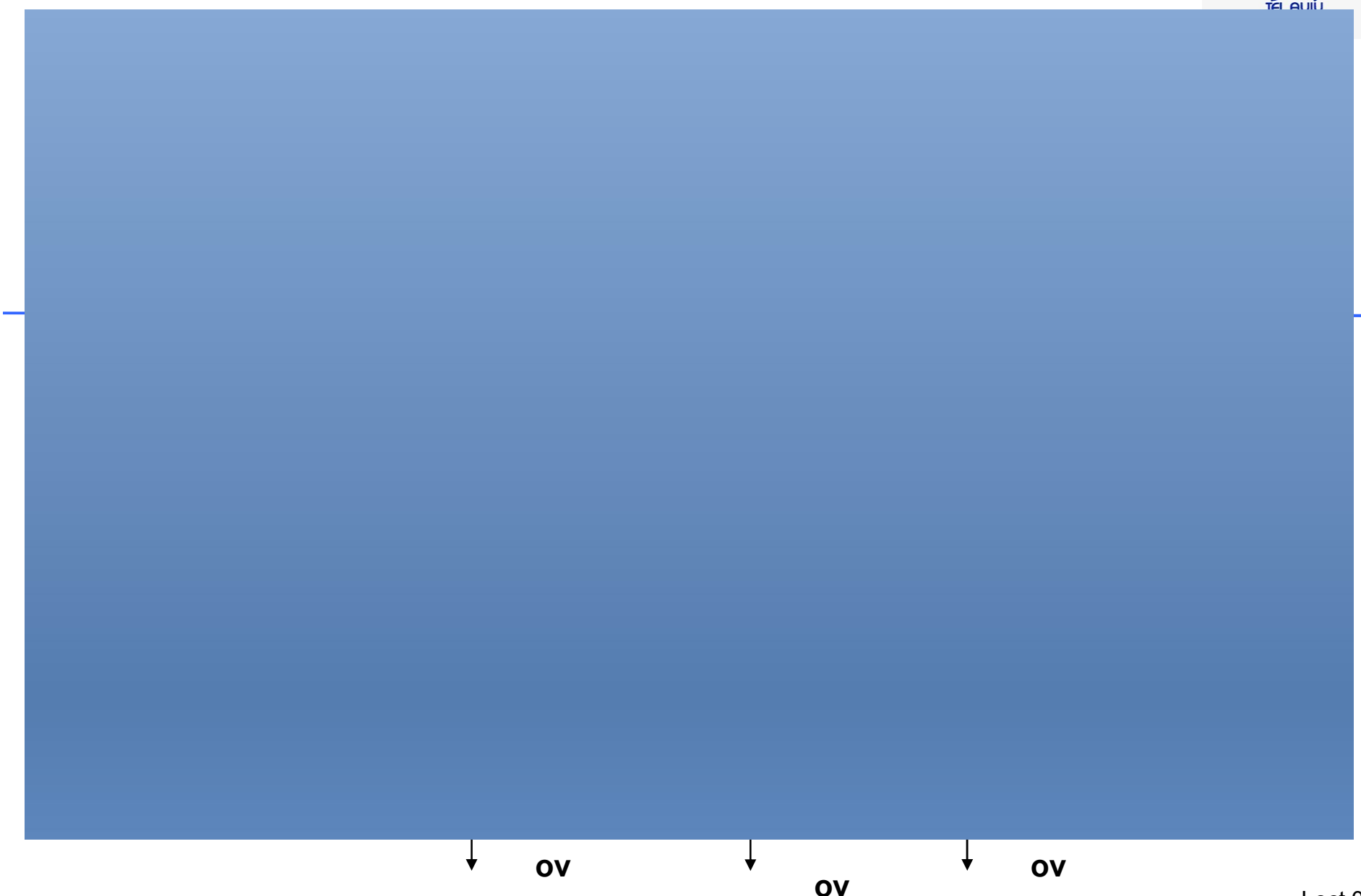


1. What is W/L of a round donut shape transistor?

2. Can you derive it?

3. What is it good for?

Homework 1/3 – next lecture. 20%.



END Lect. 01