Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 12

Parallel ADCs- Time Interleaved ADC

Calibration techniques

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Agenda

Architectures

Source of Errors

Calibration Methods

Analysis

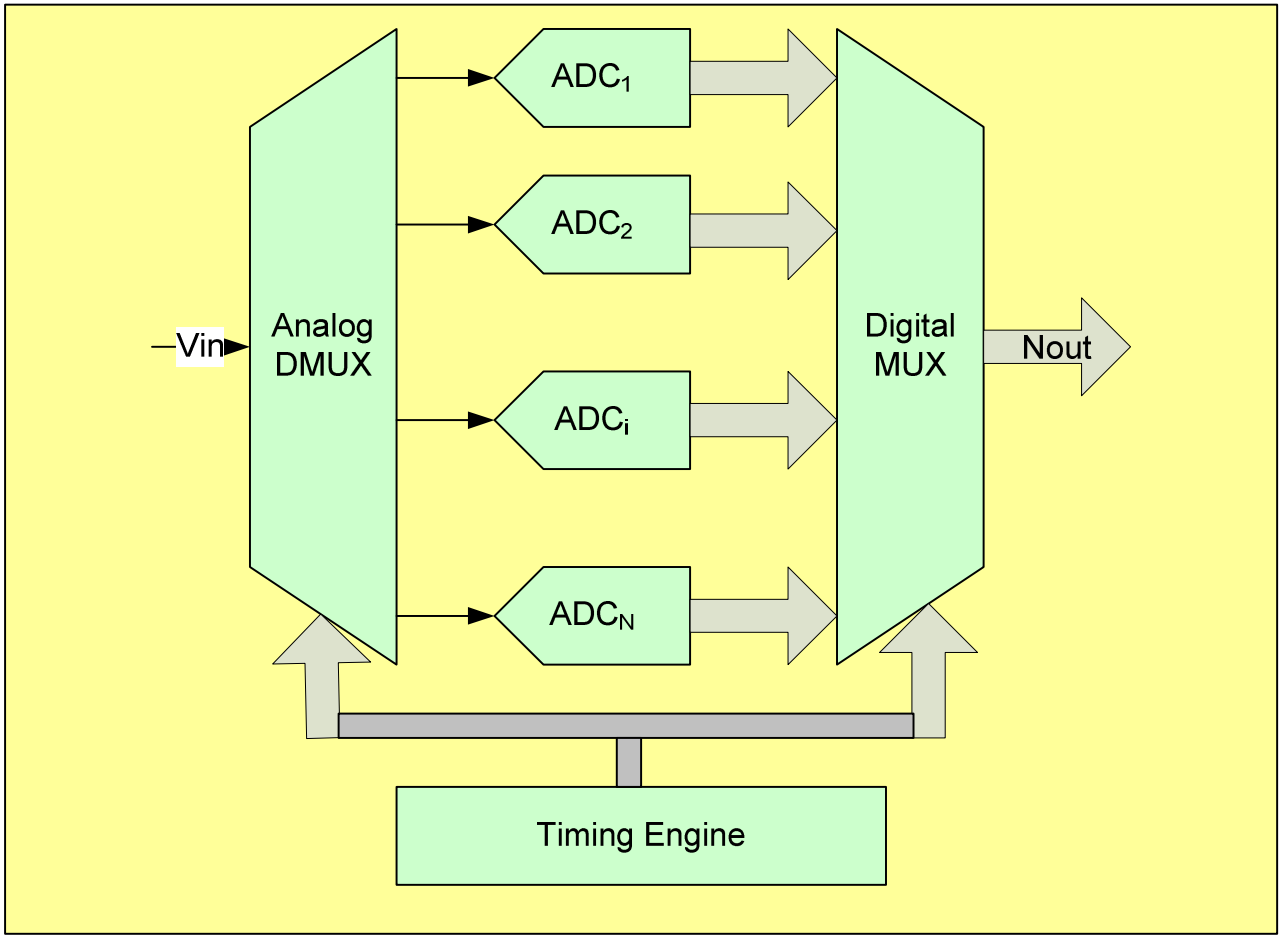
Design Example

Basics-Reason

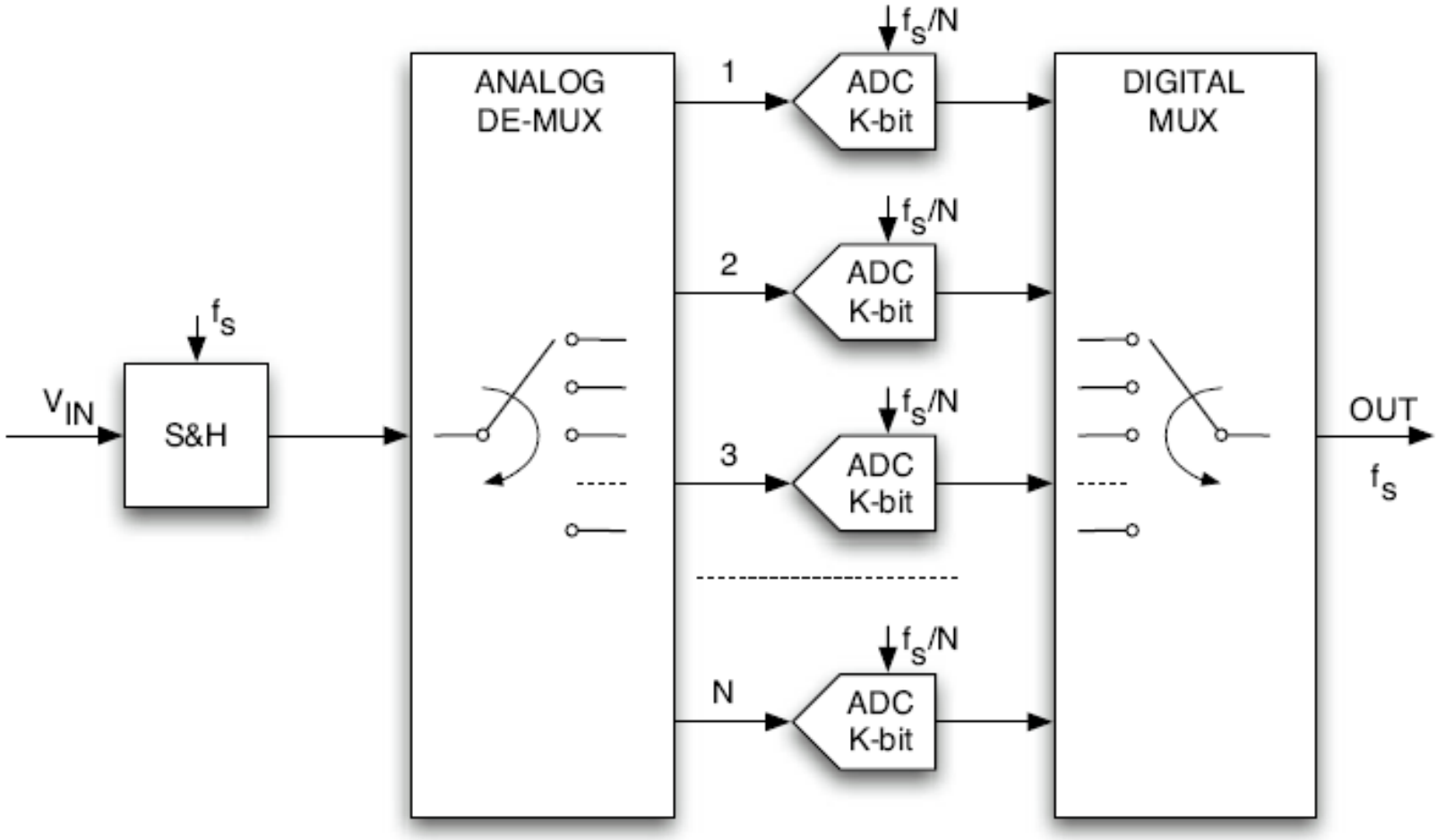
- Time Interleaved ADC Architectures
  - The concept of time interleaving
  - Mismatch Artifacts in Time Interleaved ADC
  - Time Interleaved ADC Examples
- ADC Calibration Techniques
  - The concept of ADC Calibration
  - Limitations of ADC Calibration
  - Classification of Calibration Techniques
  - Examples of ADC Calibration Techniques
    - Trimming Techniques
    - Digital Calibration in Pipeline ADC
    - Digital Calibration with State Space Error Table

1a. Time Interleaved ADC Approach (1)

- **System Level Concept:**

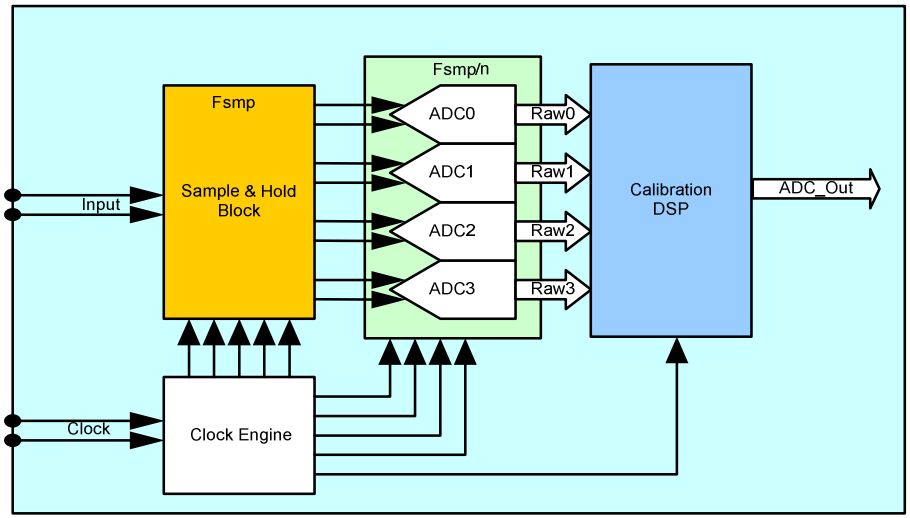


MUXING interface



1a. Time Interleaved ADC Approach (2)

- Partition the problem of building a high resolution ultra-fast ADC to 3 main sub-problems:
  - Build a nx time-interleaved sample and hold
  - Build n identical ADC-s that each samples at Fsmp/n
  - Perform digital signal processing to eliminate/reduce interleaving artifacts



HOW TO CHOOSE ? –

Example: in class.
SAR Interleaving ADC
Backward approach:

Given technology

1) design a comparator find its maximum speed- use desired power Idd- call it time: T1

2) Design best Digital FF (logic) : determine speed T2

3) Switch time to charge maximum cap MSB T3

3) T=T1+T2+T3 this is roughly maximum one cycle

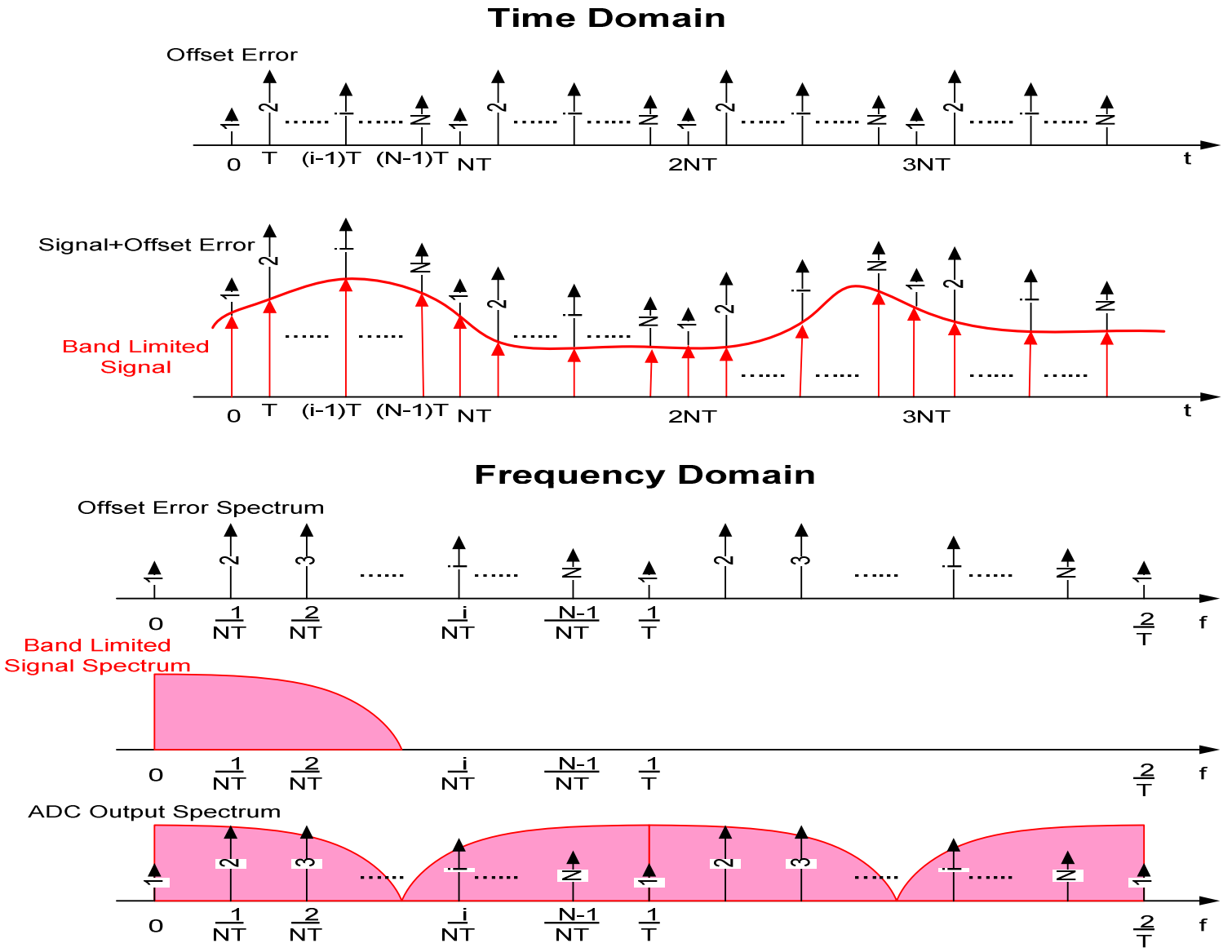
clock speed is T , need number of bit +1 Time per ADC.

2x BW needed

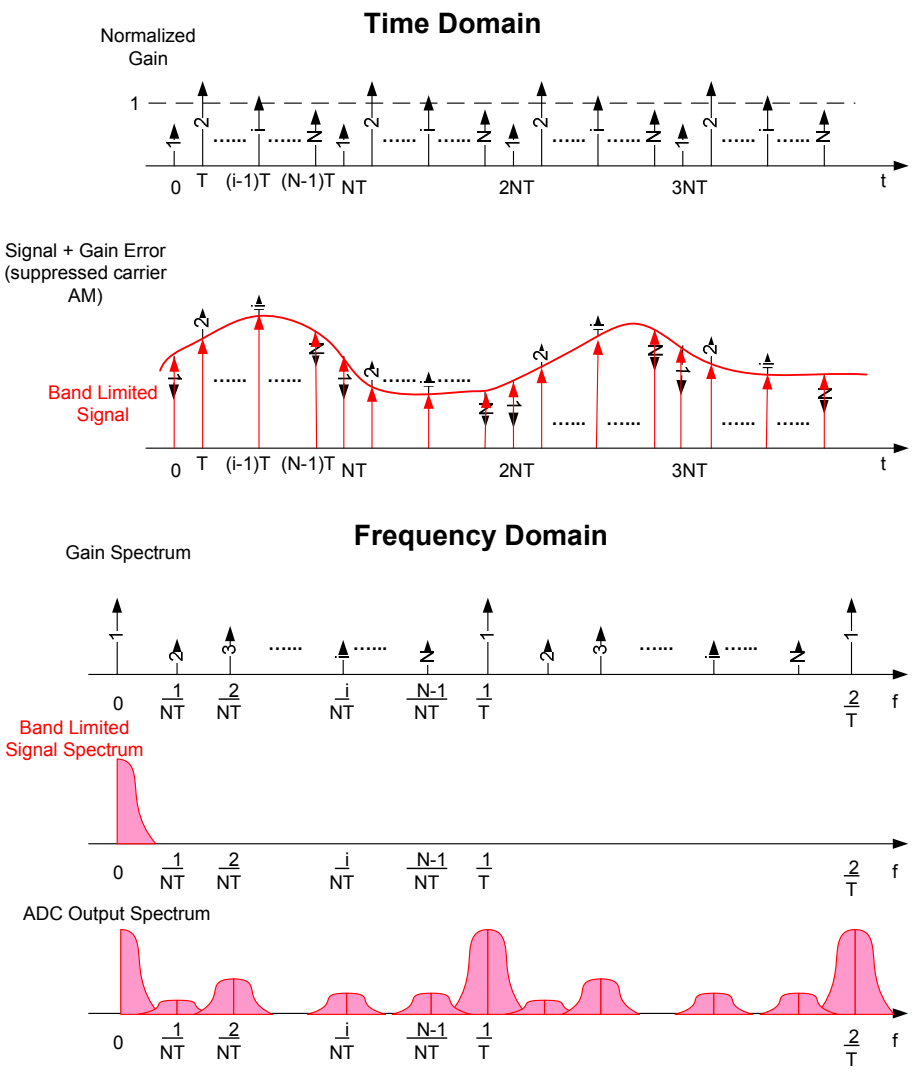
1b. Mismatch Artifacts due to Time Interleaved Architecture (1)

- The branches of a time interleaved ADC are not identical
- There are 3 main mismatch issues:
  - Offset mismatch
  - Gain mismatch
  - Timing instance skew
    - can be overcome if full speed sample and hold is used
    - Can be corrected in DSP – generalization of Nyquist theorem for non-uniform sampling

1b. Mismatch Artifacts due to Time Interleaved Architecture (2 - Offset)



1b. Mismatch Artifacts due to Time Interleaved Architecture (3 - Gain)



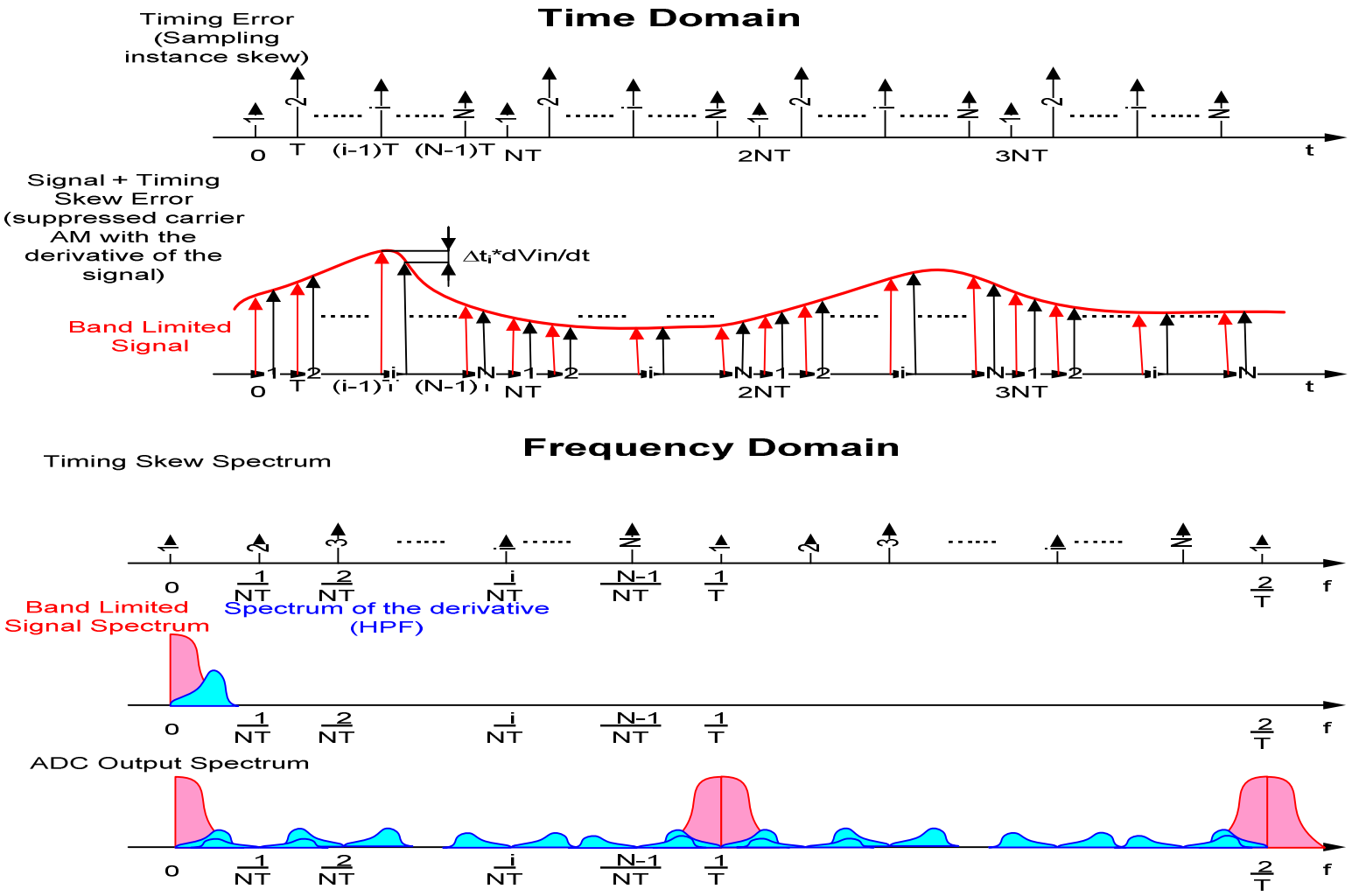
Analytical Formulas:

N. Kurosawa, K. Maruyama, H. Kobayashi, H. Sugawara, K. Kobayashi
, "Explicit Formula for Channel Mismatch Effects in Time-Interleaved ADC Systems", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Volume: 48 , Issue: 3 , March 2001,

Pages:261 – 271

$$SNR_{Missmatch} = -10 \cdot \log\left(\sigma_{\Delta G}^2 + \frac{8 \cdot \sigma_{Noff}^2}{N_{FS}^2}\right)$$

1b. Mismatch Artifacts due to Time Interleaved Architecture (4 Timing Skew)



Five Important Sources of Mismatch

- Offset mismatch
- Gain Mismatch
- Clock Skew

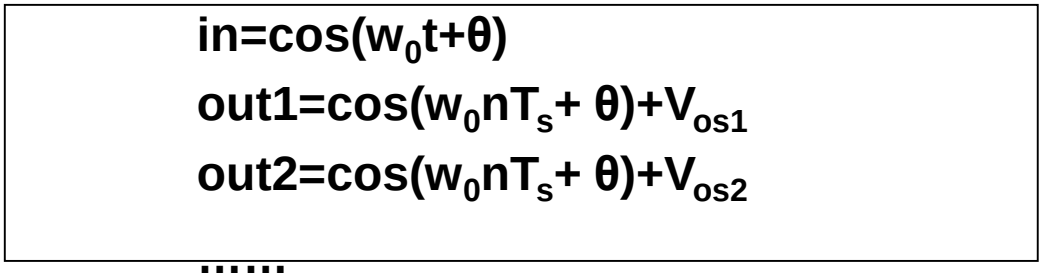
  - Bandwidth Mismatch

    Make sure that BW is wide enough
  - Jitter

    Use a low-jitter source

KEY DEPENDENCIES

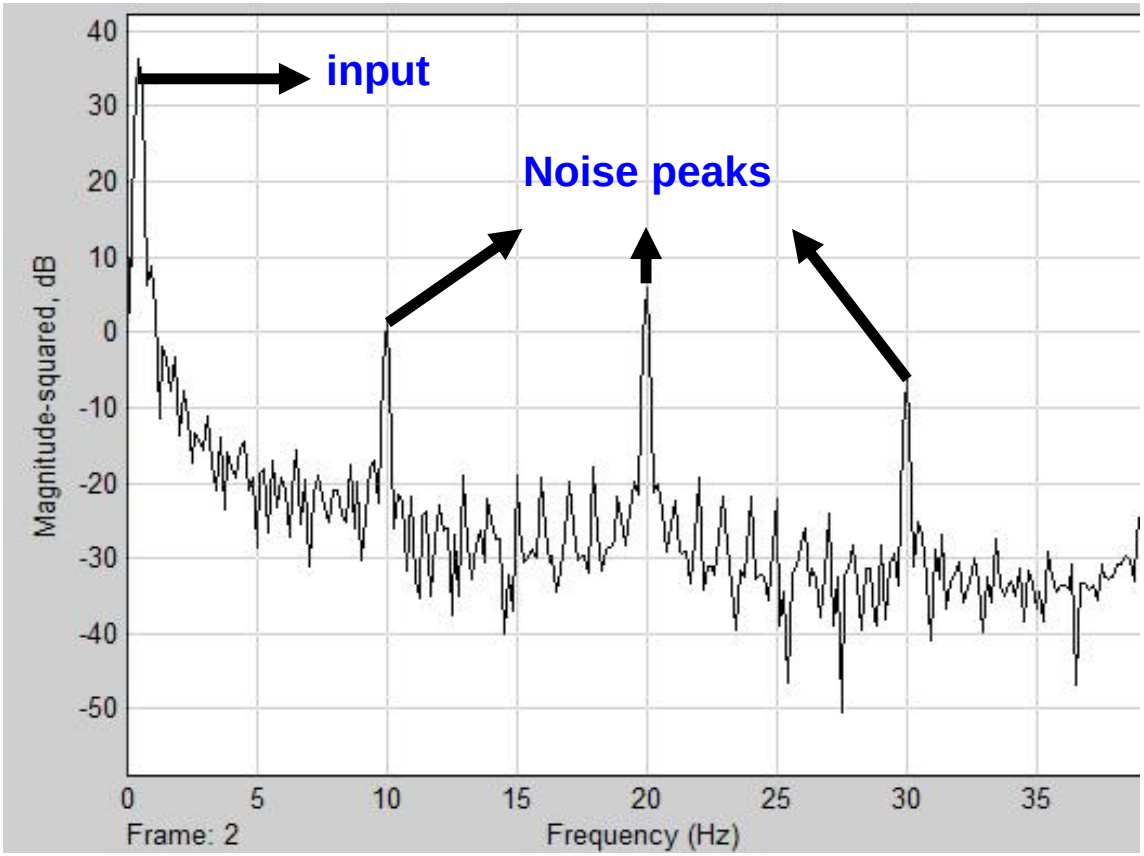
	SNR Degradation Due To			
	Offset	Gain	Clock skew	BW
Input amplitude	independent	Linearly dependent	Linearly dependent	Nonlinearly dependent
Input frequency	independent	independent	Linearly dependent	Nonlinearly dependent



- Input amplitude and frequency independent
- Causes fixed pattern noise
- Noise peaks at frequencies, f=k*Fs/M

- **M=# of interleaved ADCs**
  - Fs=sample frequency
  - k=1, 2, 3, … M-1
- Noise peak amplitudes are offset voltage dependent

Offset sim example… SAR ADC



Spectrum of a 4-channel interleaved ADC model

Fin=0.5Hz, Fs=40Hz

Noise peaks at 10Hz, 20Hz, 30Hz

Gain Mismatch Problem

$$in=\cos(w_0 t+\theta)$$

$$out1=G1*\cos(w_0 nT_s+\theta)$$

$$out2=G2*\cos(w_0 nT_s+\theta)$$

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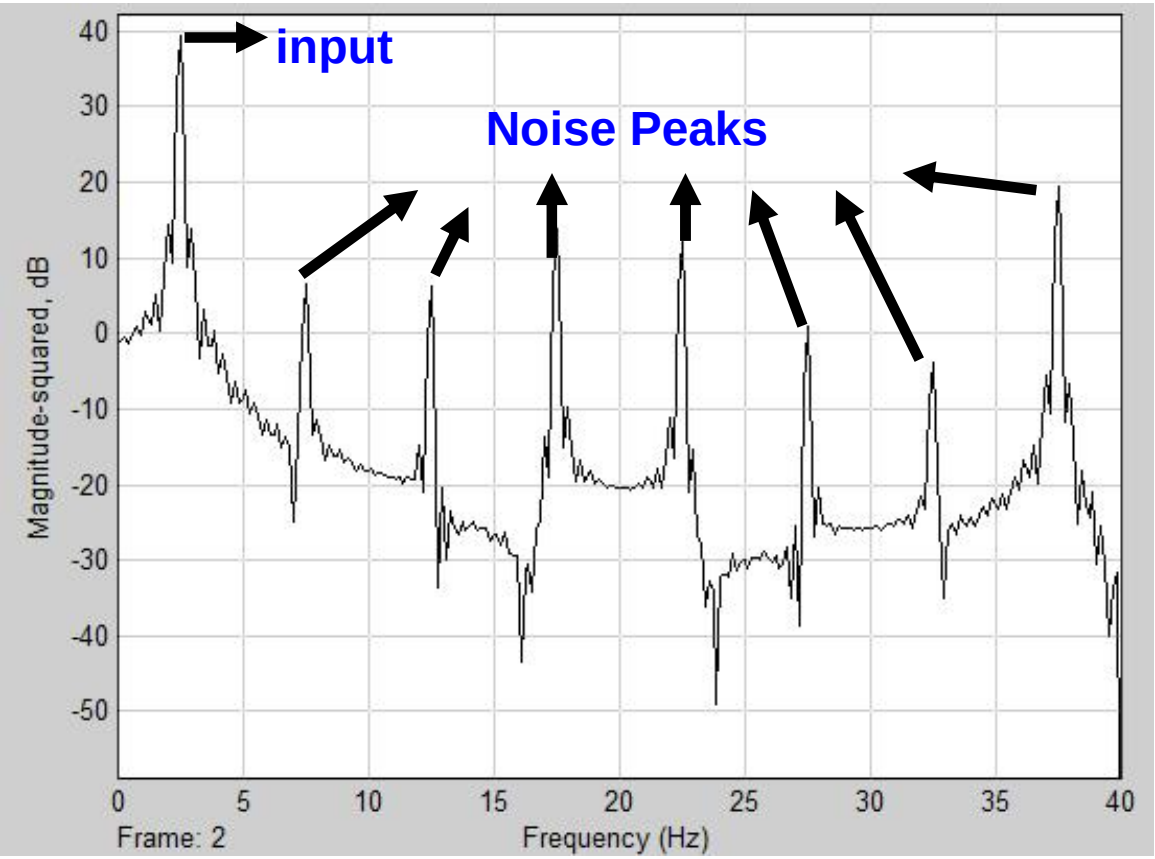
- Error is max and min when the input is max and min, respectively
- Linear input amplitude dependency
- Input frequency independent
- Noise peaks at frequencies, f=±fin+k*Fs/M
  - fin=input frequency
  - M=# of interleaved ADCs
  - Fs=sample frequency
  - k=1, 2, 3, … M-1

Gain Mismatch Problem



Spectrum of a 4-channel interleaved ADC mode

Fin=2.5Hz, Fs=40Hz

Noise peaks at 7.5Hz, 12.5Hz, 17.5Hz, 22.5Hz….

Timing Mismatch Problem

$in=\cos(w_0 t+\theta)$

$out1=\cos(w_0 n_1 T_s+ \theta)$

$out2=\cos(w_0(n_2 T_s+dT+ \theta)$

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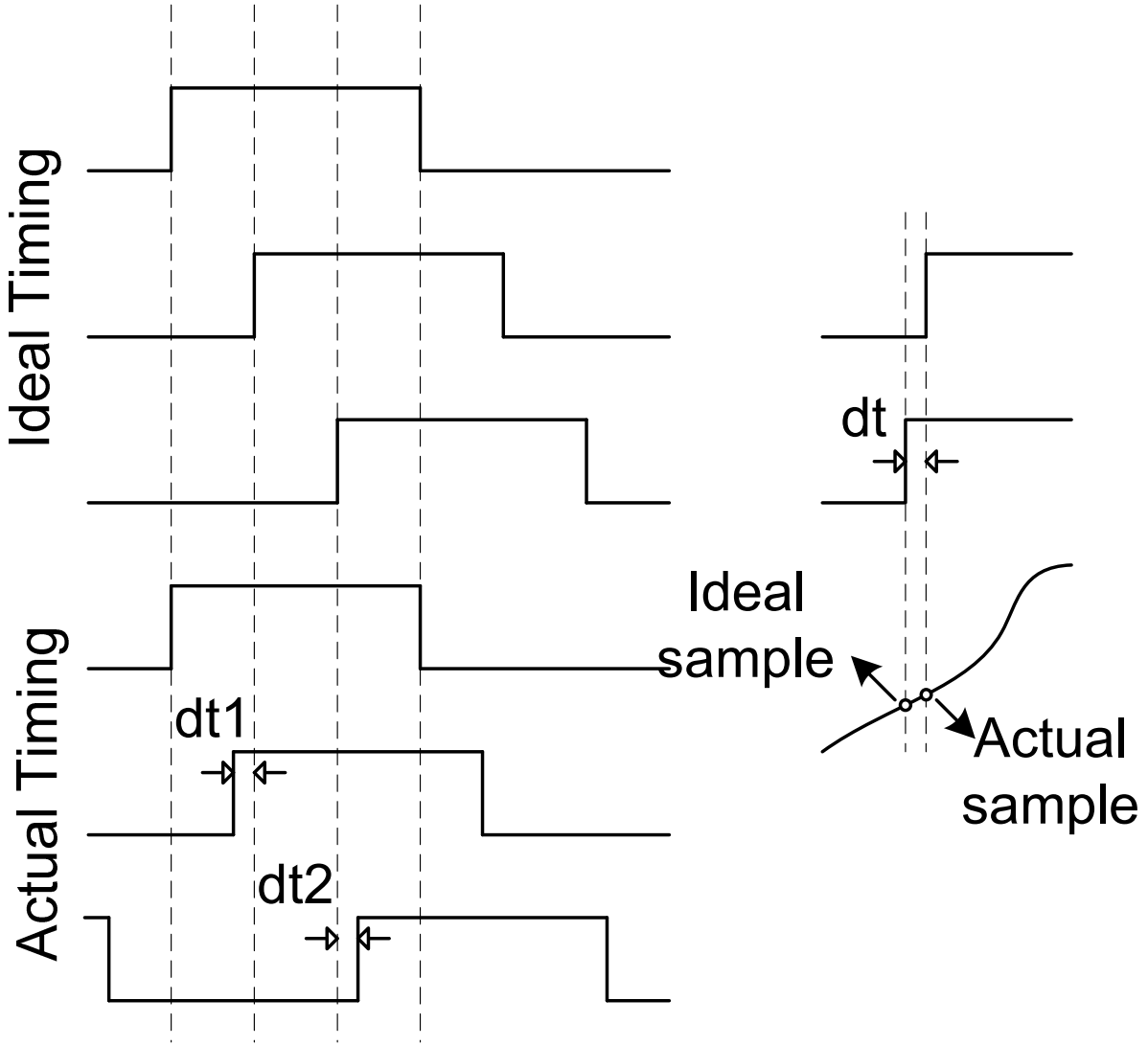
- Creates nonuniform sampling
- Error is max. when the input slope is max, thus frequency dependent
- Linear input amplitude dependency

- Noise peaks are at the same frequencies as gain offset
- Noise peaks at frequencies, f=±fin+k*Fs/M
  - fin=input frequency
  - M=# of interleaved ADCs
  - Fs=sample frequency
  - k=1, 2, 3, … M-1

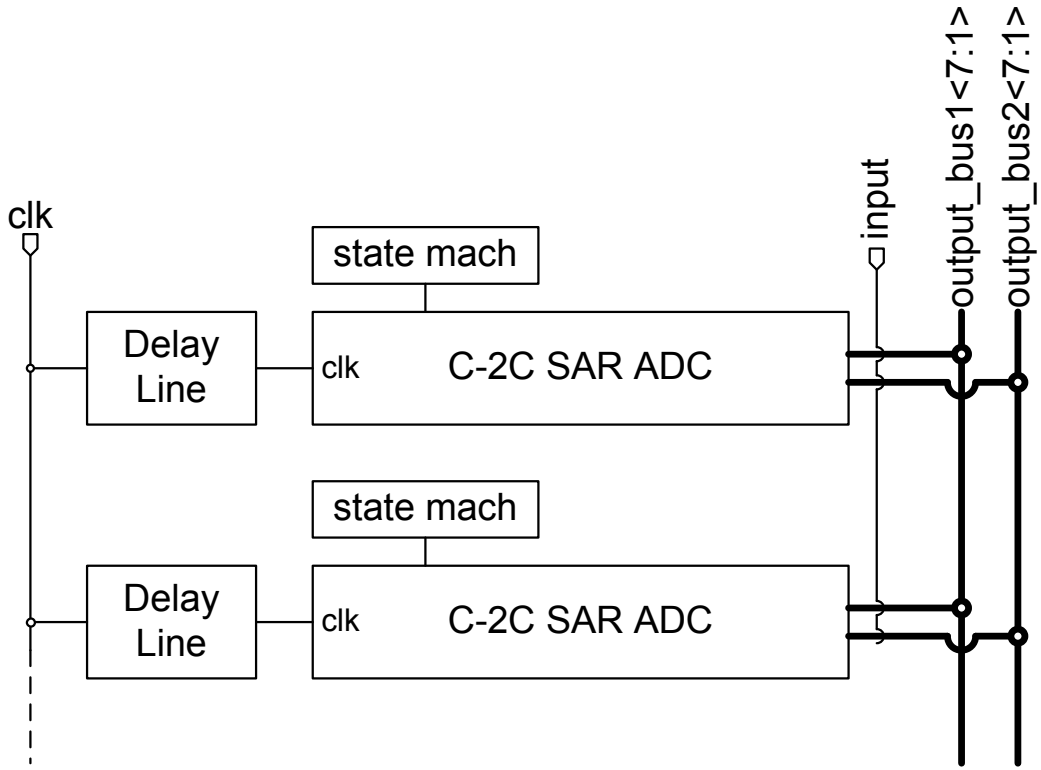
Timing Mismatch Problem



CALIBRATIONS

: Timing Calibration-1

- **This has to be done, after the gain and the offset calibration**
- **Take the outputs of the two consecutive ADCs**
- **Take the difference between the samples**
- **Take the standard deviation of the difference after adequate number of samples are collected**



2b. Limitations of ADC Calibration Techniques

- Calibration techniques can not cancel:
  - Random effects (thermal noise, jitter)
  - Quantization noise (an 8 bit ADC can not become 9 bit after calibration)
  - Fast events (spikes, metastability)

2c. Classification of ADC Calibration Techniques (1)

- By the domain of the correction:
  - Analog calibration techniques
    - Adjust reference voltages
    - Adjust components (capacitors, resistors)
    - Dynamic matching techniques
  - Digital calibration techniques
    - No adjustment is performed on the analog circuitry
    - Some analog calibration source is always needed
  - (By the nature of the problem any calibration technique is a mixed-mode circuit)

2c. Classification of ADC Calibration Techniques (2)

- By the time the correction is performed:
  - Background calibration techniques
    - Calibration circuits run in parallel and not interfering with the normal functioning of the ADC
  - Off-line calibration techniques
    - Require a specially allocated training mode
    - Offline calibration can be performed
      - At fabrication (expensive, done at testing time)
      - At power-up
      - Periodically (but it incurs inactive times)

End Lecture 12

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