Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 11- Synthesis, and design..

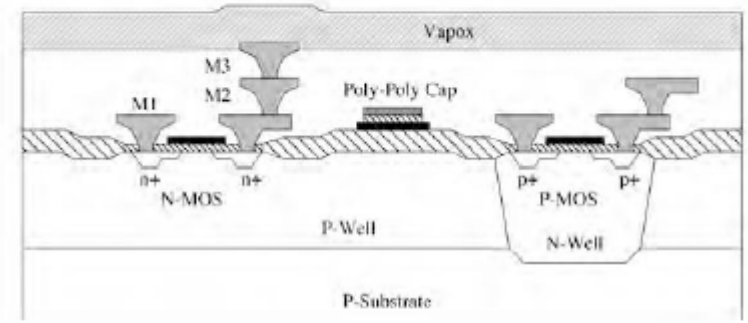
Over Sampling ADCs

Example of 1 loop design – time continuous
Stability of higher loops
Switch C building blocks
Synthesis Switch C
Time continuous - design

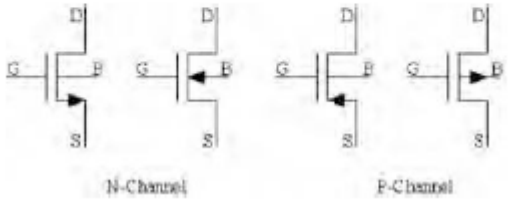
www.gigalogchip.com

Review-- transistor/process view

CMOS technology



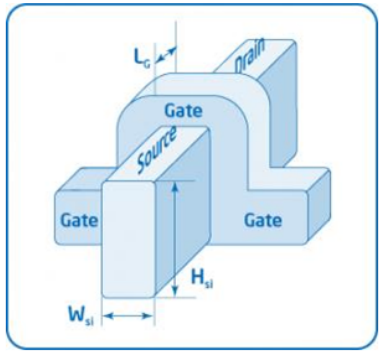
Symbols of the MOS transistors



Intel's 22nm Process. Atom, ARM, Apple

by Paul McLellan
Published on 05-05-2011 06:52 AM

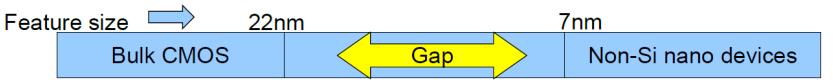
20 Comments



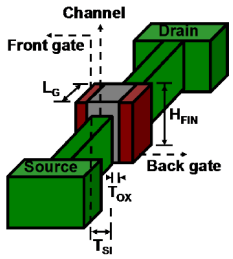
Intel had a big press event yesterday at which they announced details of their 22nm process. In a change from their current processes, it goes with a vertical gate. In fact 3 gates which gives them much better control of leakage through transistors that are switched off, along with more transmission through the on transistors. They claim to get 37% better performance and 50% power reduction compared to 32nm. Although vertical transistors have been talked about for nearly a decade, Intel's tri-gate is the first time anyone has brought them into volume production.

One speculation is whether the performance of Atom at 22nm hits a better power/performance than ARM does at 28nm in TSMC and other foundries. Of course the ATOM vs ARM battle isn't really just about technical specs but rather about ecosystems and partners. The mobile industry in particular are unlikely to suddenly switch everything to Atom for a small increase in battery life because it would be very expensive and risky.

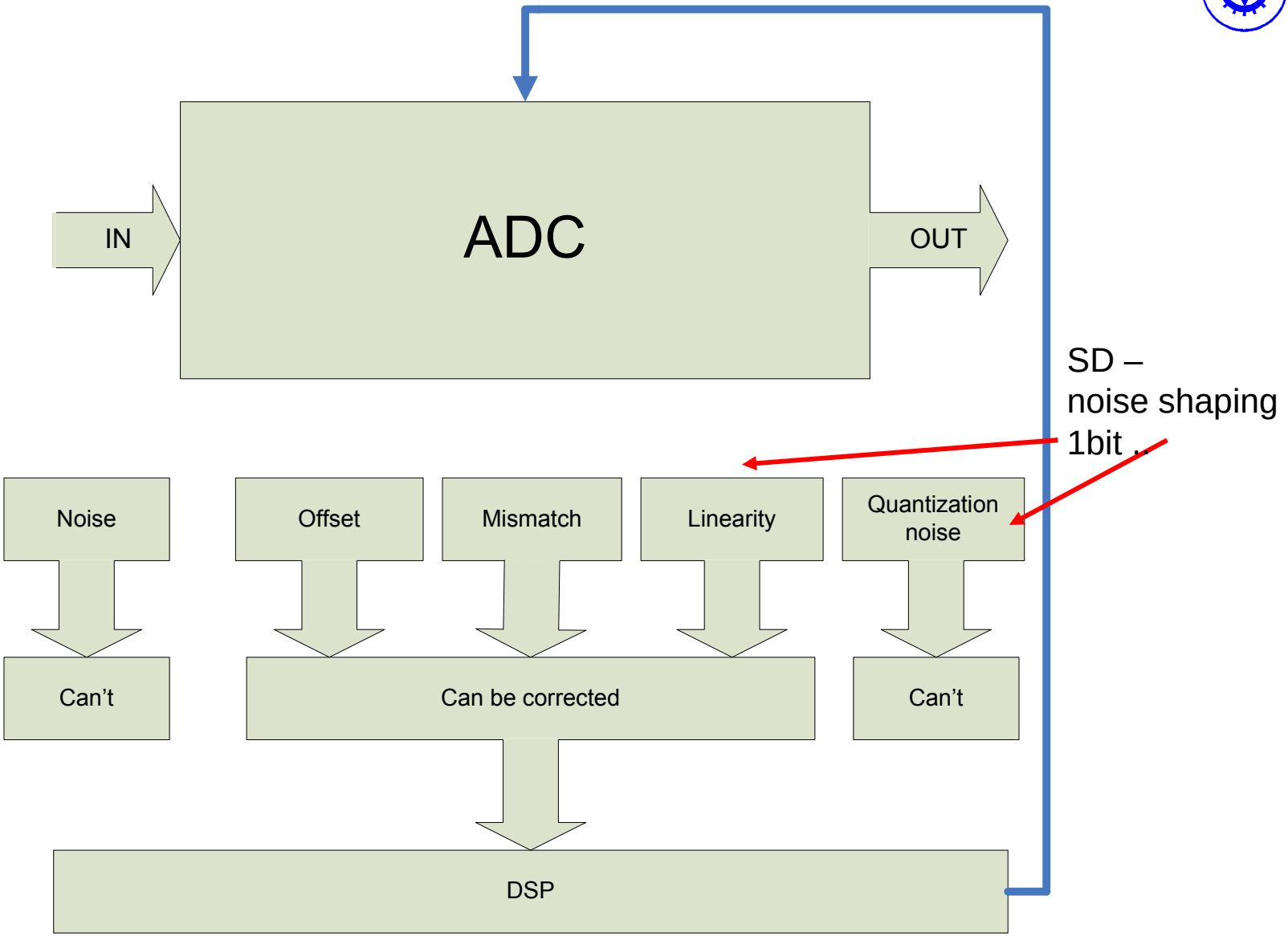
Why FinFETs?



- FinFETs expected to continue transistor scaling to 7nm
  - FinFET fabrication compatible with CMOS process
  - FinFETs address scaling challenges faced by bulk CMOS
    - Better channel control with double gates ➔ reduced short-channel effects
    - Improved subthreshold slope
    - Better Ion/Ioff
  - Different styles
    - Shorted-gate (SG)
    - Independent-gate (IG)
    - Asymmetric-workfunction SG (ASG)



Potential calibrations:



CT Sigma DELTA
1st Order Loop as an example

Objective : To be aware of the many issues of CT design

From Lect. 10, remember:

$$SNR_{max} = 10\log\left[\frac{3}{2}(2^{B}-1)^{2}\frac{(2L+1)M^{2L+1}}{\pi^{2L}}\right]$$

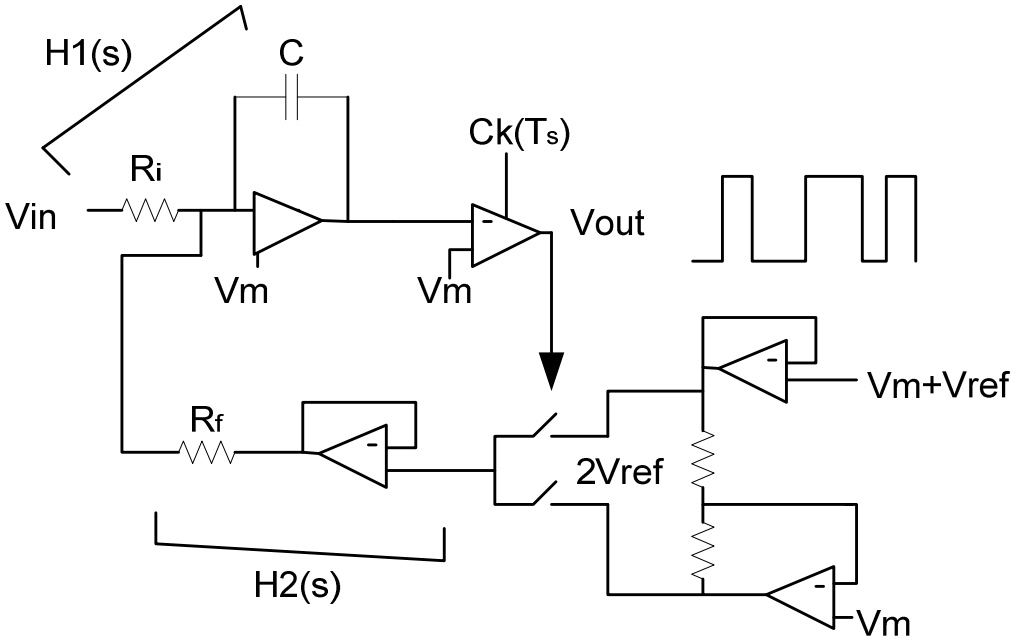
$M = \frac{f_s}{2f_B}$ = Oversampling Ratio

L = Modulator Order

B = Internal Quantizer Resolution

ADC time continue – example 1

Development of SD ADC



Design ”spec”

For 84dB SNR

For input pk signal 500 mV

For BW=8 KHz

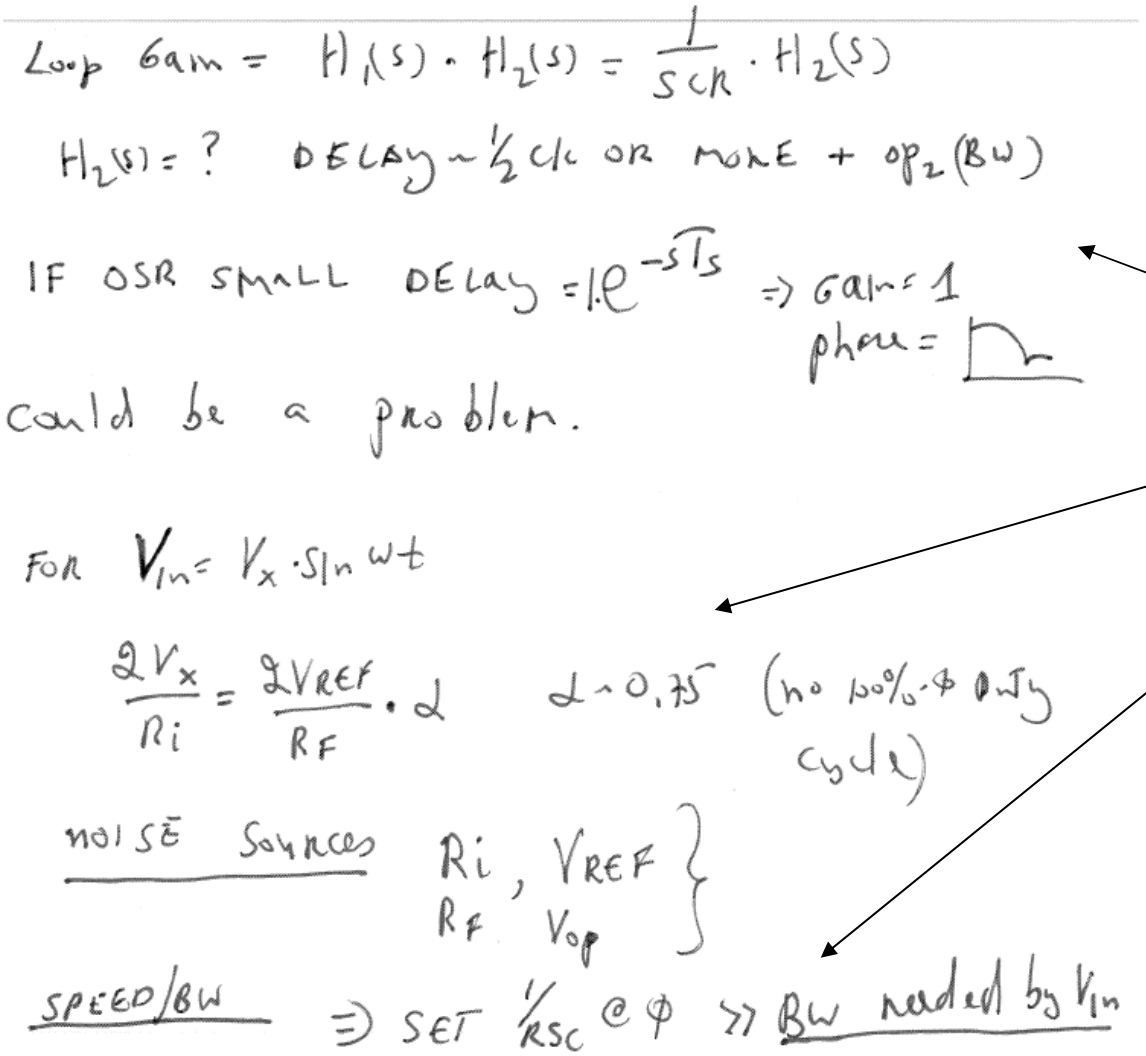
STEP 1 : SNR: Setting Clock Speed: (OSR) and inventory:

Let choose: One loop – Perfect linearity
1 bit DAC Vref/Rf
1 Comparator 200ua – 3ma (very fast)
1 Integrator 100uA – 2ma (very fast)
References and clock signals 500uA
Needed: DSP (Decimation filters)

SNR:
87db-6db(1bit) /9db/oct=9 octaves !

Clock: 16KHz x 512 = 8.192MHz

ADC time continue – example 1



STEP 2

Stability issue

Fscale setting

Needed Integrator BW

ADC time continue – example 1

STEP 3 : Noise sources finding Rin and C

For 84dB SNR (qunatization + Thermal Noises) linearities=0)
For input pk signal 500 mV
For BW=8 KHz – phone: codec voice applications..

Input resistor should be as low as possible
but also as large as possible (lower I dac, Low C,)

The maximum resistor is set by:
Calculation of thermal noise to achieve 12dB higher SNR (96dB)
(i.e., 10db added to 84dB will drop total SNR by ~ 1dB to 83dB)

Calculate Noise due to Rf and Ri

For signal input of
400mV: 96dB down from (1:65,536) = 6.1035uV (in 8 KHz)
Per sqrtHz=> 6.1035/89.44 ~ 68 nV
For each of the 2 resistors: /1.414 (Rdac=Rin) = 48 nV/sqrtHz (room T)
If 1K has 4.09nV/sqrtHz

STEP 3

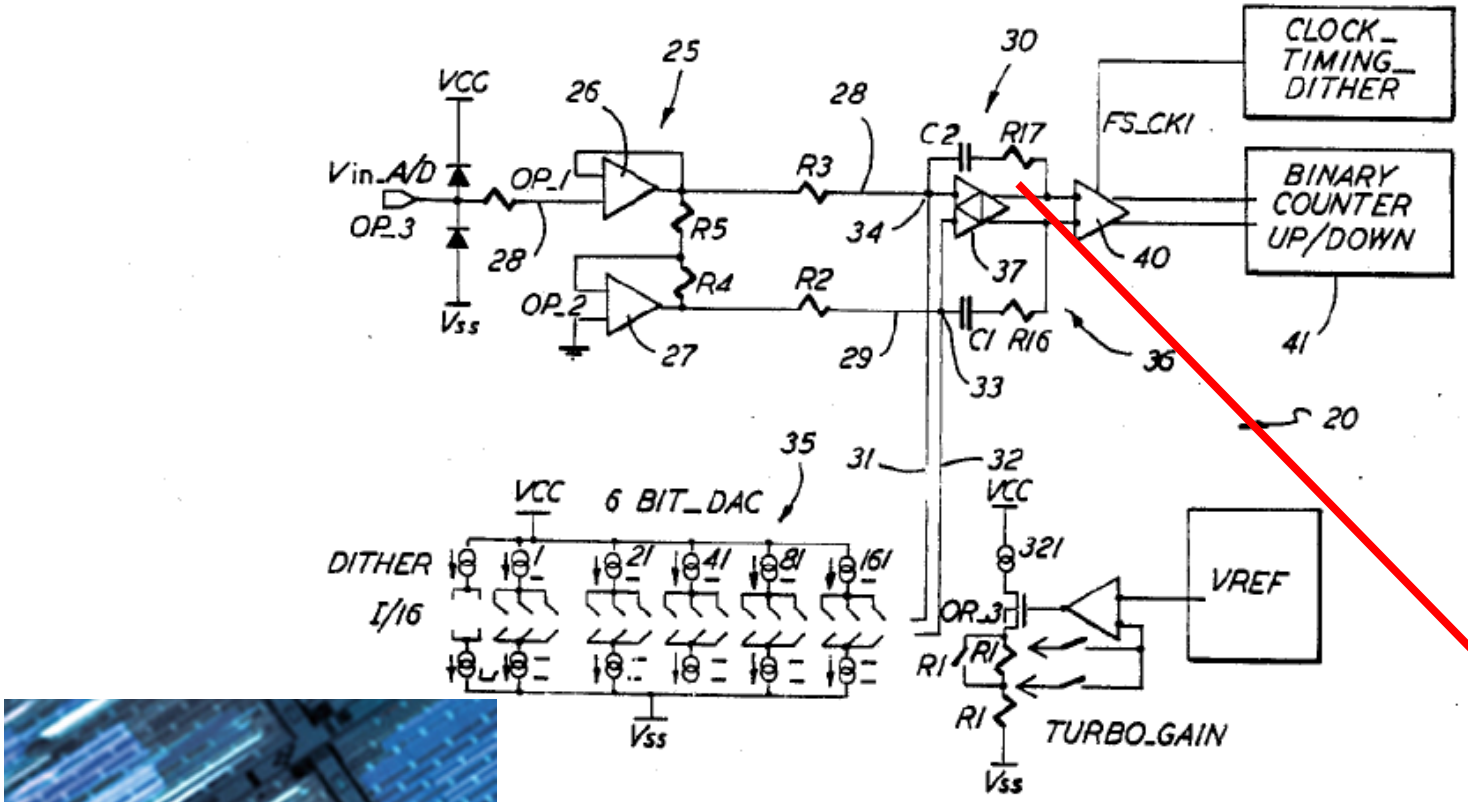
Find R and C

R= 137 K ohm (will produce ~48nV/sqrtHz : 4.09 xsqrt(137))
I dac = 0.5/137000 ~ 3.6uA (forgot to take temp in 4kT..)

Finding C:

For 8 KHz setting the op BW it ~2.5 time 8 KHz = **need 68pF !**

ADC time continue – more options multi loop..

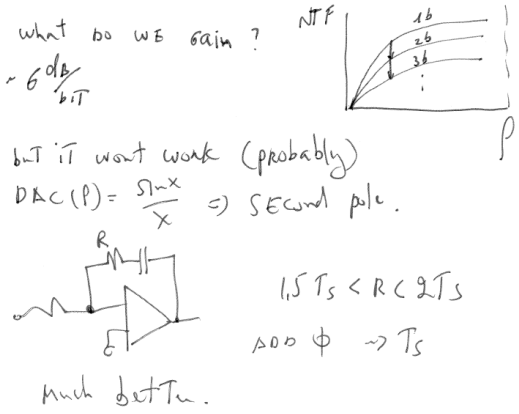


Key: add 0 to the loop

[54] **TIME CONTINUOUS, DIFFERENTIAL ANALOG-TO-DIGITAL CONVERTER**

[75] Inventor: **Miki Z. Moyal, Austin, Tex.**

[73] Assignee: **Advanced Micro Devices, Inc., Sunnyvale, Calif.**



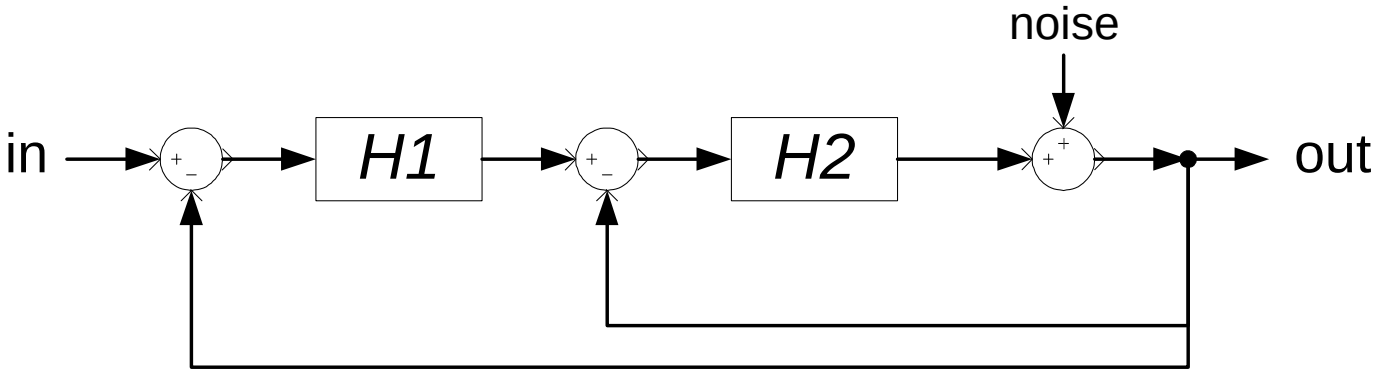
Note: Beyond this lecture but. Remember..

ADD made of 1 loop can be sensitive to “tone spikes”
(dithering is needed)- it take long fix sequence..
(nice feature: SD “like” noisy environment..)

Slew rate and amplifier performance should be evaluated

Feedback C (add R to compensate for loop DAC ~integrator
And simulate best values).

Stability of higher order loop – 2nd order..

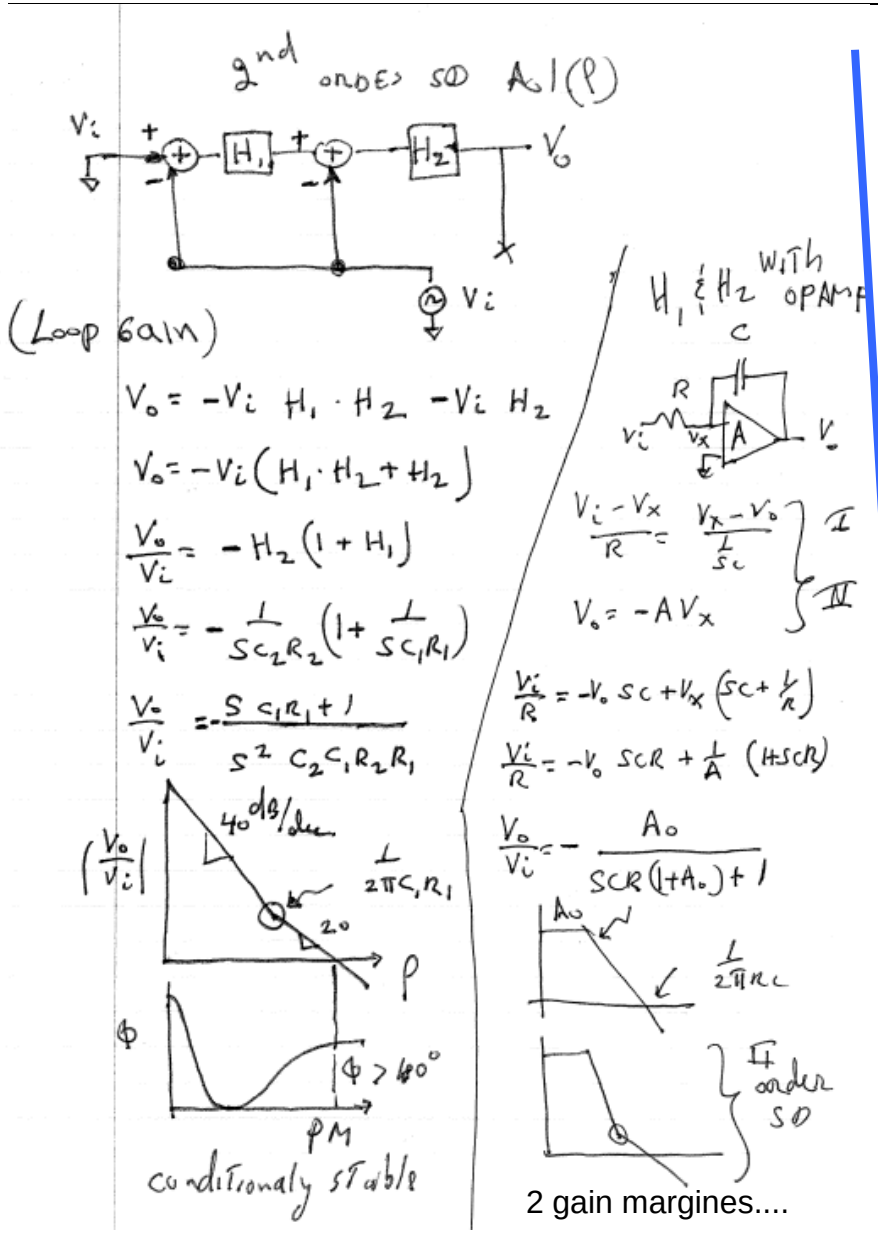


2 loops: Were to open the loop ?

$$(noise=0): \quad \frac{out}{in} = \frac{H_1 H_2}{1 + H_2 + H_1 H_2}$$

$$(in=0): \quad \frac{out}{noise} = \frac{1}{1 + H_2 + H_1 H_2}$$

Stability of higher order loop – 2nd order..



2 gain margines....

TRANSFER FUNCTION RC POSITIONING

Pole 1=1MHz pole2=2MHz

first loop integrator second loop integrator

integaor values : $C_1 := 31.4\cdot10^{-12}$ $R_1 := 5\cdot10^{3}$ $C_2 := 15.7\cdot10^{-12}$ $R_2 := 5\cdot10^{3}$

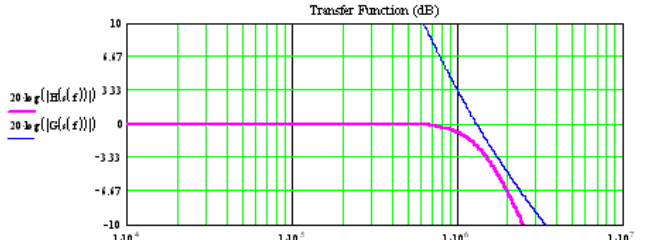
1st integrator $f_1 := \frac{1}{2\cdot\pi\cdot(R_1\cdot C_1)}$ $f_1 = 1.014\times10^{4}$

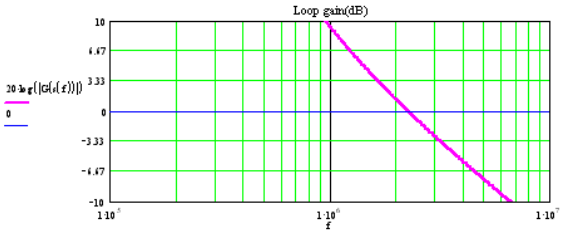
2nd integrator $f_2 := \frac{1}{2\cdot\pi\cdot(R_2\cdot C_2)}$ $f_2 = 2.027\times10^{4}$

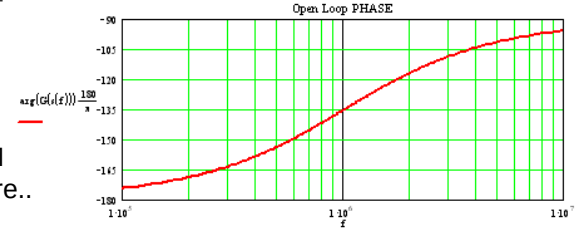
$H22(s) := 1\frac{1}{s\cdot(R_2\cdot C_2)}$ $H11(s) := 1\frac{1}{s\cdot(R_1\cdot C_1)}$

T.F $\frac{((H11(s)\cdot H22(s)))}{1+(H22(s))+((H11(s)\cdot H22(s)))}$

$f := 100, 2000..10000000$ $s(f) := 2\cdot\pi\cdot f\cdot i$







Key: PM from here..

first loop integrator second loop integrator

integaor values : $C_1 := 31.4 \cdot 10^{-12}$ $R_1 := 5 \cdot 10^3$ $C_2 := 15.7 \cdot 10^{-12}$ $R_2 := 5 \cdot 10^3$

1st integrator $f_1 := \frac{1}{2 \cdot \pi (R_1 \cdot C_1)}$ $f_1 = 1.014 \times 10^6$

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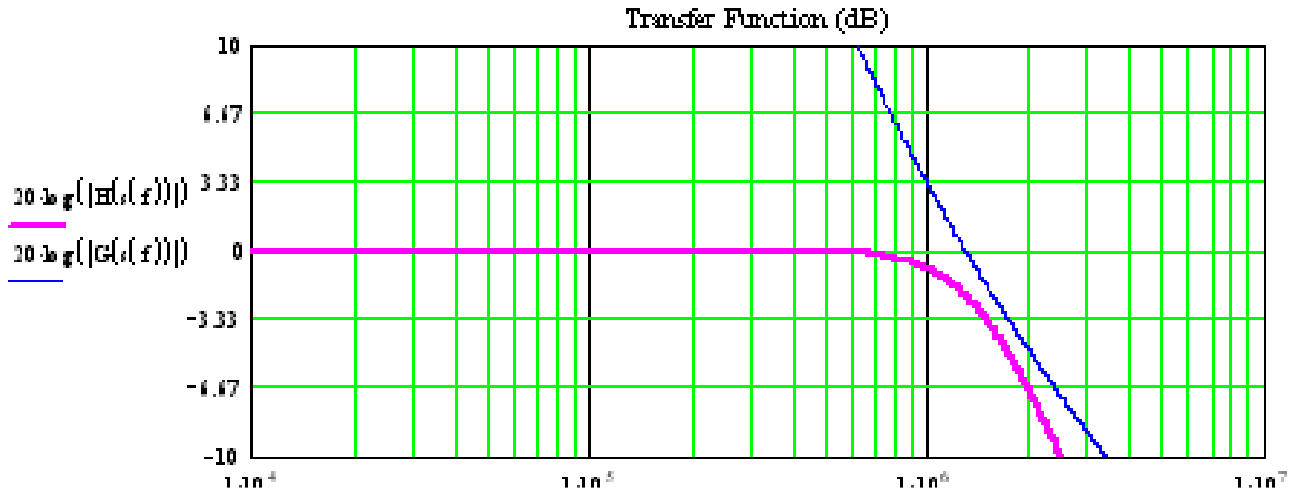
T.F $\frac{((H11(s) \cdot H22(s)))}{1 + (H22(s)) + ((H11(s) \cdot H22(s)))}$

$f := 100, 2000 .. 10000000$ $s(f) := 2 \cdot \pi \cdot f \cdot i$



Example: Stability " Wrong positioning"

Pole1~ 1MHz
Pole2~1MHz

first loop integrator second loop integrator

integaor values : $C_1 := 31.4\cdot10^{-12}$ $R_1 := 5\cdot10^{3}$ $C_2 := 31.40\cdot10^{-12}$ $R_2 := 5\cdot10^{3}$

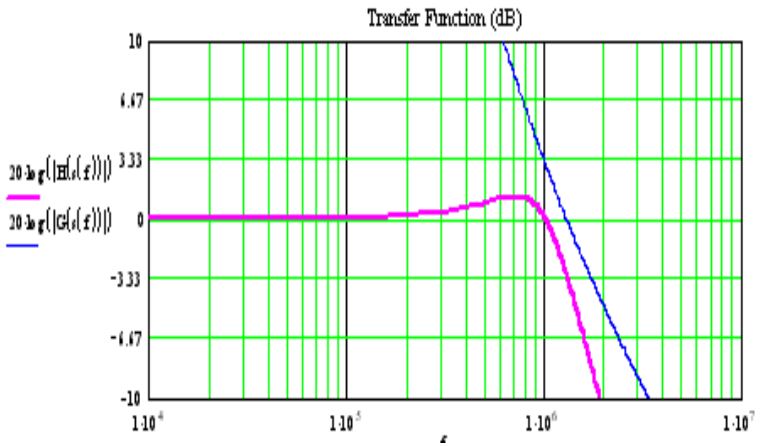
1st integrator $f_1 := \frac{1}{2\cdot\pi\cdot(R_1\cdot C_1)}$ $f_1 = 1.014\times10^{6}$

2nd integrator $f_2 := \frac{1}{2\cdot\pi\cdot(R_2\cdot C_2)}$ $f_2 = 1.014\times10^{6}$

$H22(s) := 1\frac{1}{s\cdot(R_2\cdot C_2)}$ $H11(s) := 1\frac{1}{s\cdot(R_1\cdot C_1)}$

T.F $\frac{((H11(s)\cdot H22(s)))}{1+(H22(s))+((H11(s)\cdot H22(s)))}$

$f := 100, 2000..10000000$ $s(f) := 2\cdot\pi\cdot f\cdot i$



Pole1~ 1MHz
Pole2~ 0.2MHz

first loop integrator second loop integrator

integaor values : $C_1 := 31.4\cdot10^{-12}$ $R_1 := 5\cdot10^{3}$ $C_2 := 157\cdot10^{-12}$ $R_2 := 5\cdot10^{3}$

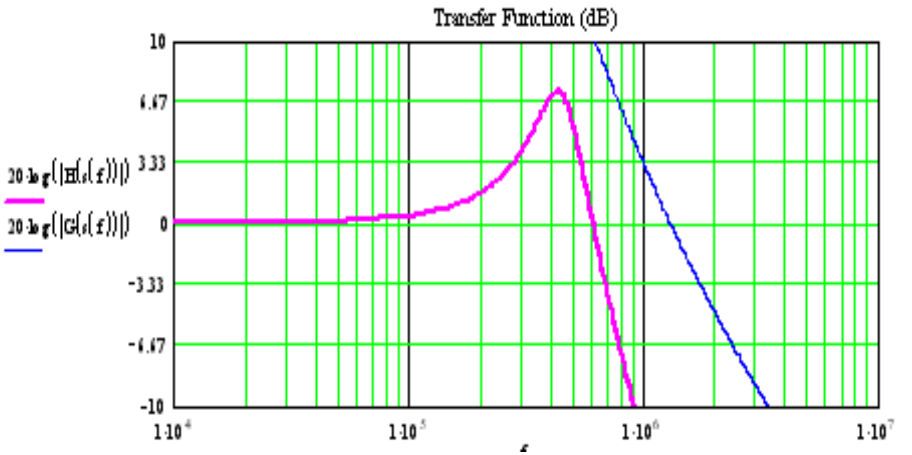
1st integrator $f_1 := \frac{1}{2\cdot\pi\cdot(R_1\cdot C_1)}$ $f_1 = 1.014\times10^{6}$

2nd integrator $f_2 := \frac{1}{2\cdot\pi\cdot(R_2\cdot C_2)}$ $f_2 = 2.027\times10^{5}$

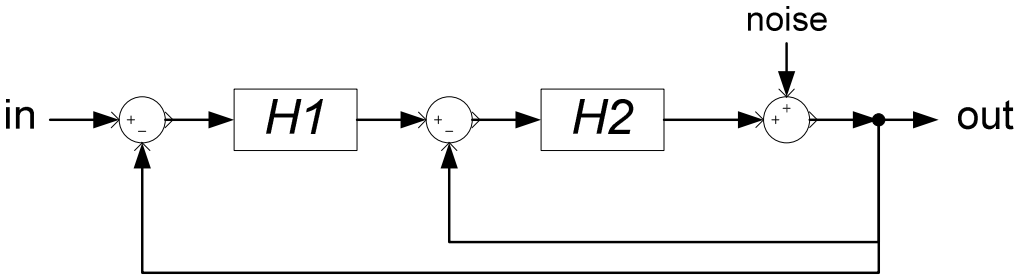
$H22(s) := 1\frac{1}{s\cdot(R_2\cdot C_2)}$ $H11(s) := 1\frac{1}{s\cdot(R_1\cdot C_1)}$

T.F $\frac{((H11(s)\cdot H22(s)))}{1+(H22(s))+((H11(s)\cdot H22(s)))}$

$f := 100, 2000..10000000$ $s(f) := 2\cdot\pi\cdot f\cdot i$



Example: Stability noe in z domain..



- Each H is an integrator with delay:
- In Ideal Integrator α=1
- Transfer functions are:

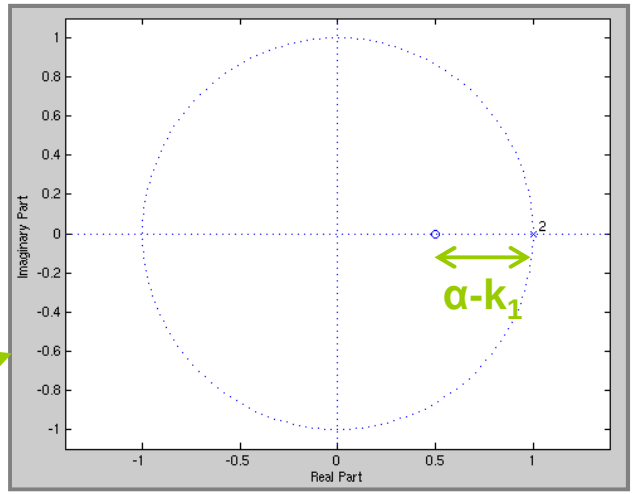
$$(noise=0):\ \frac{out}{in}=\frac{H_1H_2}{1+H_2+H_1H_2}$$

≠-1

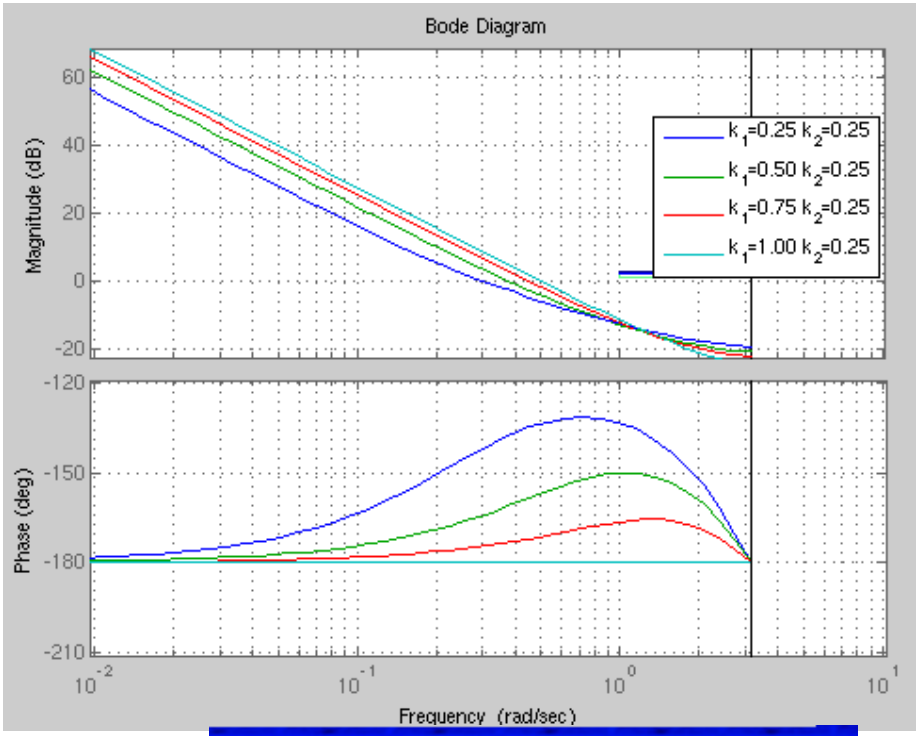
$$(in=0):\ \frac{out}{noise}=\frac{1}{1+H_2+H_1H_2}$$

$$Hol=H_2+H_1H_2=k_2\cdot\frac{Z-(\alpha-k_1)}{(Z-\alpha)^2}$$

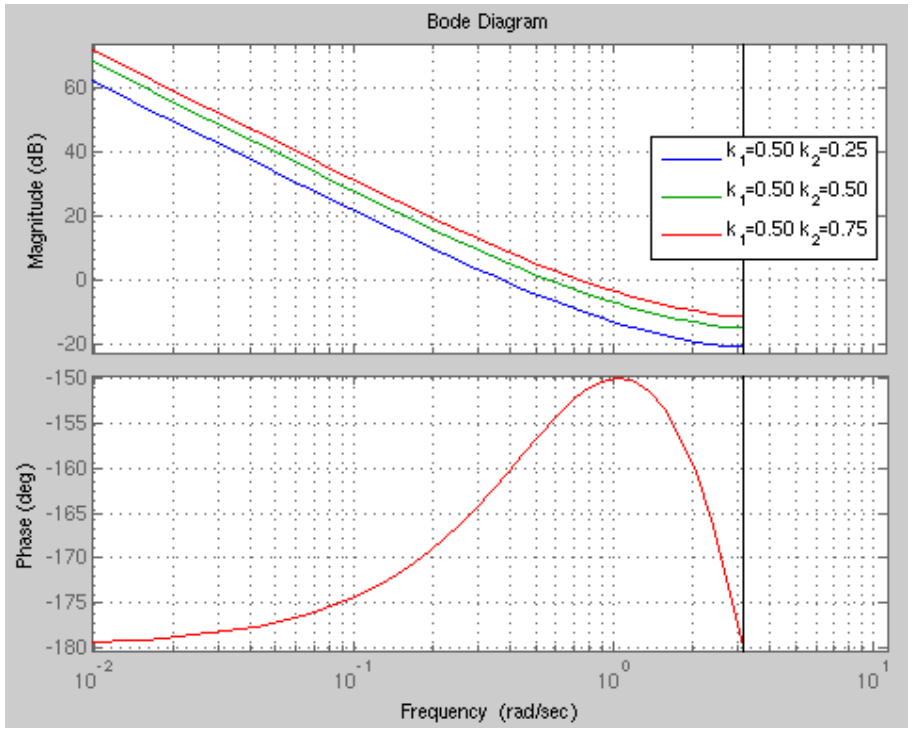
≠-1



- Constant k_2 varying k_1
- Smaller k_1 increases phase margin noticeably



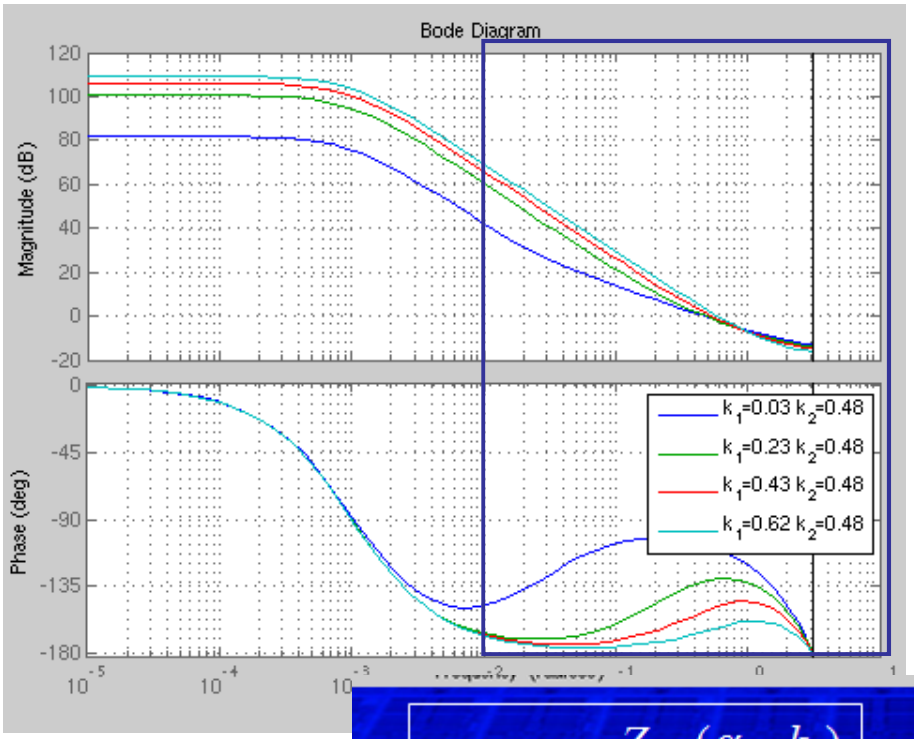
- Constant k_1 varying k_2
- The phase is constant
- Higher k_2 increases phase margin noticeably



$$Hol = k_2 \cdot \frac{Z-(\alpha-k_1)}{(Z-\alpha)^2}$$

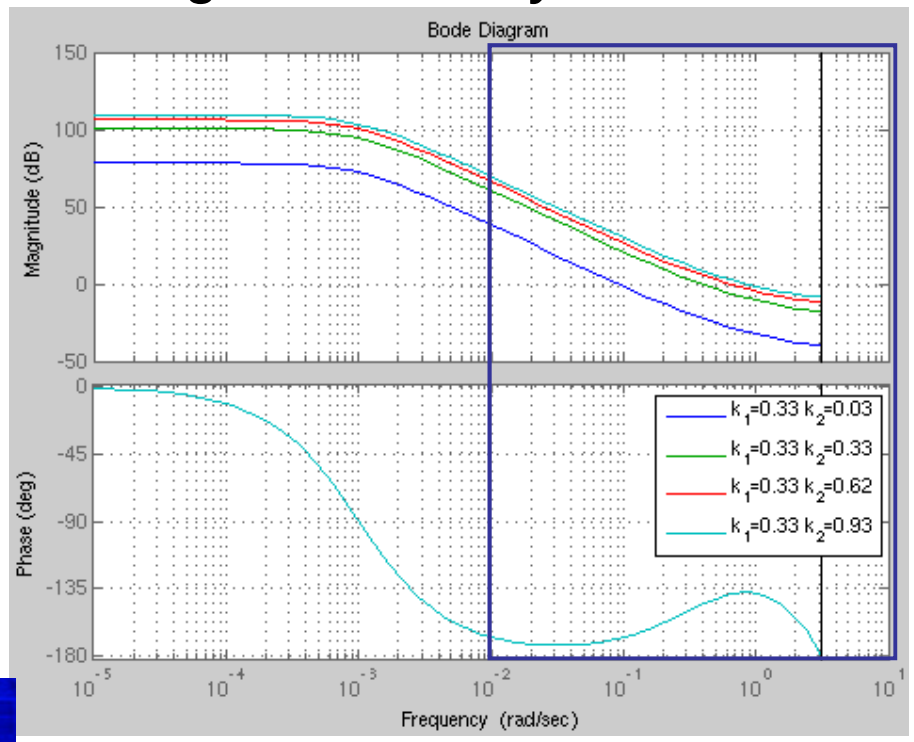
Stability Vs. k_1, k_2 (α=1-10^{-3})

- Constant k_2 varying k_1
- Smaller k_1 increases phase margin noticeably

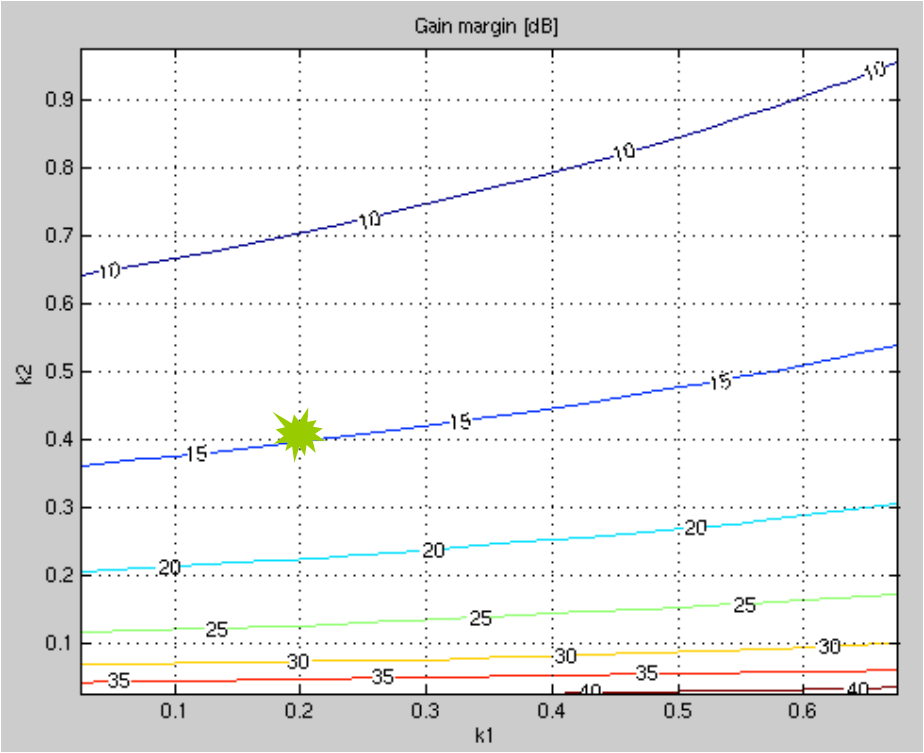


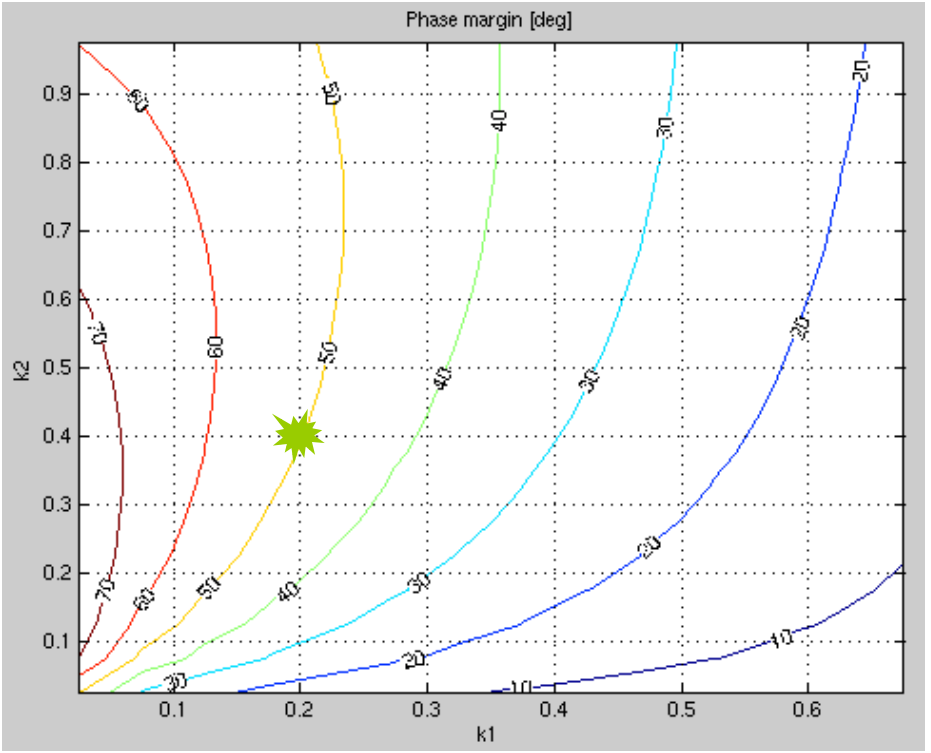
$$Hol = k_2 \cdot \frac{Z-(\alpha-k_1)}{(Z-\alpha)^2}$$

- Constant k_1 varying k_2
- The phase is constant
- Higher k_2 increases phase margin noticeably



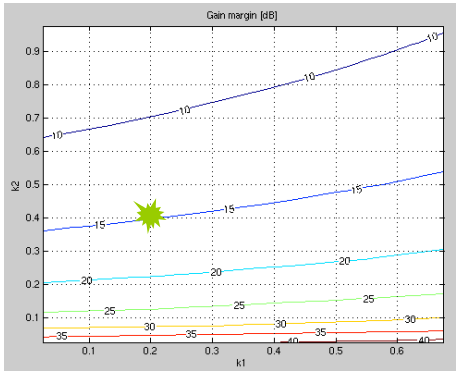
Stability Vs. k_1,k_2

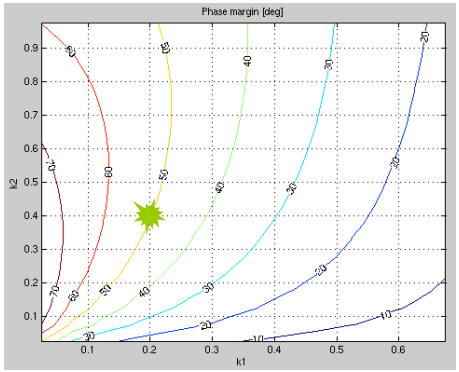


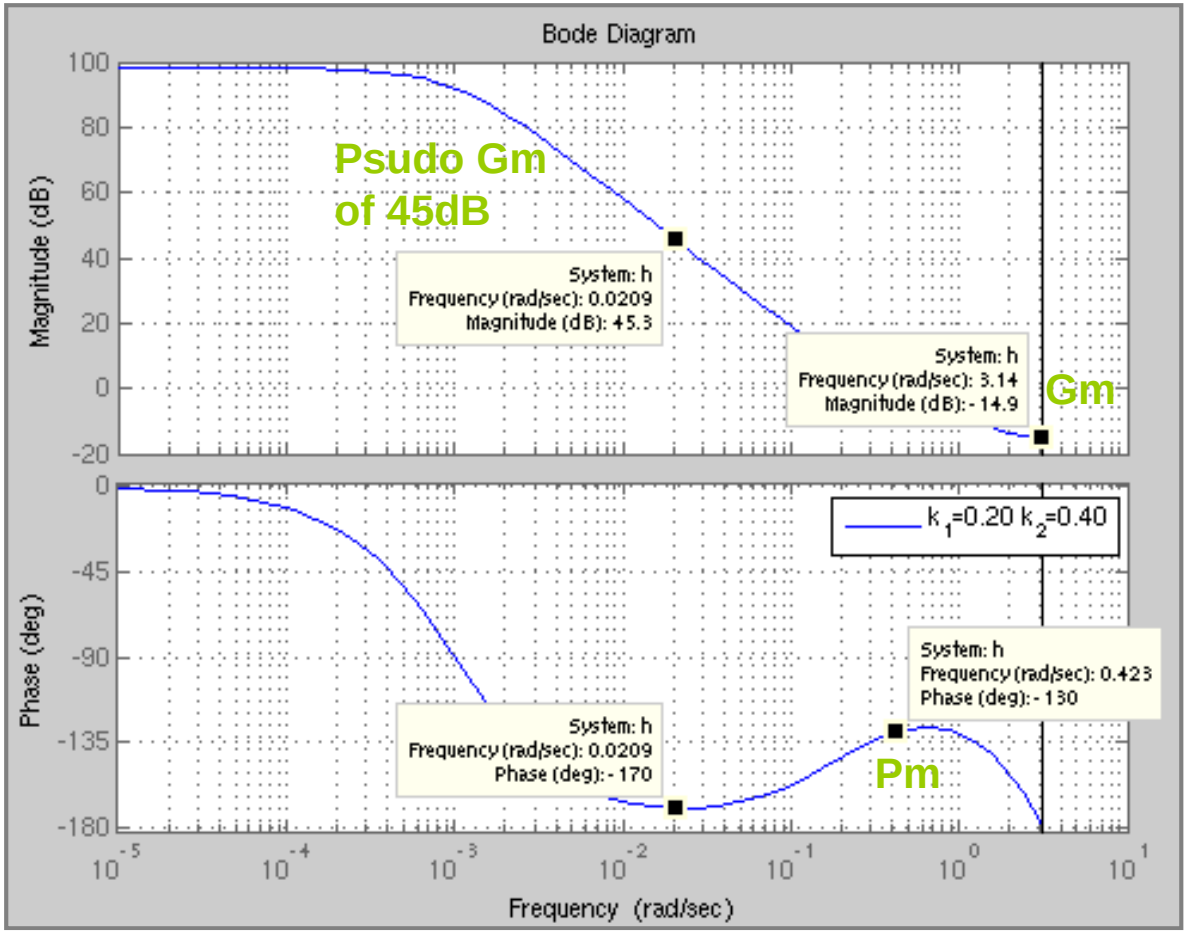


- α has neglectable affect on the Gain-margin and Phase-margin
- The gain margin is always the gain at Fs/2
- i.e. k_1=1/5 k_2=2/5 Gm=15dB Pm=50°

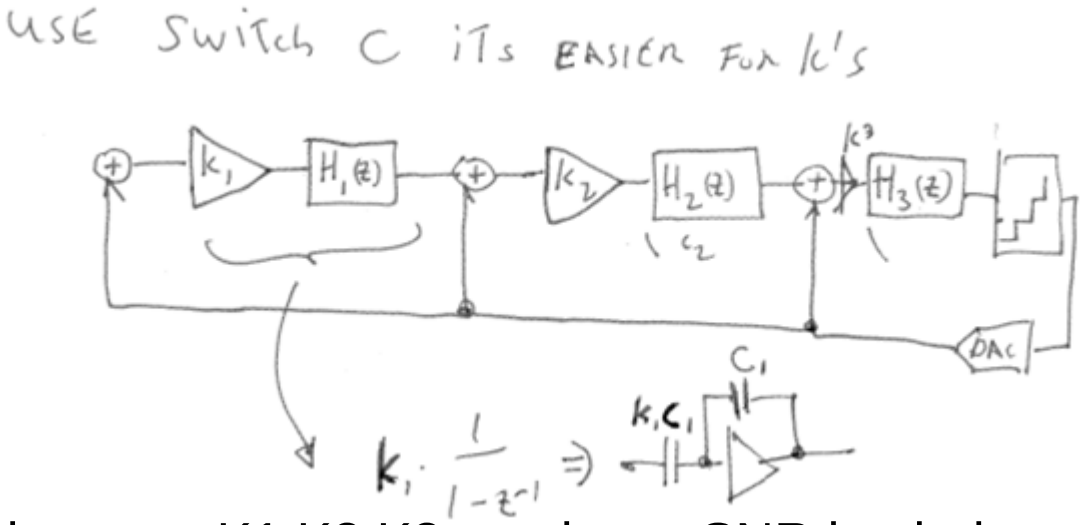
- k_1=1/5 k_2=2/5
  Gm=15dB
  Pm=50°







Stability: Introducing K1,K2,K3..Kn in the loop..



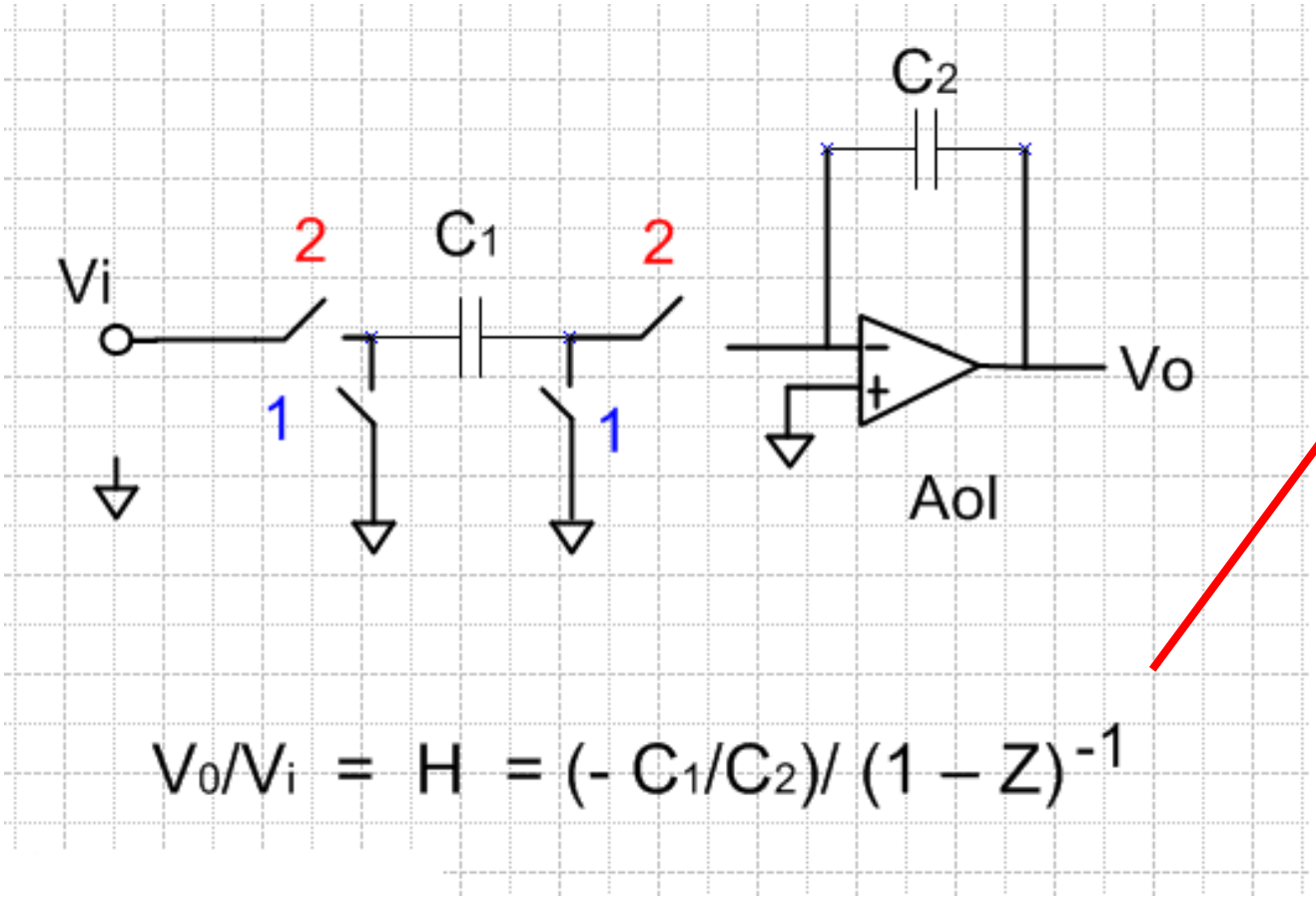
Bad news..: K1,K2,K3…reduces SNR by their product..
Good news system is stable.

Expand on lect. 10 to figure SNR:

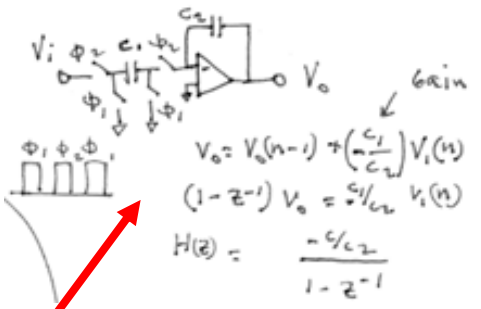
$$SNR_{pk} = \left[2^B - 1\right]^2 \cdot (2n+1)\left(\frac{R}{\pi}\right)^{2n+1} \cdot a_0 \cdot a_1 \cdot a_2 \left(\frac{3\pi}{2}\right) \cdot V$$

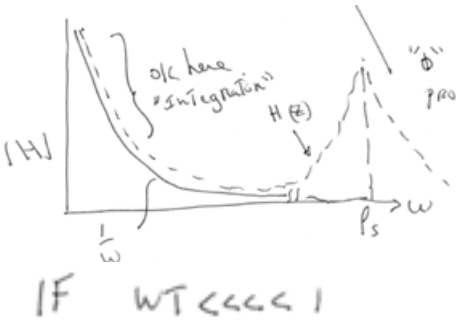
B=number of bits, R =OSR, n=loops, a0=K1..

Ideal Transfer function basic switch C:



$$V_0/V_i = H = (-C_1/C_2)/(1 - Z)^{-1}$$





Non Idealities:
With Open loop A is finite

$$V_0/V_i = H = (-C_1/C_2)L/(1 - (1 - (C_1/AC_2))Z^{-1})$$

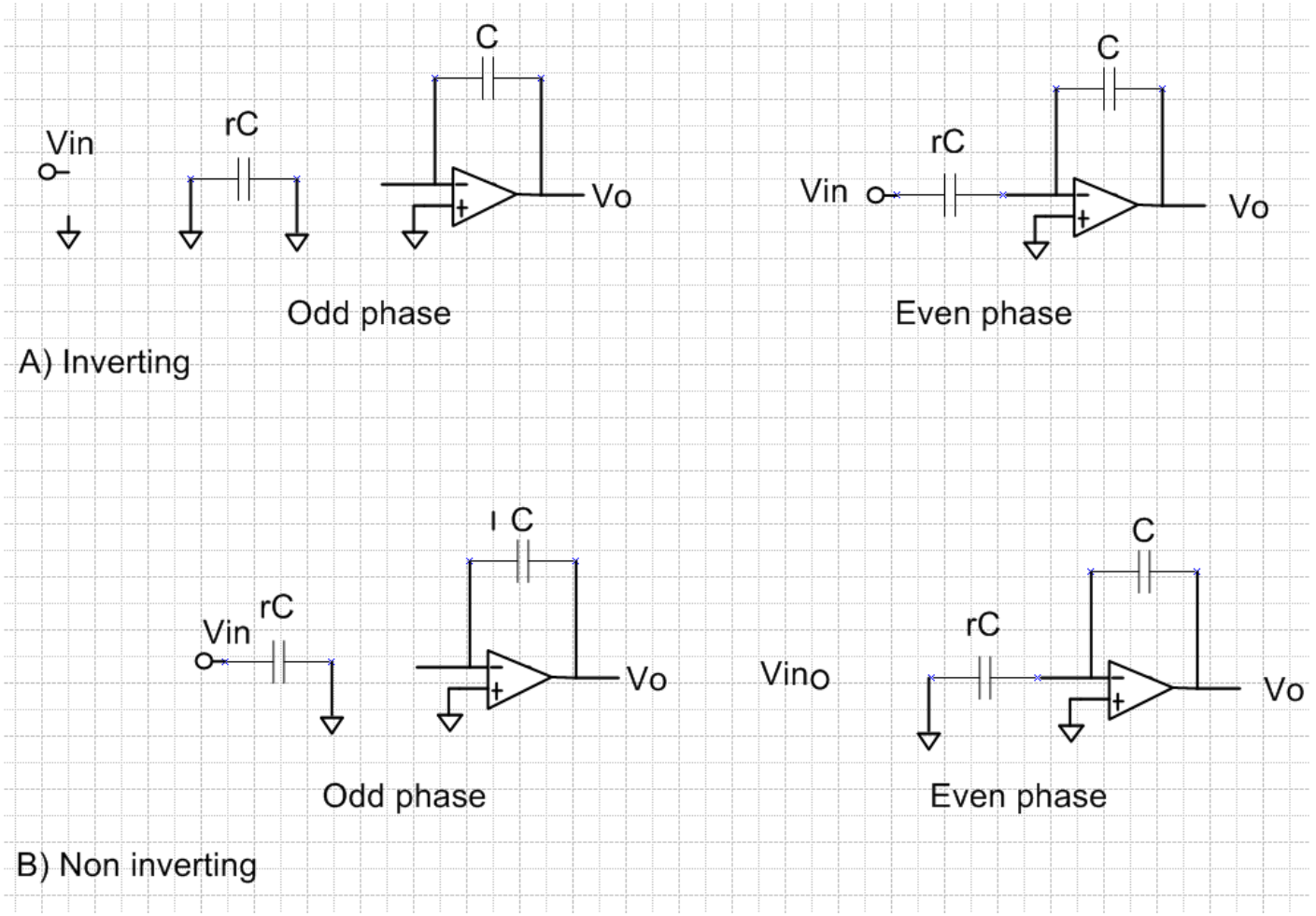
$$L = 1 - 1/A - (C_1/AC_2)$$

$R \simeq \left[\frac{C_1}{T}\right]^{-1}, C = C_2$

f(bw)= (C1/C2) / (Ts x 2pi)

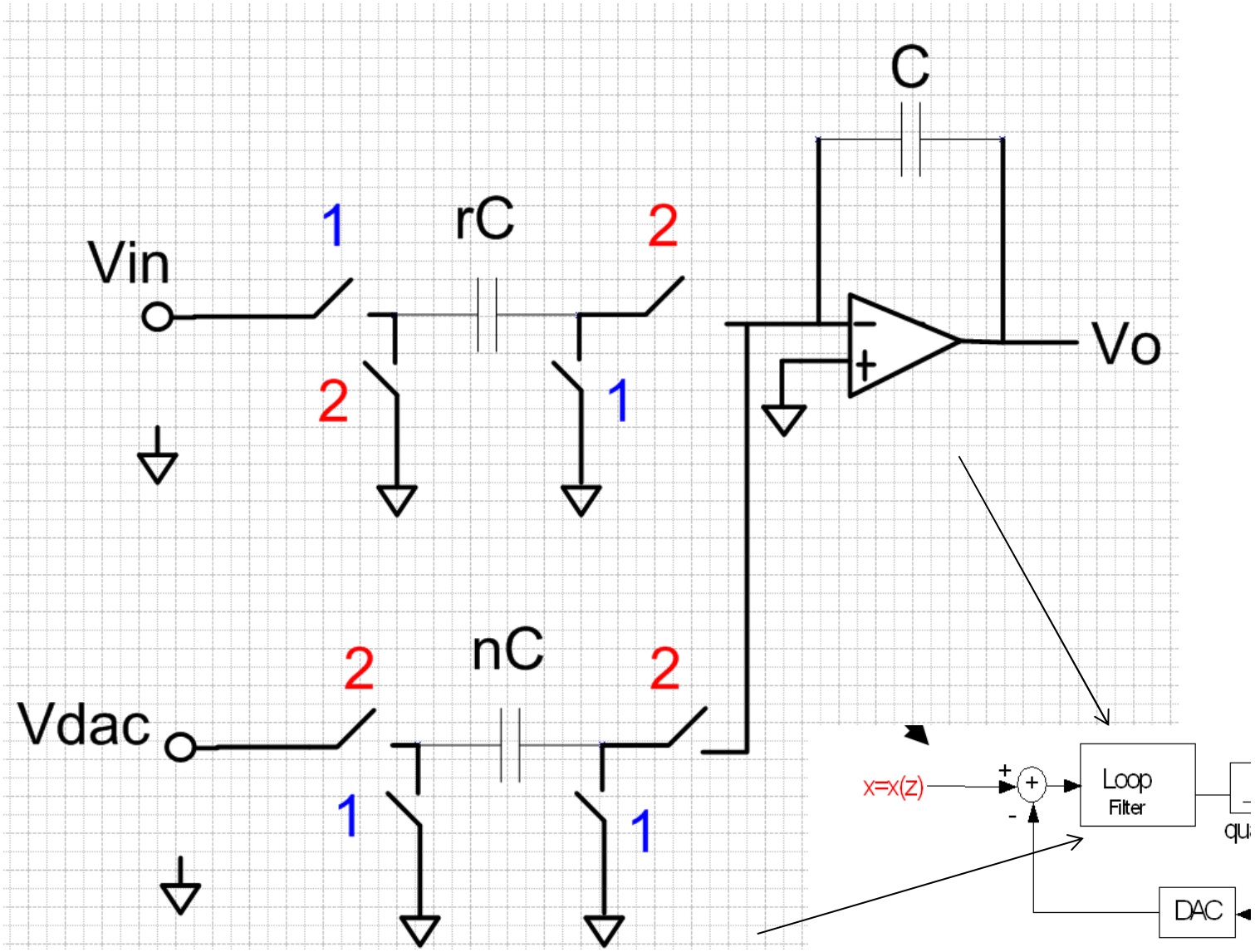
Big advantage: process indep.

SWITCH C OPTIONS: INVERTING AND NON INVERTING



KEY: in SC WE CAN SUBSTRACT BY PLACING THE PHASE TIMING
(no need for inverting amplifiers)

Building the basic switch C SD and dac

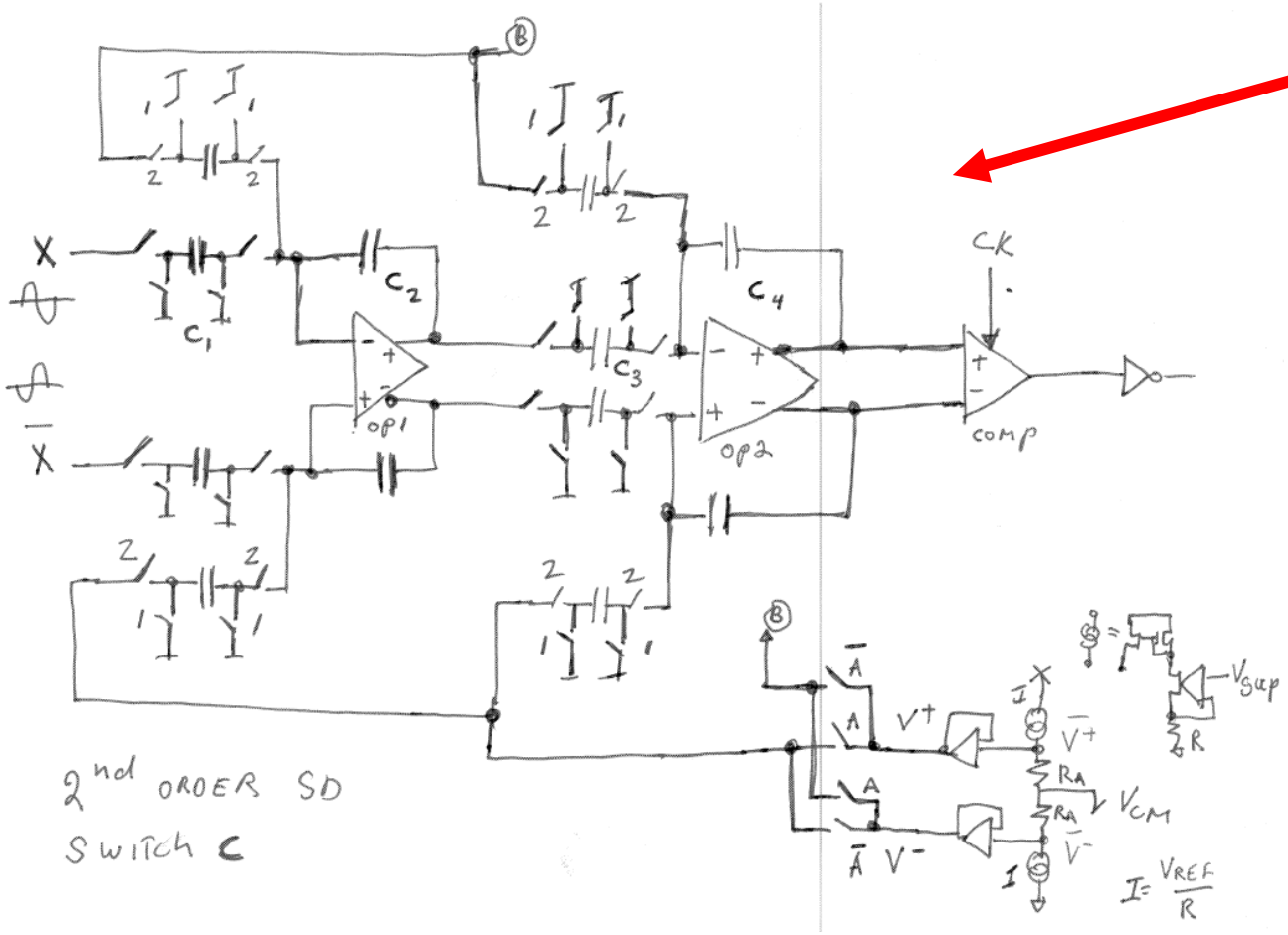


EXAMPLE:

Analysis of a Switch C Sigma Delta Second order

Analyze this second order SD
How does it works?
What is the potential SNR ? , Noise in ? max input signal BW ?

Example: Given schematic and ckt parameters

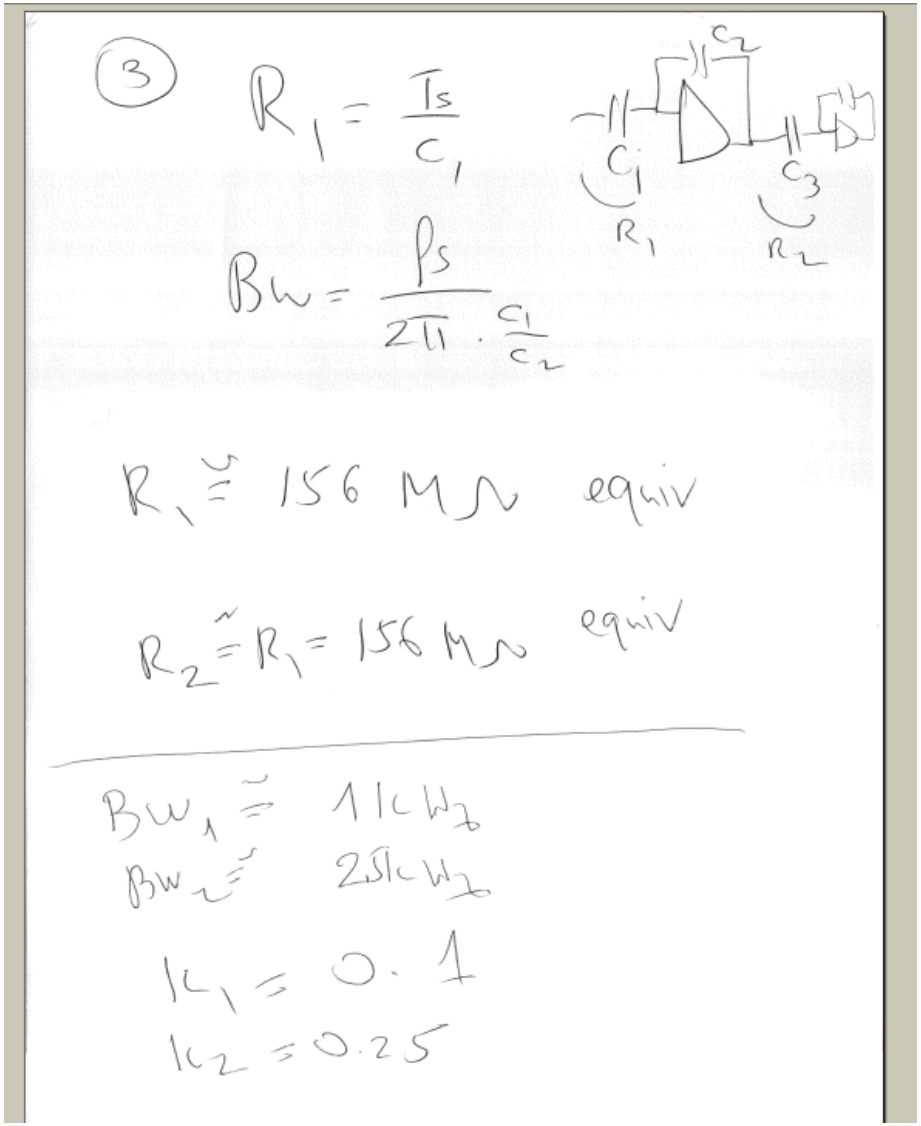


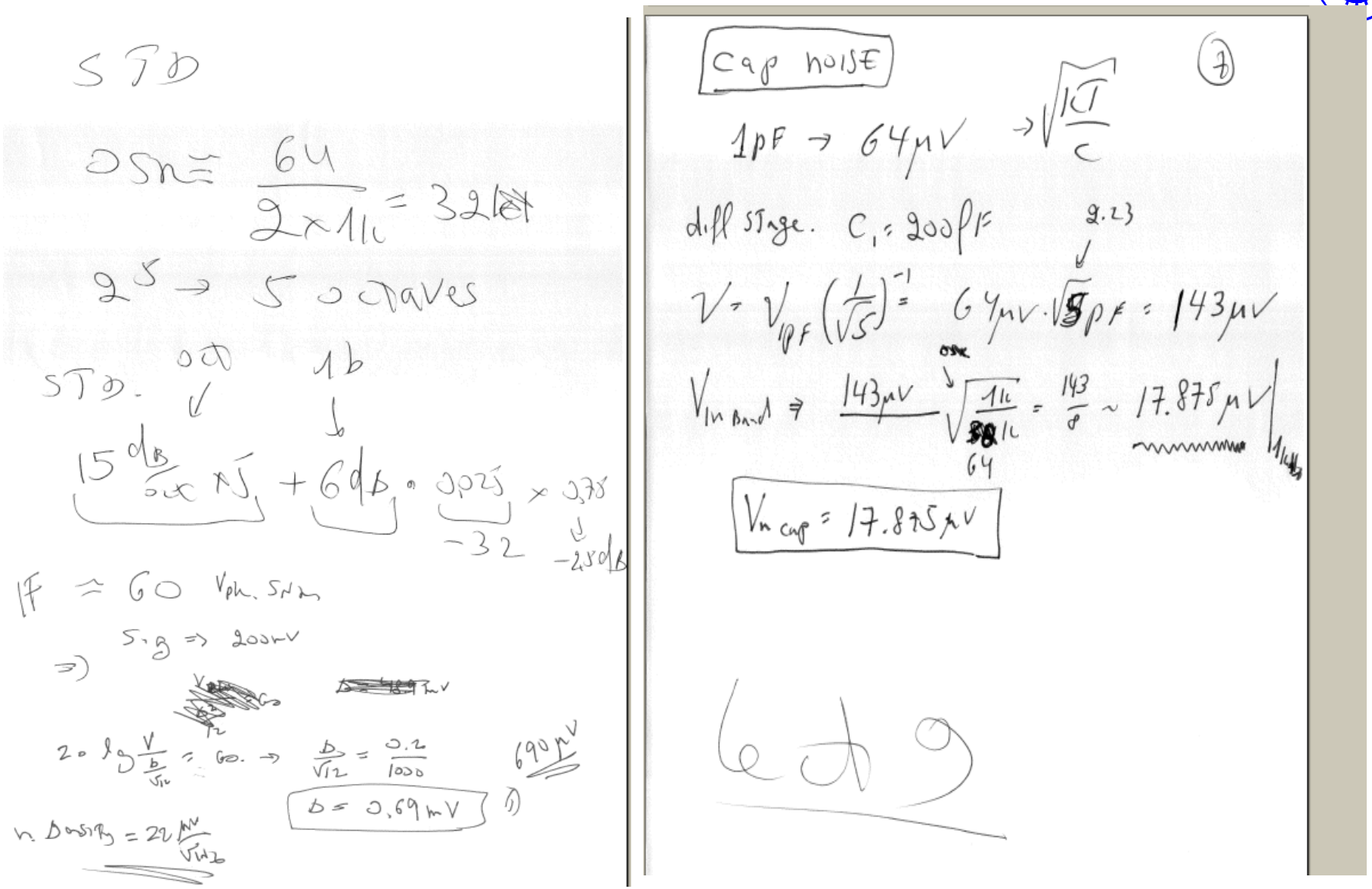
What's going on ?

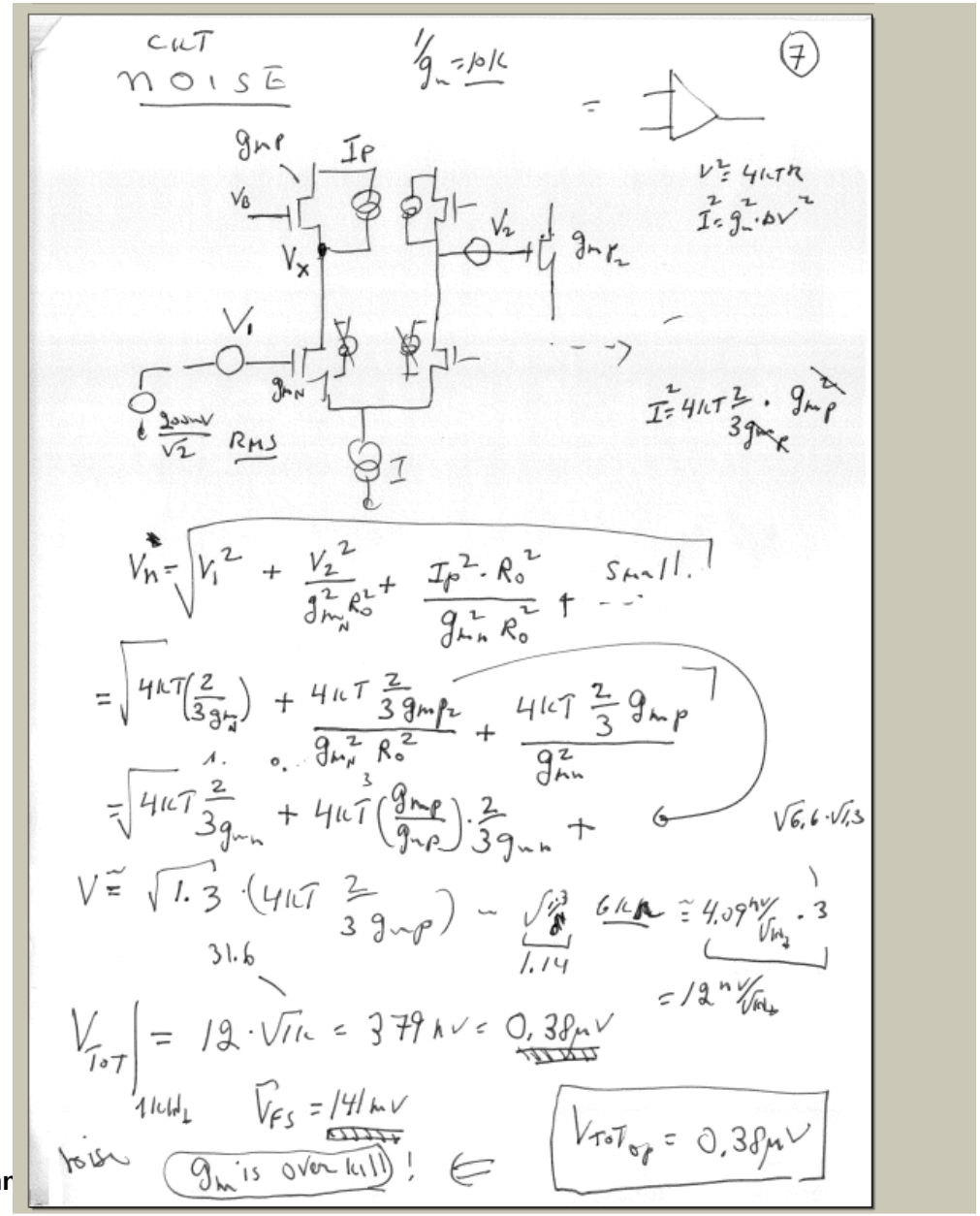
Given only :
Clock rate => fck = 62 KHz , Vsigpk=0.2V
C1 =100 ff , C3=100 ff
C2= 1pf C4=0.5 pF op: gm=100e-6 1/ohm

Identify loop order
Identify bit order
Calculate integrator time constant values
Calculate Ks – Stability issues
Estimate max BW and potential maximum OSR
Estimate effective number of bits, and SNR (quantization)
Calculate noise sources (caps, Reference, devices)

DESIGN in class




STD
OSR ≃ 64 / 2×11 = 32
2^5 → 5 octaves
STD. 0d 1b
15 dB/oct × 5 + 6dB · 0.25 × 0.75
−32 −2.50dB
IF ≃ 60 V_ph. SNR
5.9 ⇒ 200mV
⇒
2·log V/(b/√12) ≃ 60. → b/√12 = 0.2/1000
690μV
b = 0.69mV
n. Density = 22 nV/√Hz
Cap noise
1pF → 64μV → √(kT/C)
diff stage. C₁ = 200pF
2.23
V = V_1pF (1/√5)^-1 = 64μV·√5pF = 143μV
V_in Band ⇒ 143μV / √(11/64) = 143/8 ~ 17.875μV
OSR
V_n cap = 17.875μV
7


CMT
NOISE
7
$g_m = 10/k$
g_{mp}
I_p
V_B
V_x
V_2
$g_{mp} r_2$
V_1
g_{mN}
$\frac{200mV}{\sqrt{2}}$ RMS
I
$\overline{V^2} = 4kTR$
$\overline{I^2} = g_m^2 \cdot \overline{\Delta V^2}$
$\overline{I^2} = 4kT \frac{2}{3g_m R} \cdot g_{mp}$
$\overline{V_n} = \sqrt{V_1^2 + \frac{V_2^2}{g_{mN}^2 R_0^2} + \frac{I_p^2 \cdot R_0^2}{g_{mn}^2 R_0^2} + \text{small}}$
$= \sqrt{4kT\left(\frac{2}{3g_{mN}}\right) + \frac{4kT\frac{2}{3}g_{mp}r_2}{g_{mN}^2 R_0^2} + \frac{4kT\frac{2}{3}g_{mp}}{g_{mn}^2}}$
1. 0.
$= \sqrt{4kT\frac{2}{3g_{mn}} + 4kT\left(\frac{g_{mp}}{g_{mn}}\right)^3 \cdot \frac{2}{3g_{mn}} + \ldots}$
$\sqrt{6.6} \cdot \sqrt{1.3}$
$\overline{V} = \sqrt{1.3} \cdot \left(4kT\frac{2}{3g_{mp}}\right) \sim \sqrt{\frac{13}{6}}$ $6kR$ $\approx 4.09 \frac{nV}{\sqrt{Hz}} \cdot 3$
31.6
1.14
$= 12 \frac{nV}{\sqrt{Hz}}$
$V_{TOT}\Big|_{1kHz} = 12 \cdot \sqrt{1k} = 379nV = 0.38\mu V$
$V_{FS} = 141mV$
noise
g_m is overkill !
$V_{TOT_{op}} = 0.38\mu V$

Design 3rd order Switch C and CT ADC

① want Low/Lowest power ①

② want ~ 14 b converter 84dB PkSnR

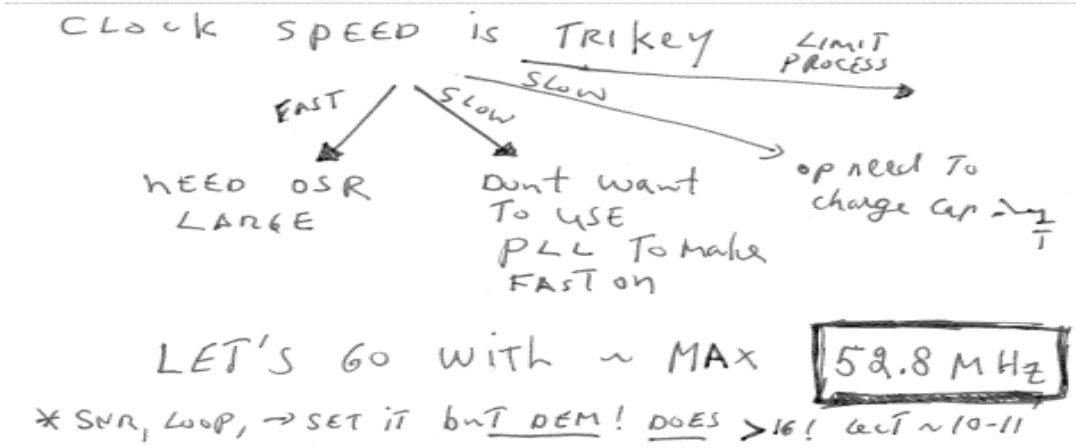
③ Sigma Delta ADC

Given, Can't change

A) Technology → Let go with CMOS 0.35μ, 3.3V

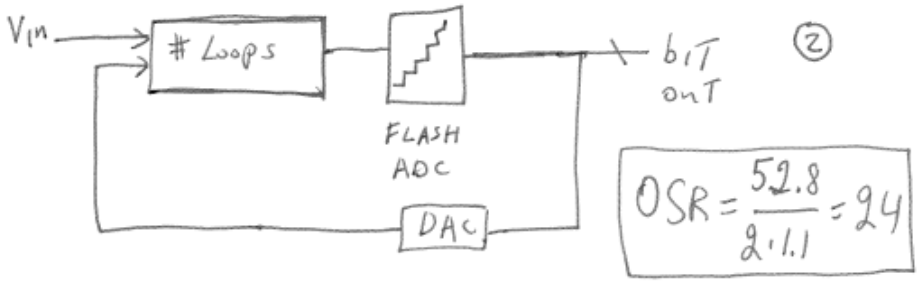
B) Input Full schale → $V_{FS} = 0.5V$

C) clock → Can decide but 20-60 MHz



Want signal=1.1MHz !
Want 84dB (ADSL)

Design in both: TC and SC.
Because some parameters are easier to calculate in TC some in SC



②

$$OSR = \frac{52.8}{2 \cdot 1.1} = 24$$

choice

LESS POWER
LESS LOOPS
LESS FLASH COMP

1 Loop → no (can't meet SNR)

2 Loop → no Can't meet SNR

3 Loop → YES

2-2 MASH → To MANY CKT'S

2-1 MASH → ~//~

FLASH & DAC

1 b → only 6dB Gain SNR → no

2 b → only 12dB Gain SNR → no

3 b, 4 b } NEED To calculate → GOOD

5 b → 2^5 comp, 2^5 DAC; Too Much/offset → no

$2^x = 24$

with OSR 24 ⇒ 4.58 octaves.

~ 21 dB/oct

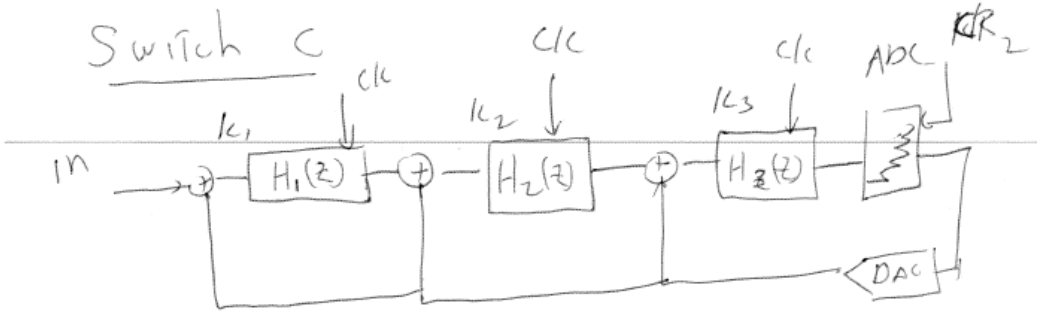
③

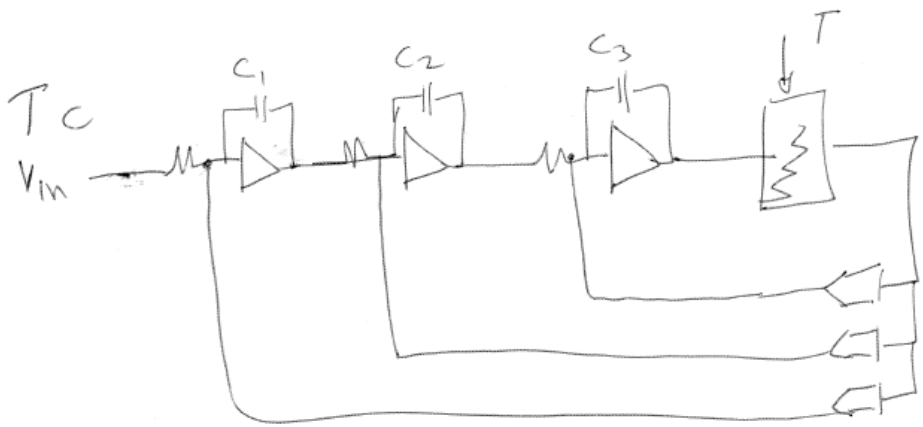
Let go with

3RD ORDER, ΔΣ, 4-bit quantizer

construction of 84 dB Low power.
SD 2.2 Mb/s (1.1 MHz)

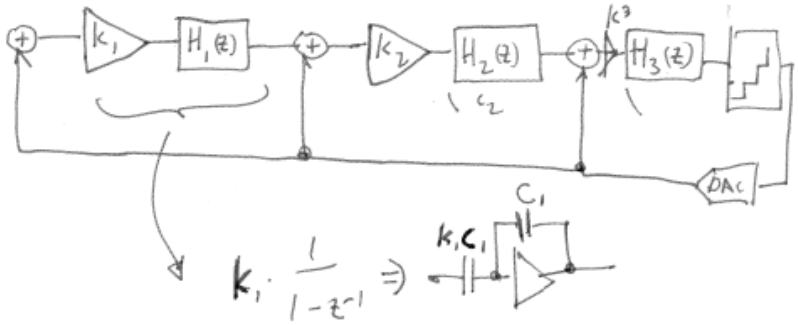
EXAMPLE





NEXT CALCULATE k_1, k_2, k_3 ⑤

USE Switch C iTs EASIER FOR k's



1ST INTEGRATOR Φ CROSSING IS THE CLOSEST POLE OF THE T.F ≥ 1.1 MHz

OR WE WON'T PASS SIGNALS.

⊛ I TAKE 2.5 MHz (TWICE)

TOO FAR [illegible] WILL FORCE OTHER k's TO GO UP.

TOO CLOSE IS ATTENUATION

& MORE IMPORTANT ⇒ CLIPPING

$$f_1 = \frac{1}{2\pi "R" C} = \frac{1 \cdot C_i}{2\pi C_F} T_s$$

(6)

$$f_1 = \frac{k_1 \Delta V}{2\pi \Delta V} f_s, \quad f_s = 52.8\,MHz, \quad f_1 = 2.5\,MHz$$

$$k_1 = \frac{2.5}{52.8} \cdot 2\pi \cong 0.3$$

$f_2 \Rightarrow$ should be $\sim 2.5 f_1$

$f_3 \Rightarrow$ should be $\sim 2.5 f_2$

$$\Rightarrow \quad f_1 = 2.5\,MHz \rightarrow k_1 = 0.3$$
$$f_2 = 6.25\,MHz \rightarrow k_2 = 0.75$$
$$f_3 = 15.625\,MHz \rightarrow k_3 = 1.875$$

1) Stability analysis, with number of bits (4)
2) Noise TF can optimize the value $\pm 20\%$ of the range!

In CT
BW & last op need to be large.

CALCULATE SNR

(7)

B = DAC bits = 4
R = OSR = 24
N = ADC order = 3
Overload V $\cong$ 0.75

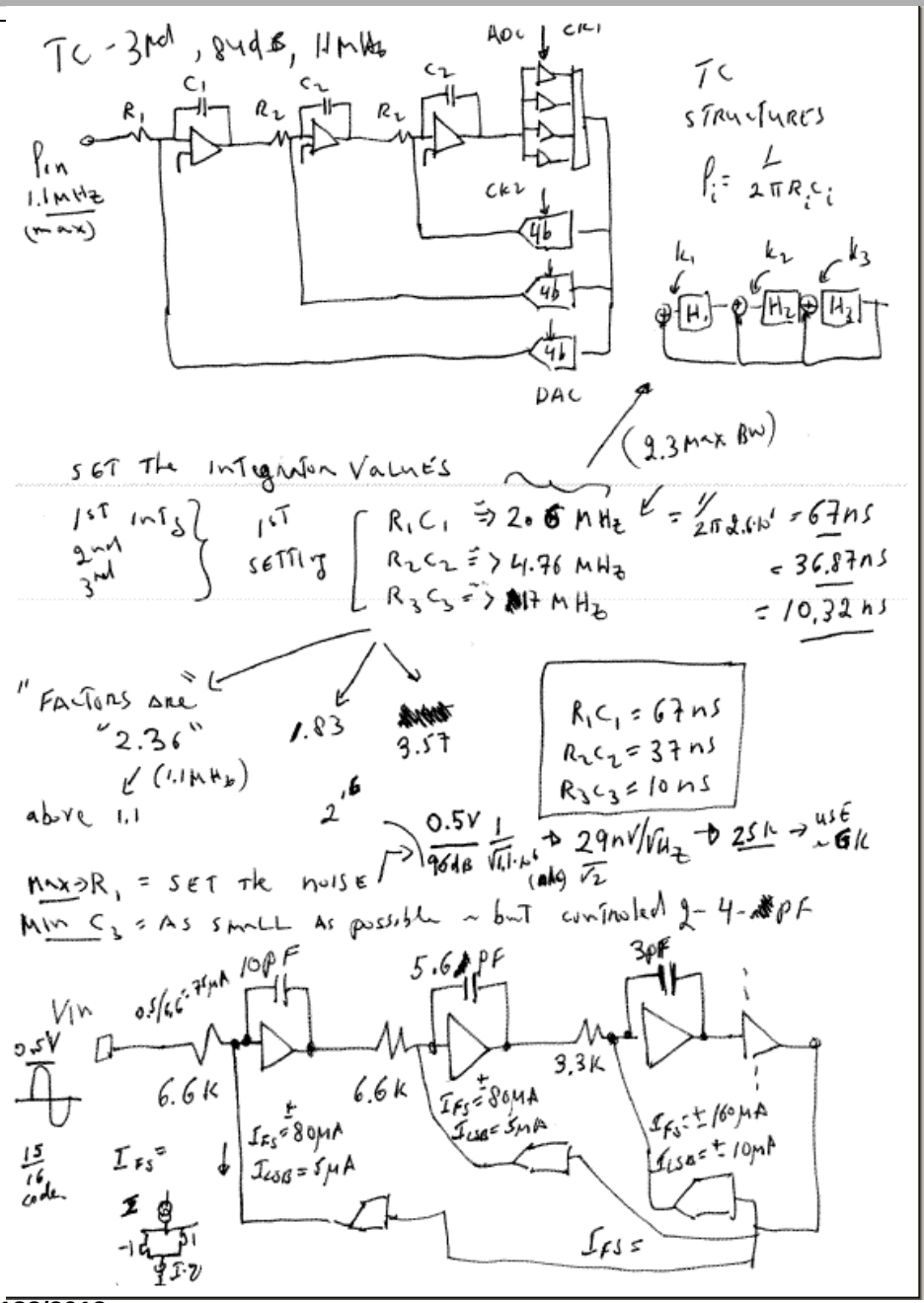
$q_0 = k_1 = 0.3$
$q_1 = k_2$ 0.875
$q_2 = k_3$ 1.875

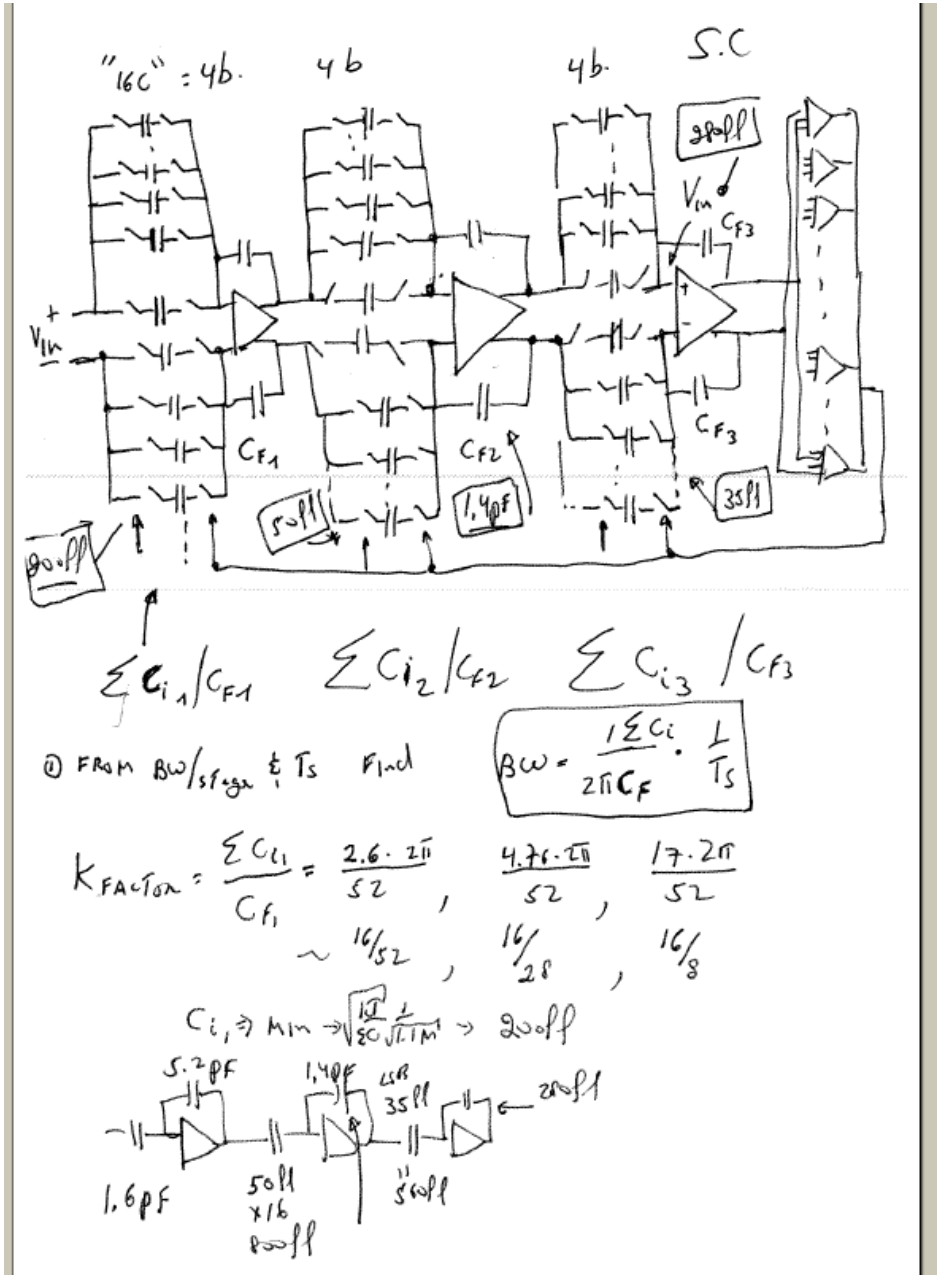
$$SNR_{PL} = \left[2^B - 1\right]^2 \cdot (2n+1)\left(\frac{R}{\pi}\right)^{2n+1} \cdot q_0 \cdot q_1 \cdot q_2 \left(\frac{3\pi}{2}\right) \cdot V$$

$$SNR = 10 \lg \left[2^4 - 1\right]^2 \cdot (2 \cdot 3 + 1)\left(\frac{24}{\pi}\right)^{2 \cdot 3 + 1} \cdot 0.3 \cdot 0.875 \cdot 1.875$$

$$10 \lg \left[225 \cdot 7 \cdot \left(\frac{24}{\pi}\right)^7 \cdot 0.369\right] = 89.45\,dB$$

Not bad we want 84
so we have some margin !


TC - 3rd, 84dB, 1MHz
ADC
CK1
CK2
DAC
TC STRUCTURES
SET THE INTEGRATION VALUES
(2.3 max BW)
1st int
2nd
3rd
1st SETTLING
R1C1 ⇒ 2.65 MHz = 1/2π2.6M = 67ns
R2C2 ⇒ 4.76 MHz = 36.87ns
R3C3 ⇒ 17 MHz = 10,32 ns
"FACTORS ARE"
"2.36"
1.83
3.57
above 1.1
2^16
R1C1 = 67 ns
R2C2 = 37 ns
R3C3 = 10 ns
MAX ⇒ R1 = SET THE NOISE
MIN C3 = AS SMALL AS POSSIBLE ~ BUT CONTROLED 2- 4- pF
Vin
0.5V
6.6K
6.6K
3.3K
10pF
5.6pF
3pF
15/16 code
IFS =
IFS = ±80μA
ILSB = 5μA
IFS = ±160μA
ILSB = ±10μA


"16C" = 4b.
4b
4b.
S.C
200ff
V_{in}
C_{F3}
V_{in}
C_{F1}
C_{F2}
C_{F3}
50ff
1.4pF
35ff
200ff
$\Sigma C_{i1}/C_{F1}$
$\Sigma C_{i2}/C_{F2}$
$\Sigma C_{i3}/C_{F3}$
① FROM BW/stage & T_s Find
$BW = \frac{1}{2\pi C_F}\cdot\frac{\Sigma C_i}{T_s}$
$K_{FACTOR} = \frac{\Sigma C_{i1}}{C_{F1}} = \frac{2.6\cdot 2\pi}{52}, \frac{4.76\cdot 2\pi}{52}, \frac{17\cdot 2\pi}{52}$
$\sim 16/52, 16/28, 16/8$
$C_{i1} \Rightarrow$ Min $\rightarrow \sqrt{\frac{12T}{80}\frac{1}{\pi\cdot 1M}} \rightarrow$ 200ff
5.2pF
1.4pF
USB
35ff
200ff
1.6pF
50ff
x16
800ff
50ff

End Lecture 11

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