Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

Instructor: Dr. Miki Moyal

Lectures
http://www.gigalogchip.com/lectures.html

Lecture 10

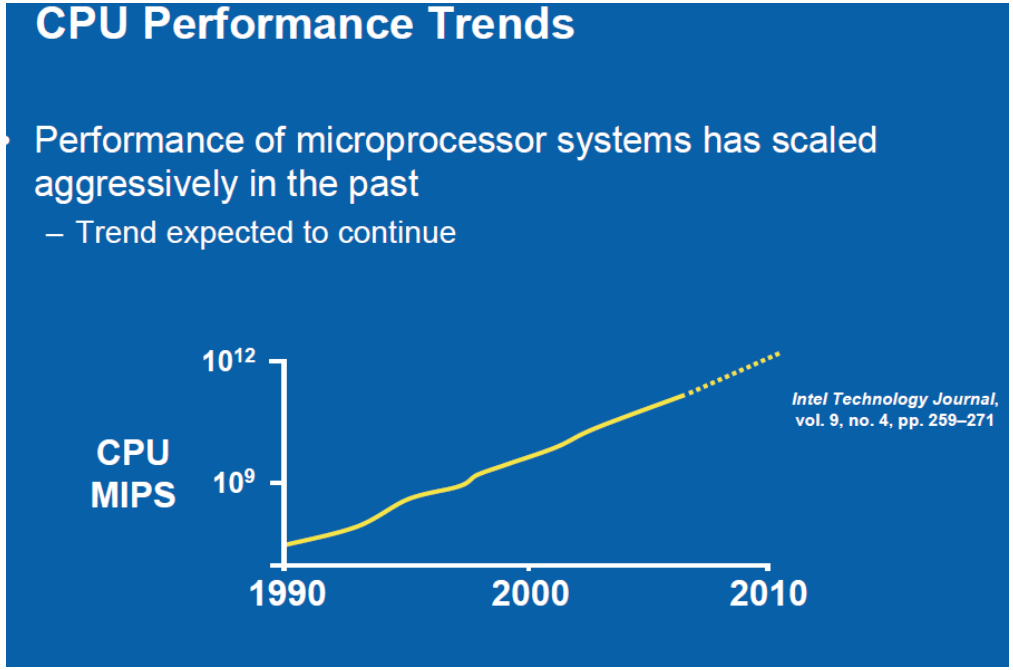
High Speed SerDes *Basics*
As a Serial link

Its your grade..

Project/assignments deadline: 1.5 mo. from now end of 2/2023

If you cant please send me e mail few days prior.
miki@gigalogchip.com

Why do we care ?

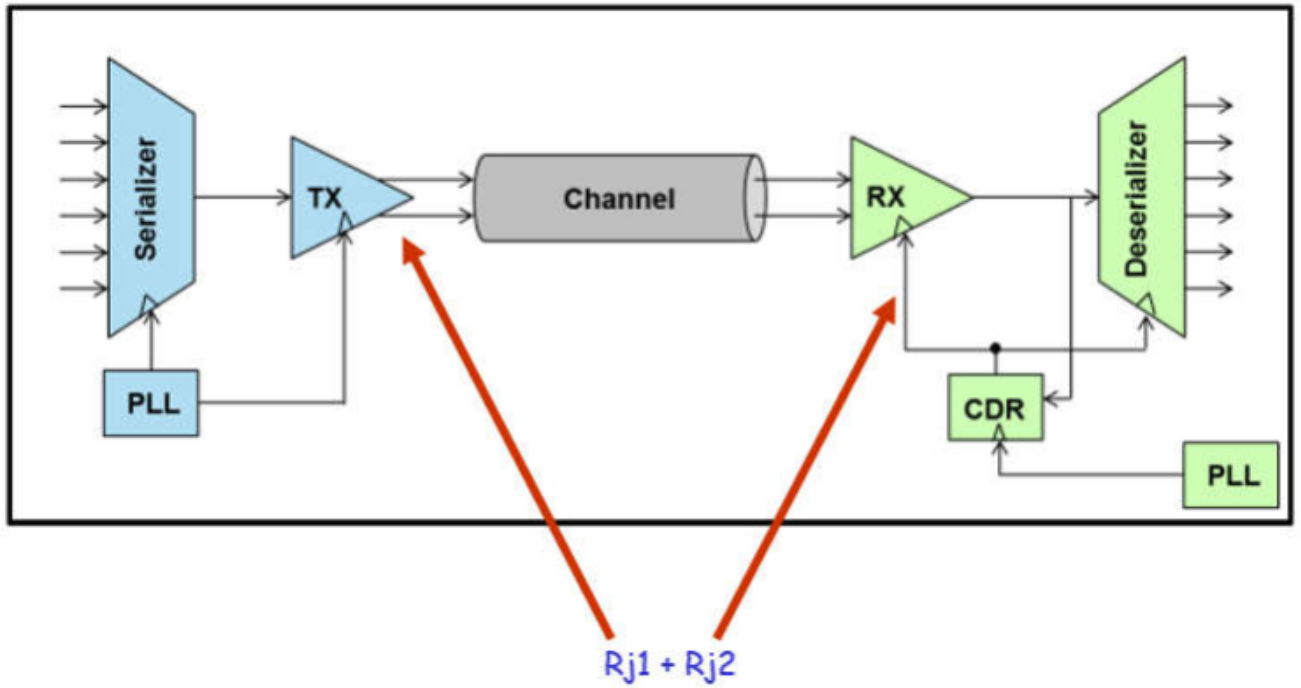


CPU freq. goes up
Everything increases..

But we are blocked.... on speed in and out
Memory2cpu, chip2chip..data2, data centers, I clouds…++

SerDes

input



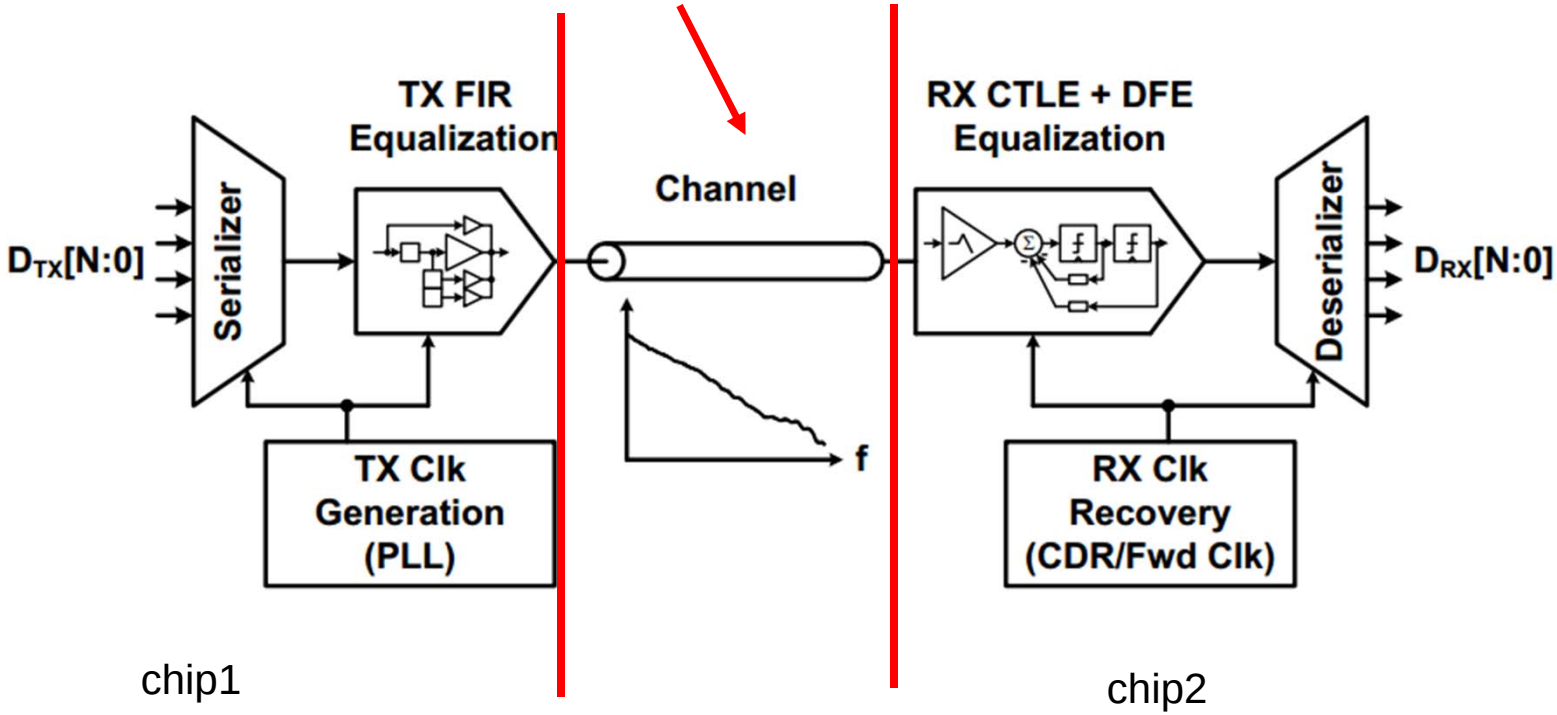
output

gure 44: SerDes for simplified jitter places

Want Transfer function =1

Wireline link

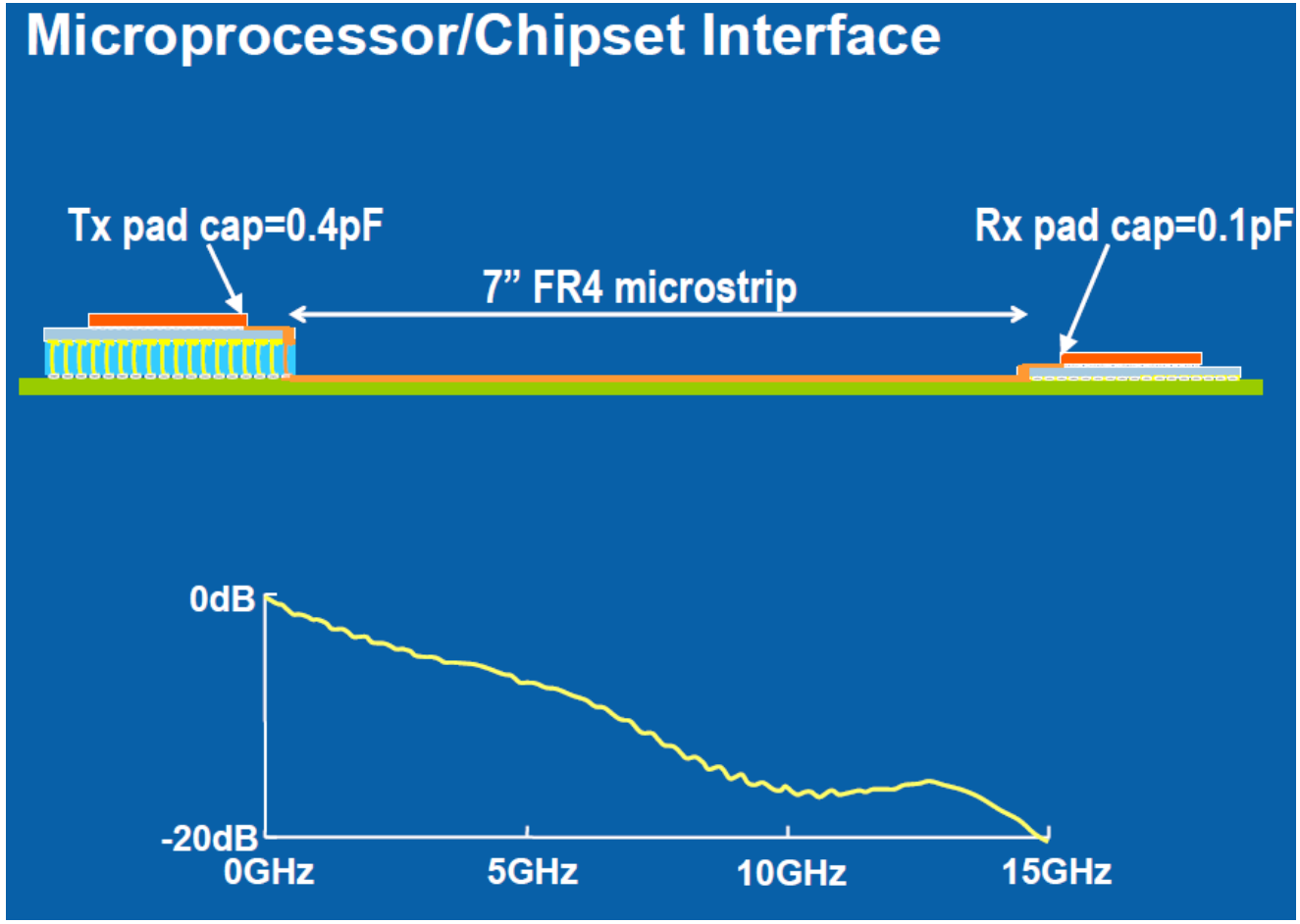
Fast as possible data: 10001001010101

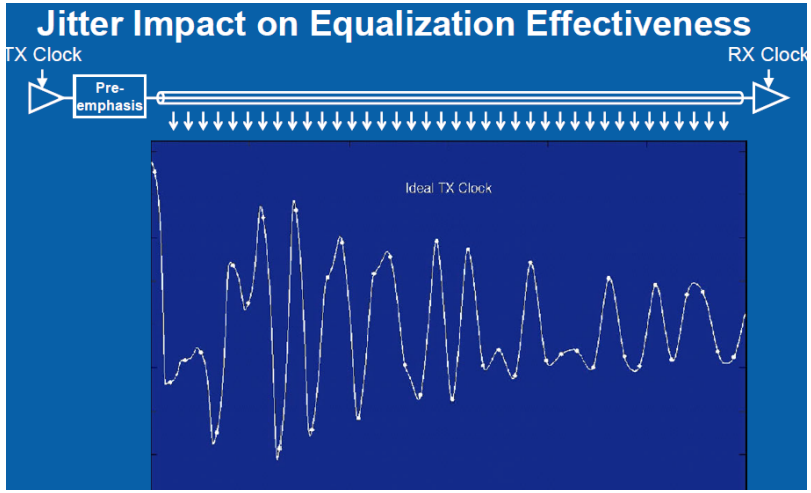


Want Transfer function =1

Few millimeters to few km (mostly few cm to 1 meter)

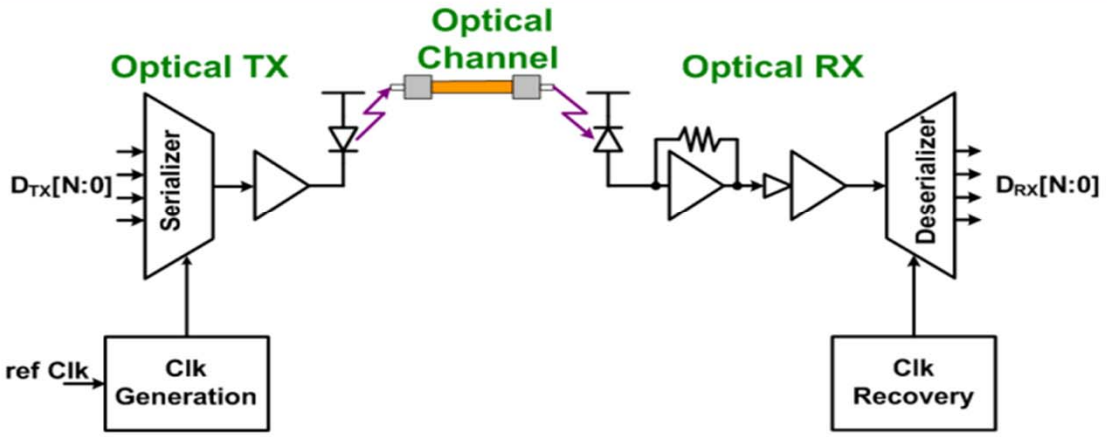
The line and BW.



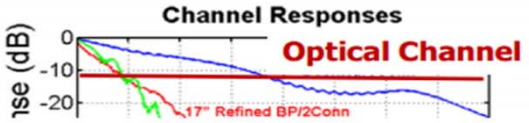


Optical link

High-Speed Optical Link System

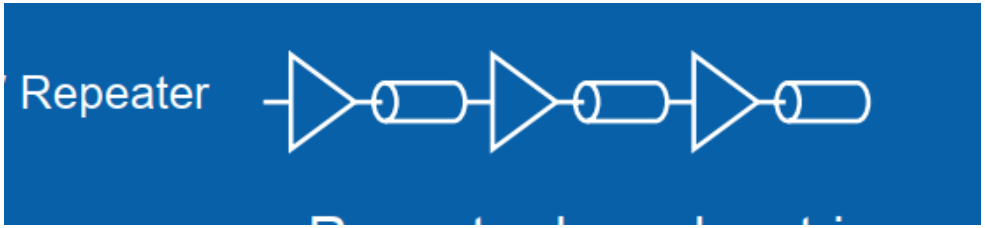


- Optical interconnects remove many channel limitations

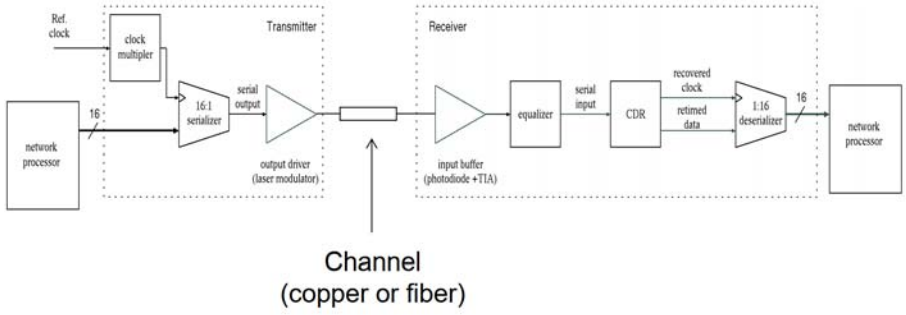


Options to deal with the data and clock…

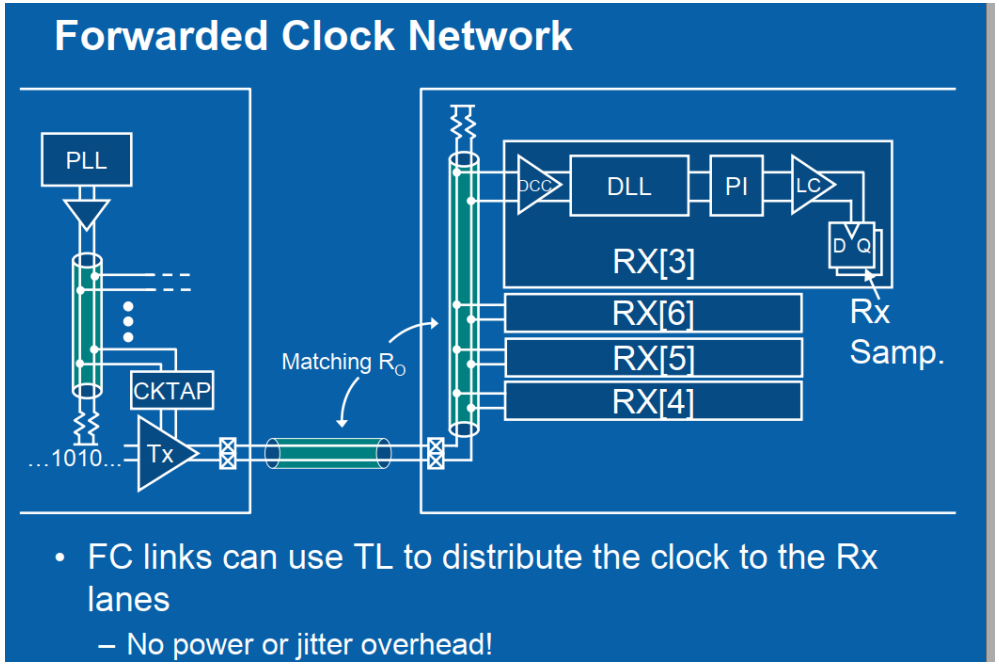
Easy way out..-



Most do this…



Next way out- send clock..



ISI- How does the line look like when data at different rate passes.

Enclosed is a line with considerably low band with: BW=1.7GHz
Enclosed is complete simulated Tx. pass

Let's assume a line (from transmitter to the end (beginning of the receiver of about -15dB (equivalent and close to 20cm line).

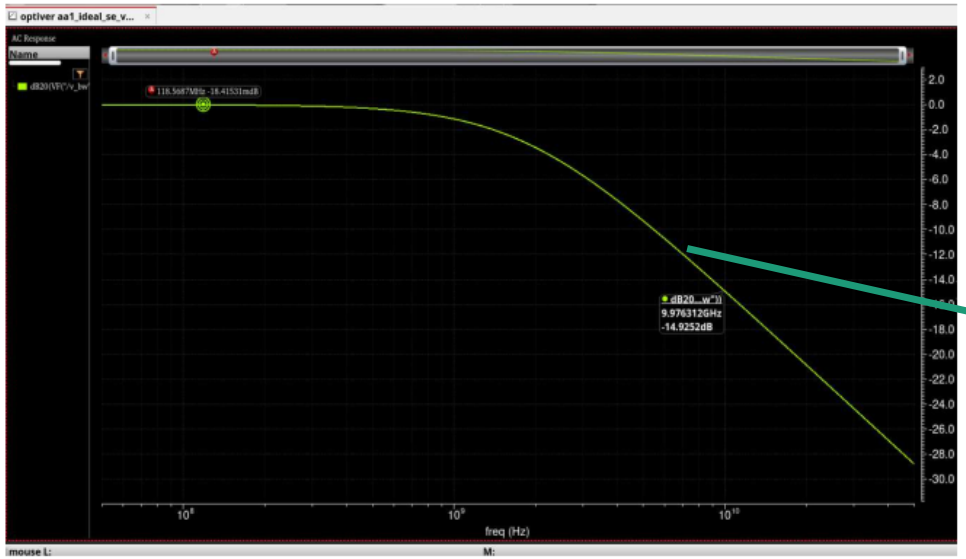
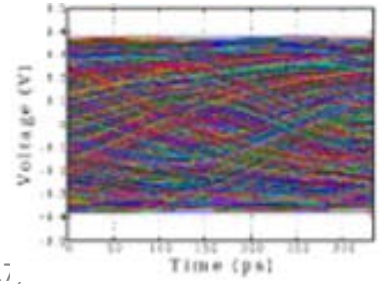


Figure 31: Loss in a 20cm line using simple RC filer: AC analysis

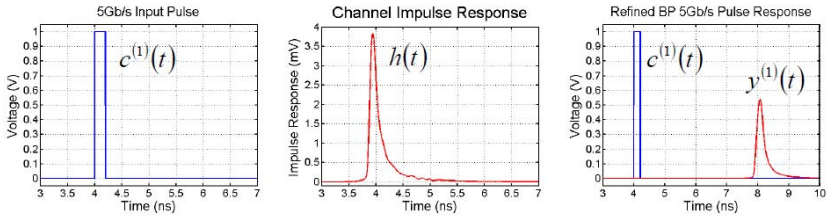


Input green
Output yellow
10gb/s

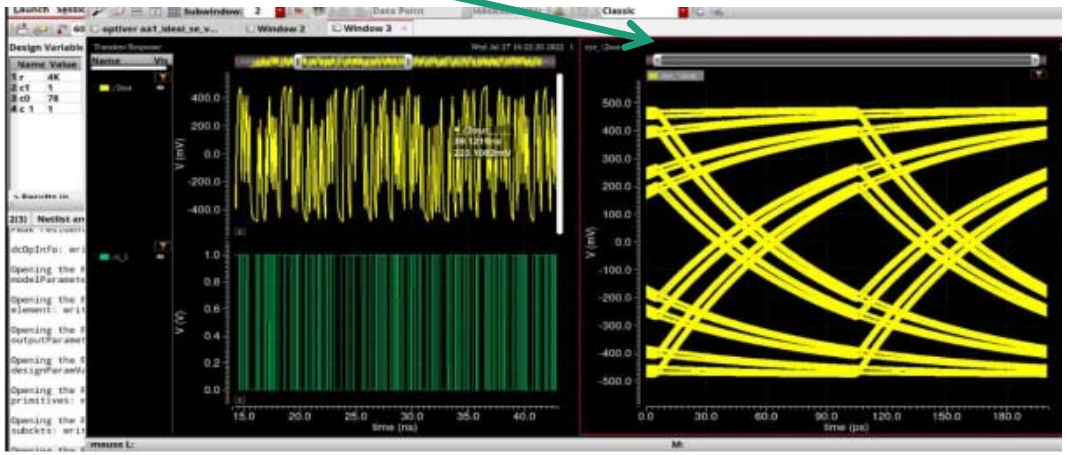
Inter-Symbol Interference (ISI)

- Previous bits residual state can distort the current bit, resulting in inter-symbol interference (ISI)
- ISI is caused by
  - Reflections, Channel resonances, Channel loss (dispersion)
- Pulse Response

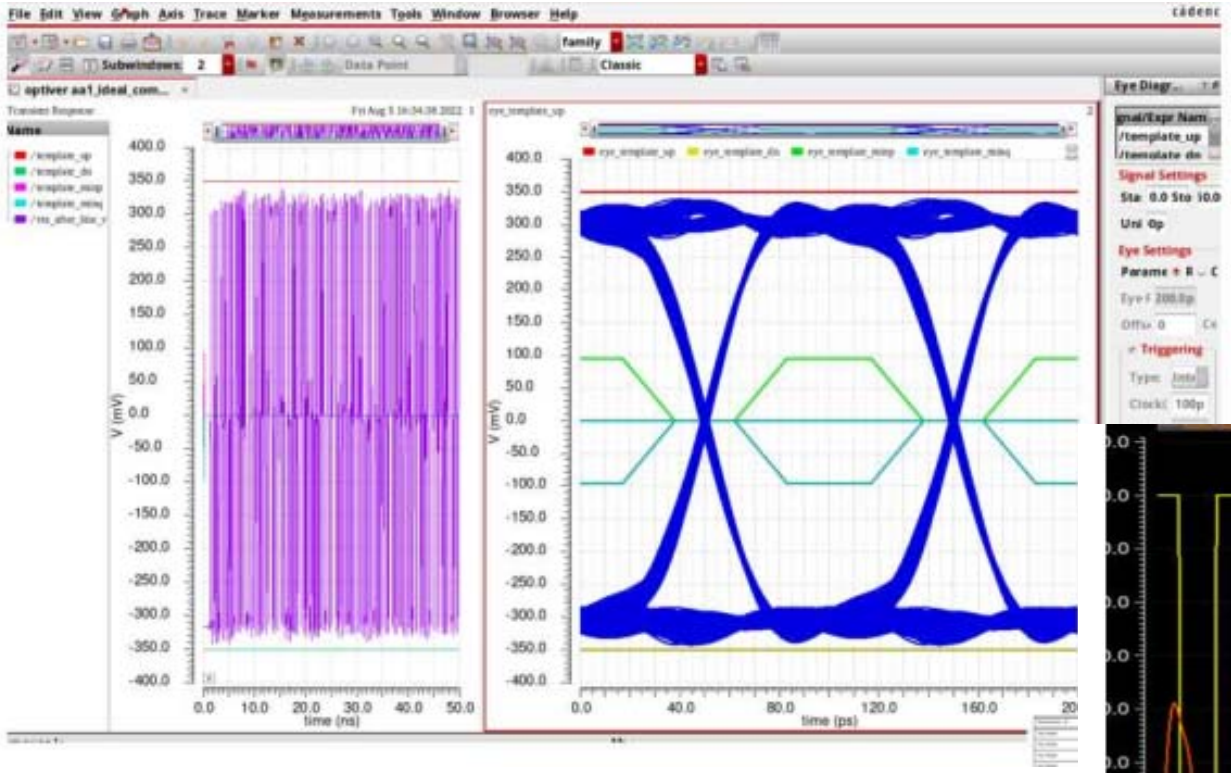
$$y^{(1)}(t) = c^{(1)}(t) * h(t)$$



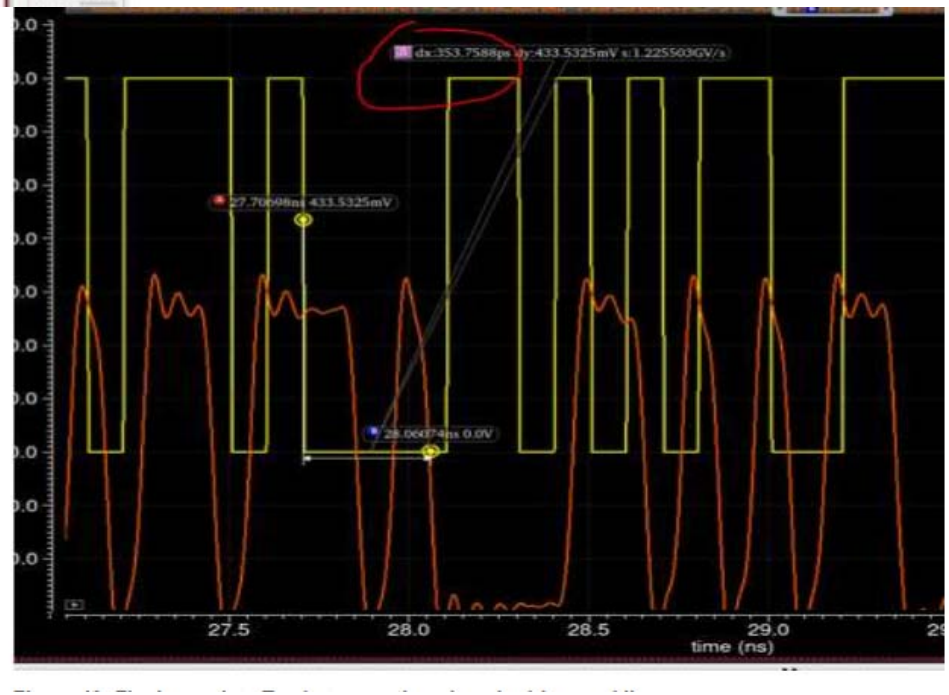
100ps=5MHz max, data bits and 1.7Mhz BW



This is what we need.



Want line transfer = 1
Impulse response is a way
to see the problem..

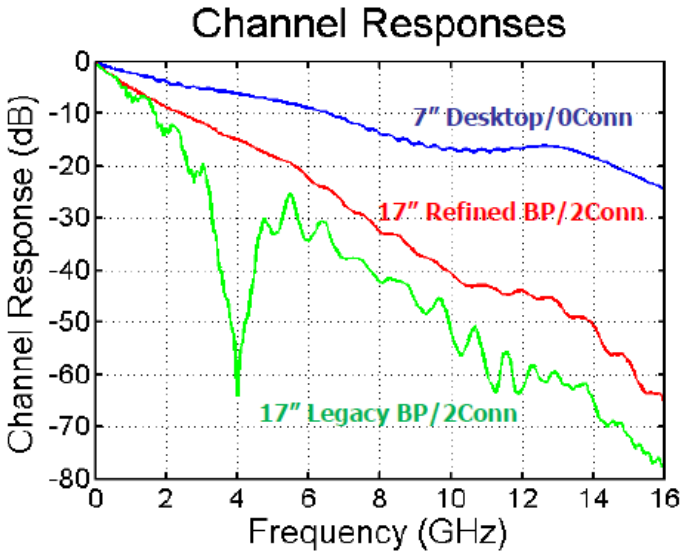


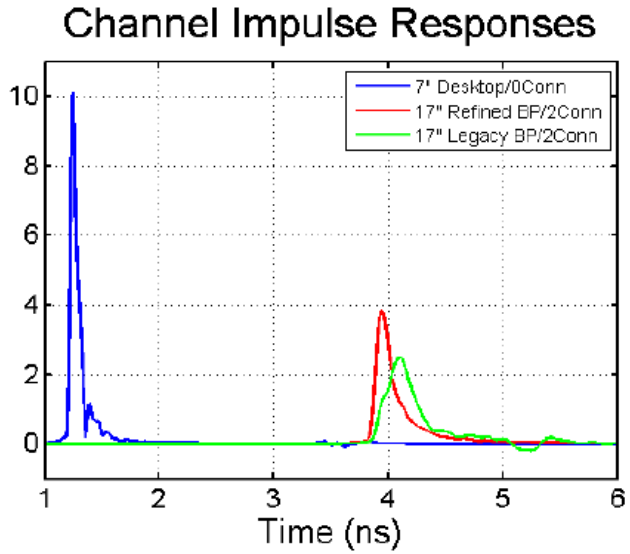
Frequency to time

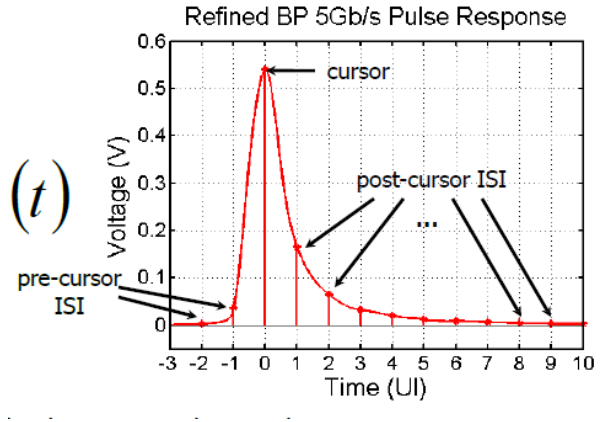
- Perform the inverse Fourier transform on the s-parameter of interest

$$h(t) = F^{-1}\{S(\omega)\}$$

Impulse Response of Different Channels



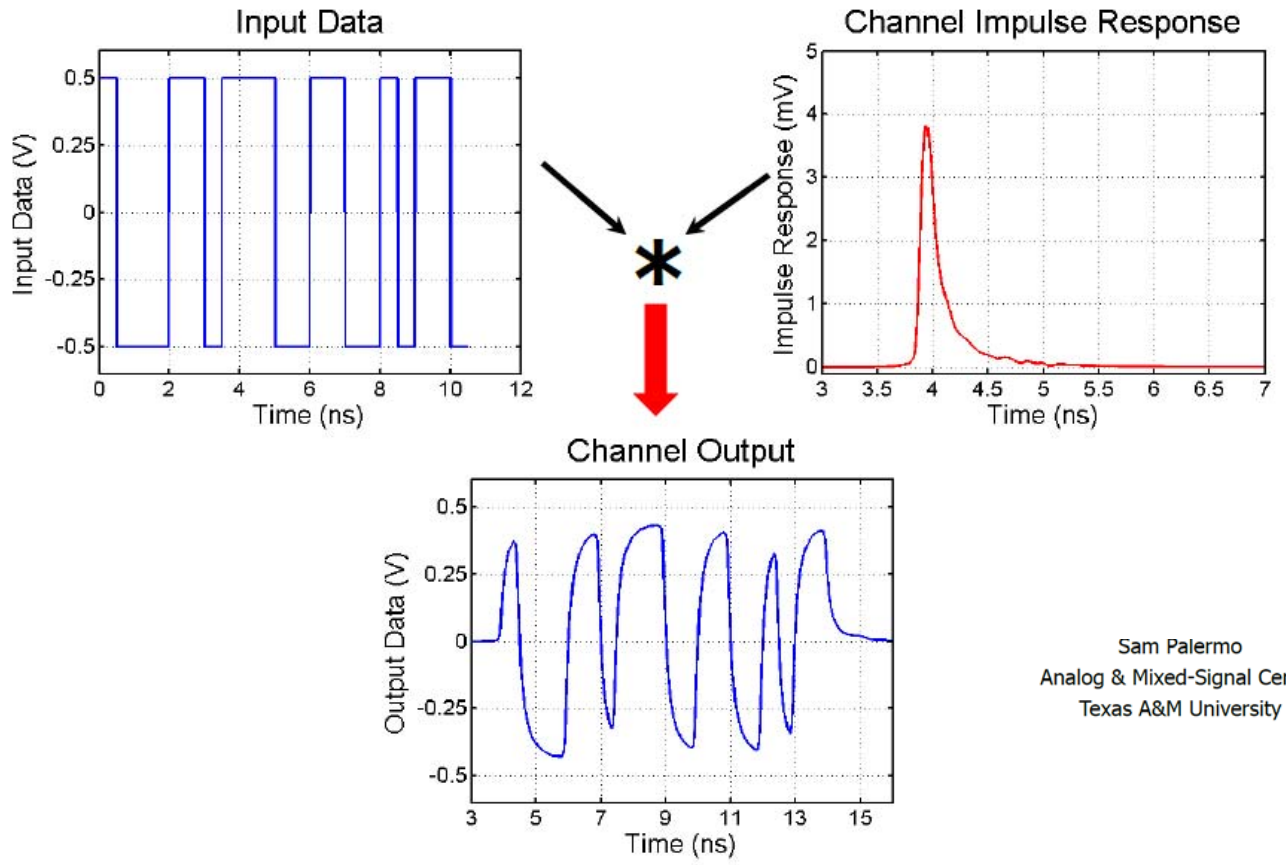




Sam Palermo
Analog & Mixed-Signal Center
Texas A&M University

Example…
Look at points in
1ui,2ui,3ui..
Bad channel can **last**
30 UIs…

Channel Transient Response



Sam Palermo
Analog & Mixed-Signal Center
Texas A&M University

What blocks are needed to do the job.

Paralell2serial
Transmitter buffer and equalization
Line
Receiver input (Rx.)
More equalization in Rx. - active CTLE
CDR
Serial2Parallel

Transmitter.

Paralell-2-serial

Option 1: Load the group and put them fast 1 by 1..

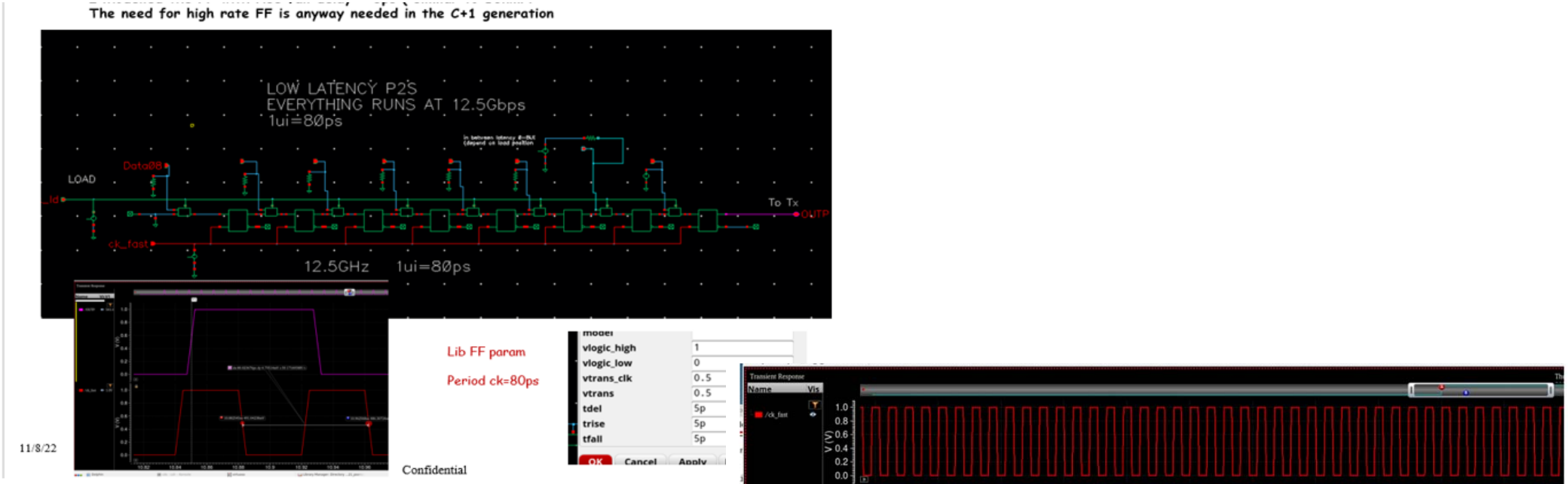


Figure 13: P2S (8:1) low latency design.

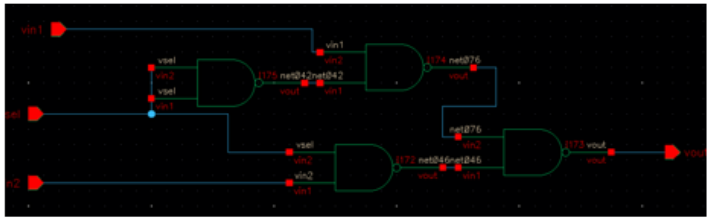
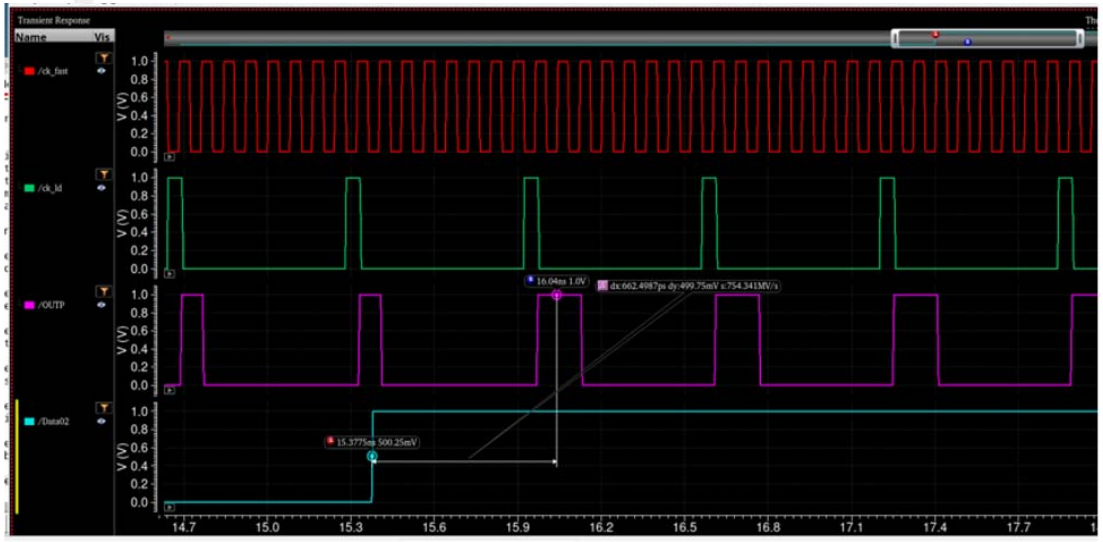


Figure 14: Mux concept for high level modeling



Option 2: cascade …

Tree-Type MUX

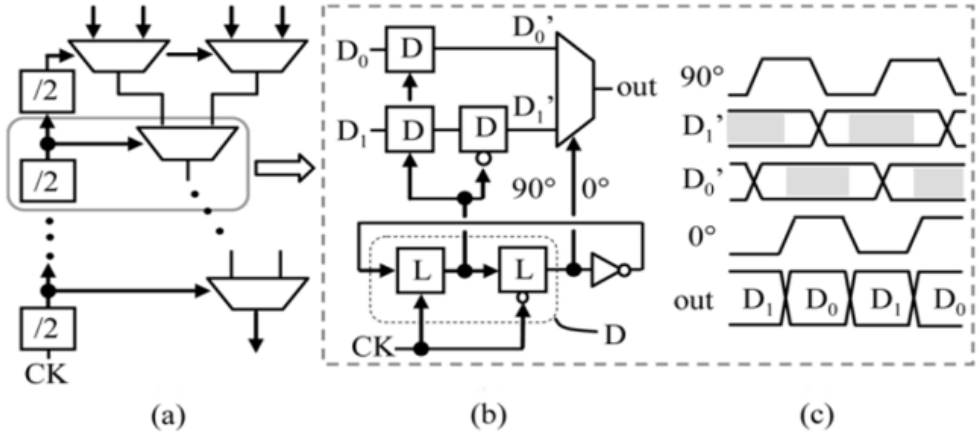
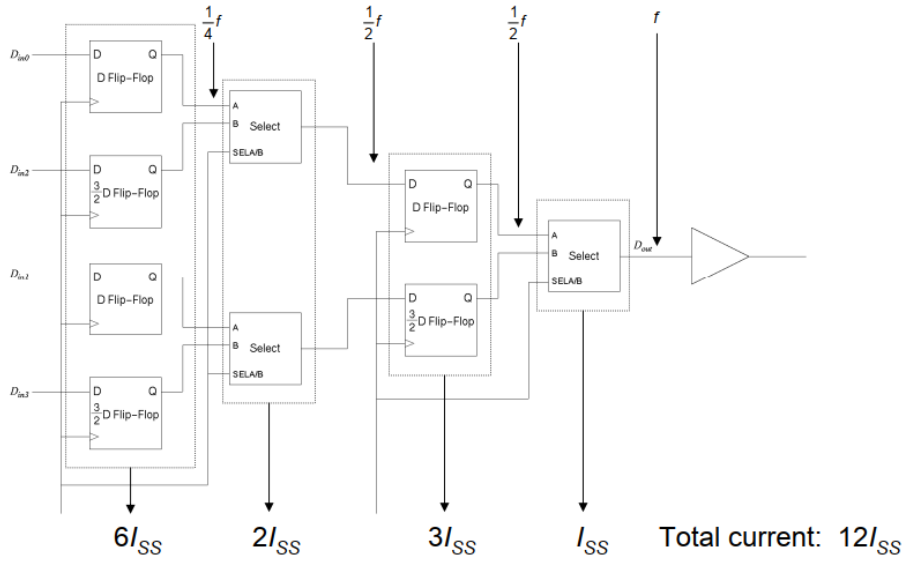


Figure 7 : The basics principle of P2S



Assume all blocks have:
- Tail current I_{SS}
- Resistor R
- Diff pair transistor sizes W/L

What's the difference ?

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srael Institute of Technology
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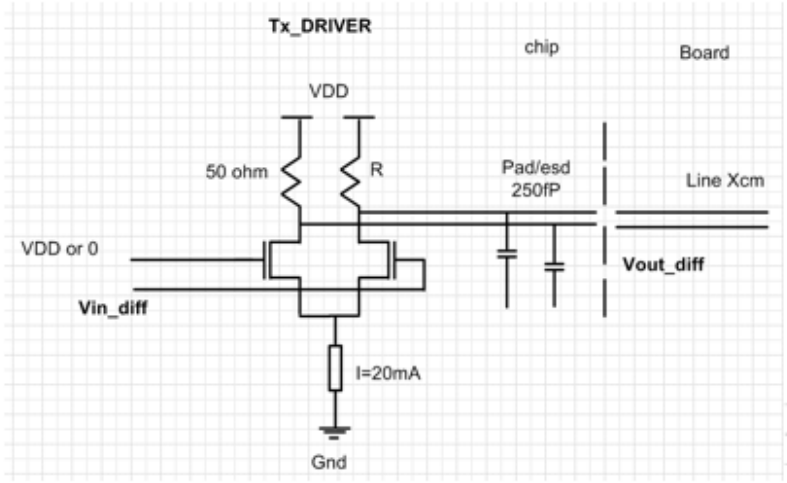
Tx. buffer and equalization

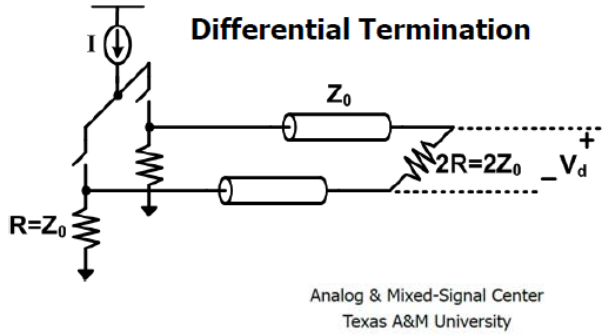
How to exit the chip at max. BW ?
ESD, package, line reflections etc..

max bw = no ISI ~ 3/4bit rare rule

If process is slow.- CML approach.

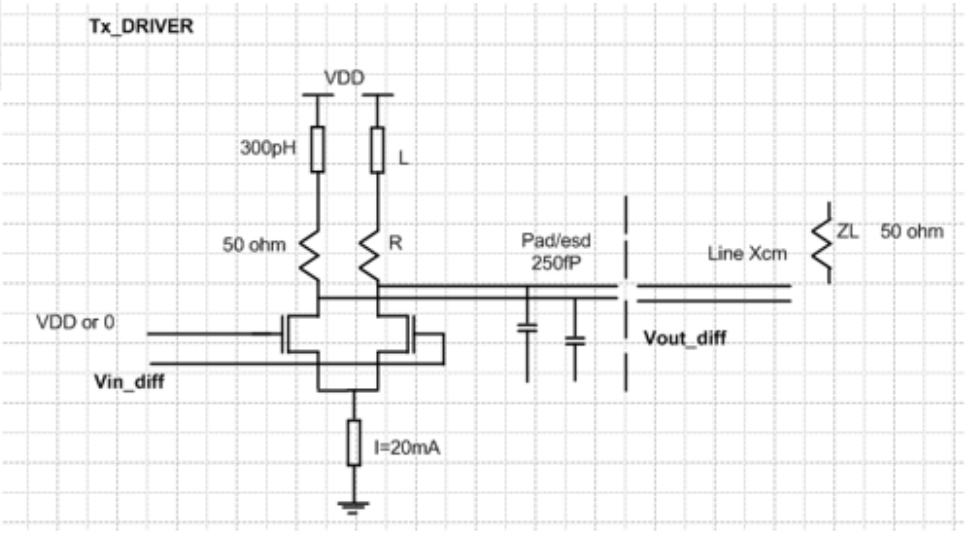
Evolution :



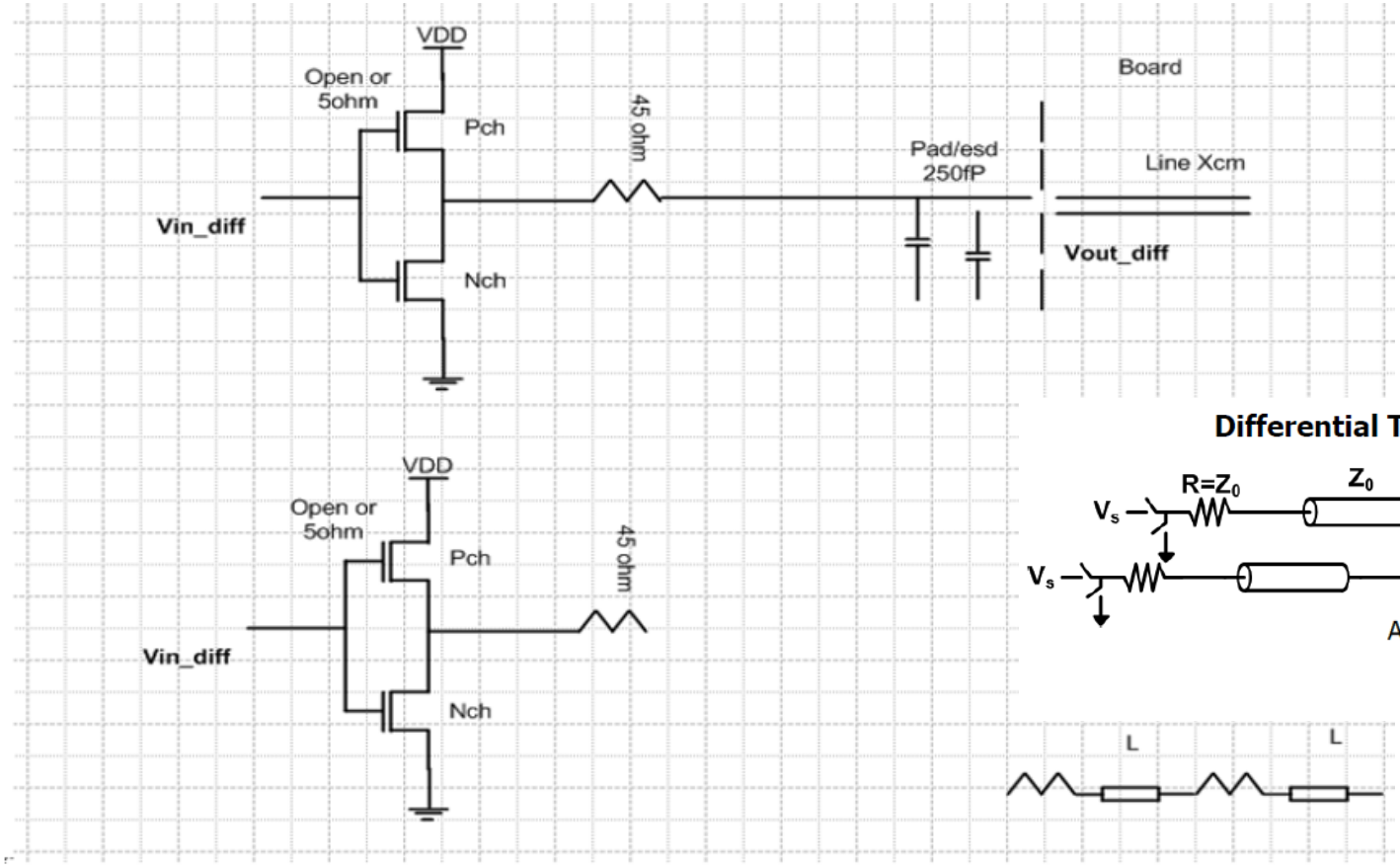


$$V_{d,1} = (I/4)(2R)$$
$$V_{d,0} = -(I/4)(2R)$$
$$V_{d,pp} = IR$$
$$I = \frac{V_{d,pp}}{R}$$

We can add L to make a peaking = **cancel the C**



Better way: voltage mode driver.



$$V_{d,1} = (V_s/2)$$
$$V_{d,1} = -(V_s/2)$$
$$V_{d,pp} = V_s$$
$$I = (V_s/4R)$$
$$\boldsymbol{I = \frac{V_{d,pp}}{4R}}$$

Figure 19: Voltage mode driver

Power waist is generally about 25% of the CML.

Now lets **add BW**

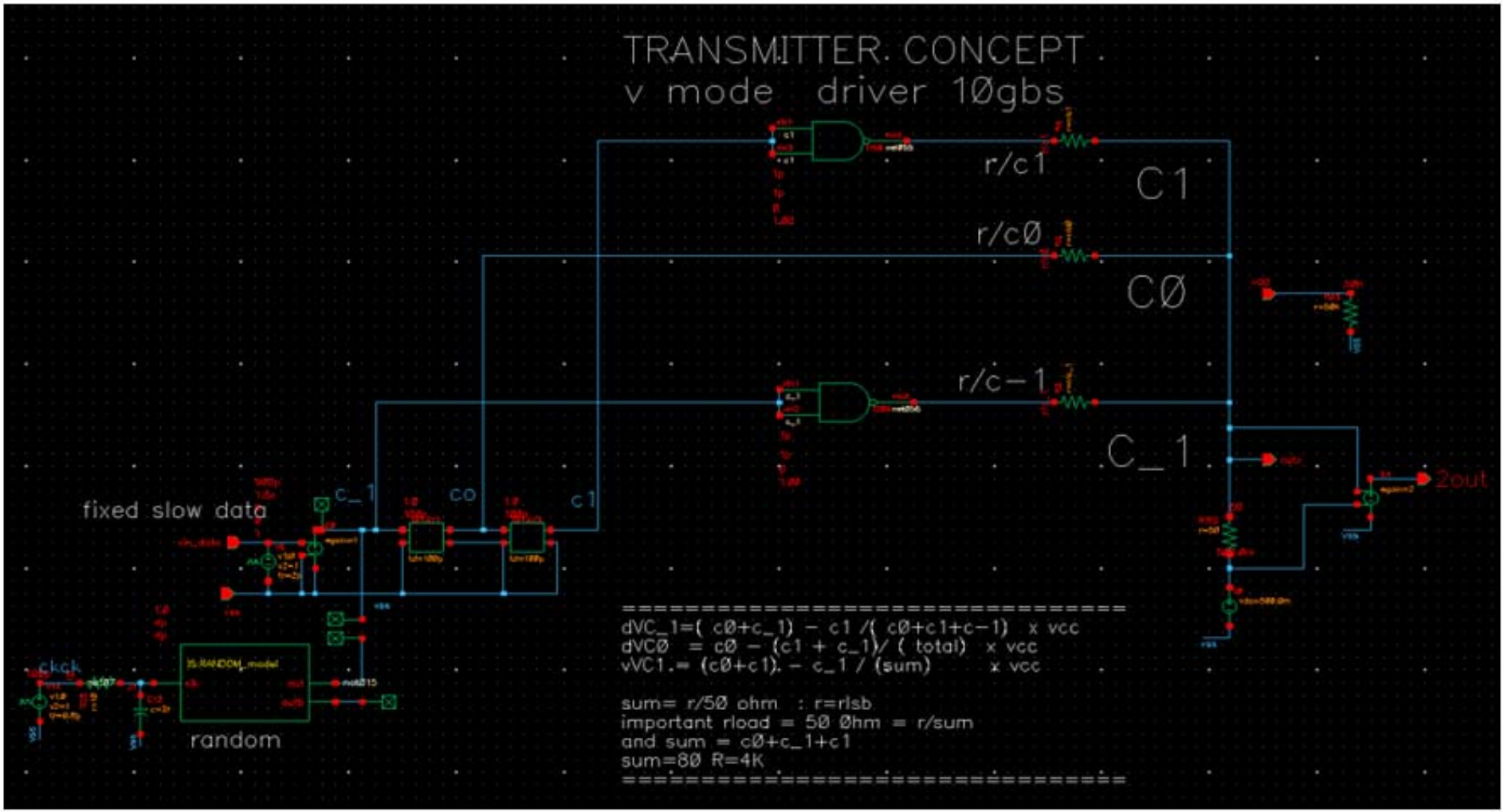
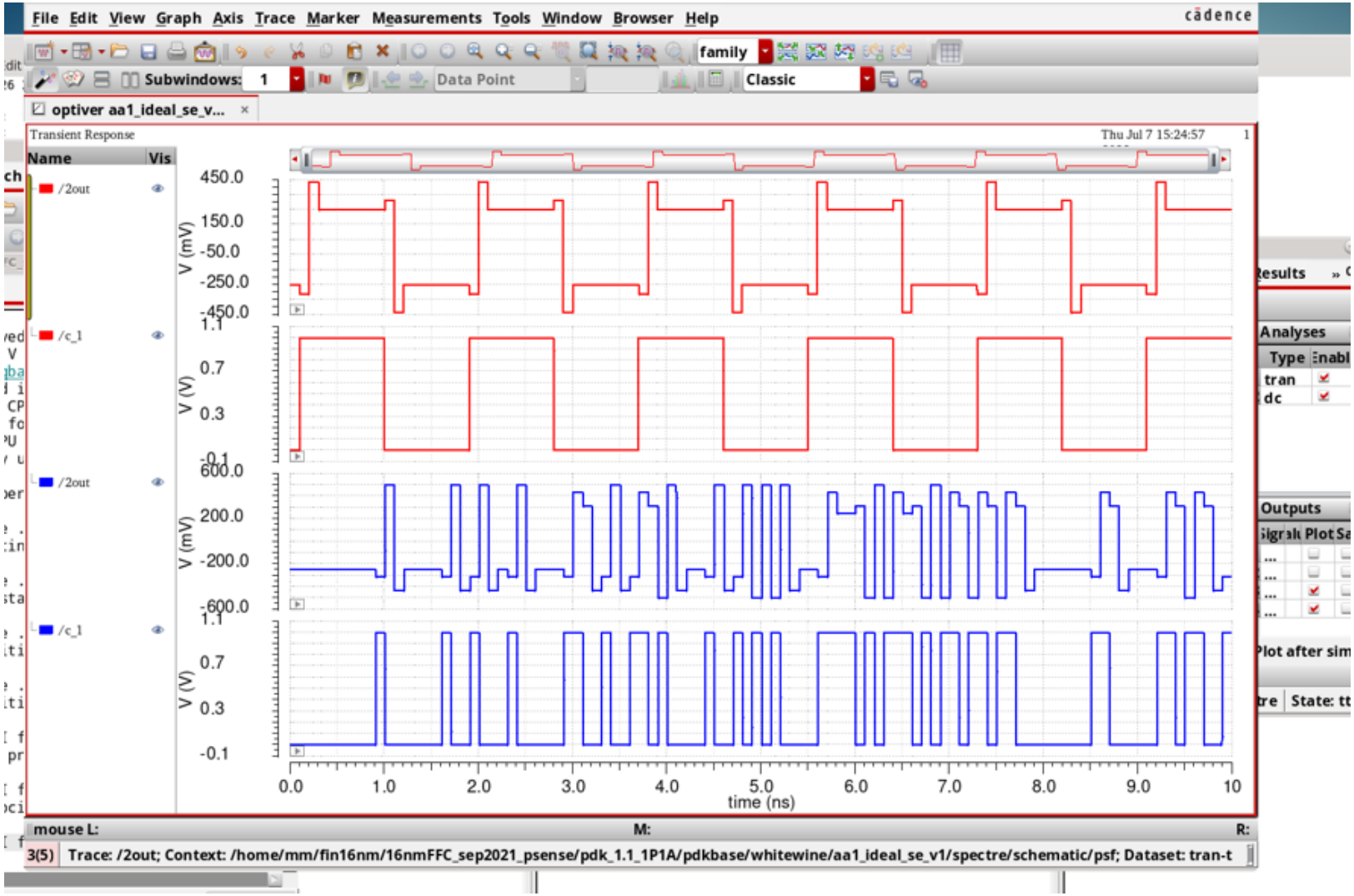


Figure 20: Single ended spice model of a Transmitter concept using 3 taps filter

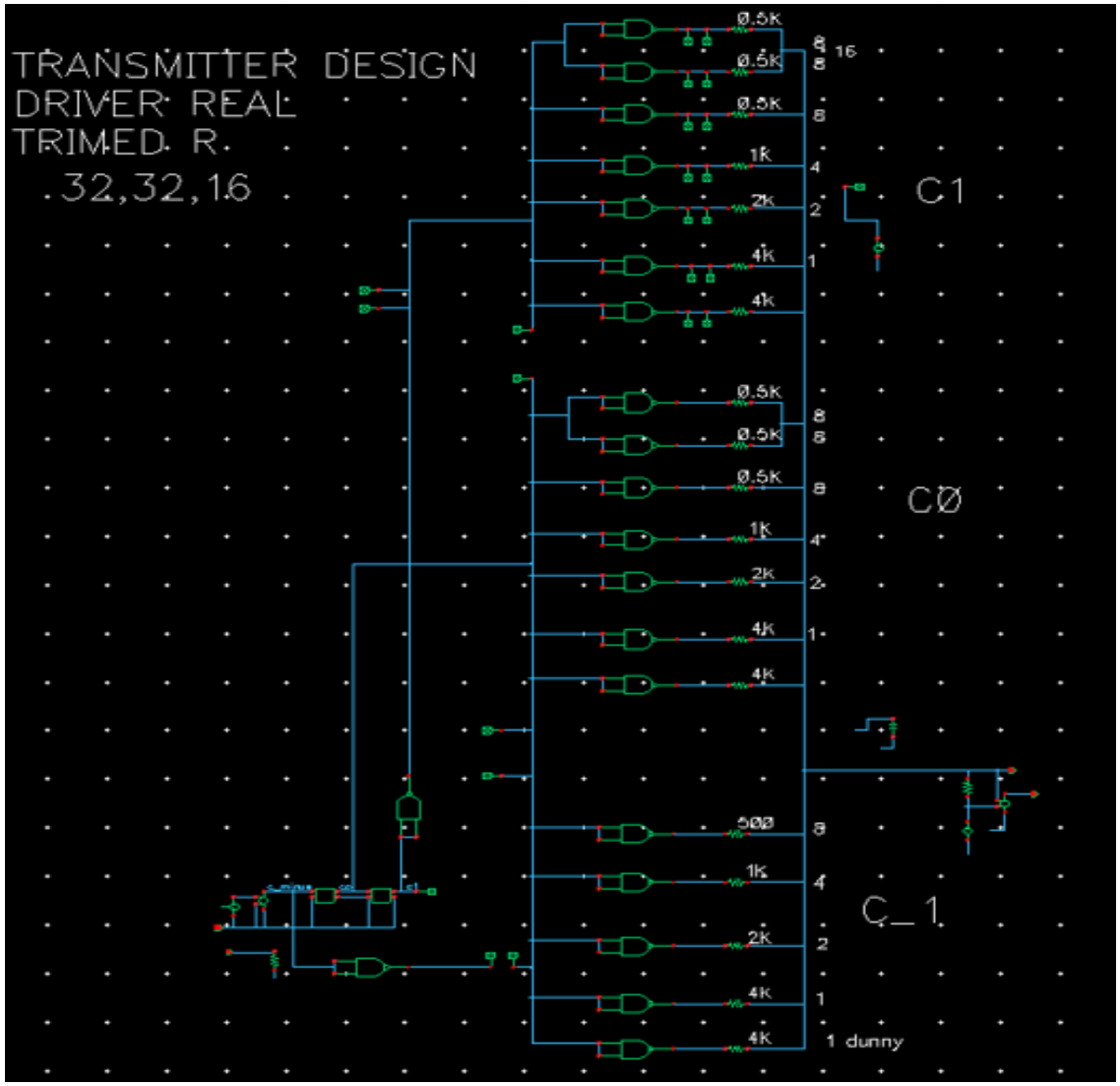
We pay in amplitude sum of R=50 oms

How does equalization work ?



Tx output view
if no capacitance
Z-1 and Z-2

Real v-mode driver



This controls all coef.

And keep 50 ohm looking back..

Resulting eye : heavy burden on Z-1..= effective ampl. down

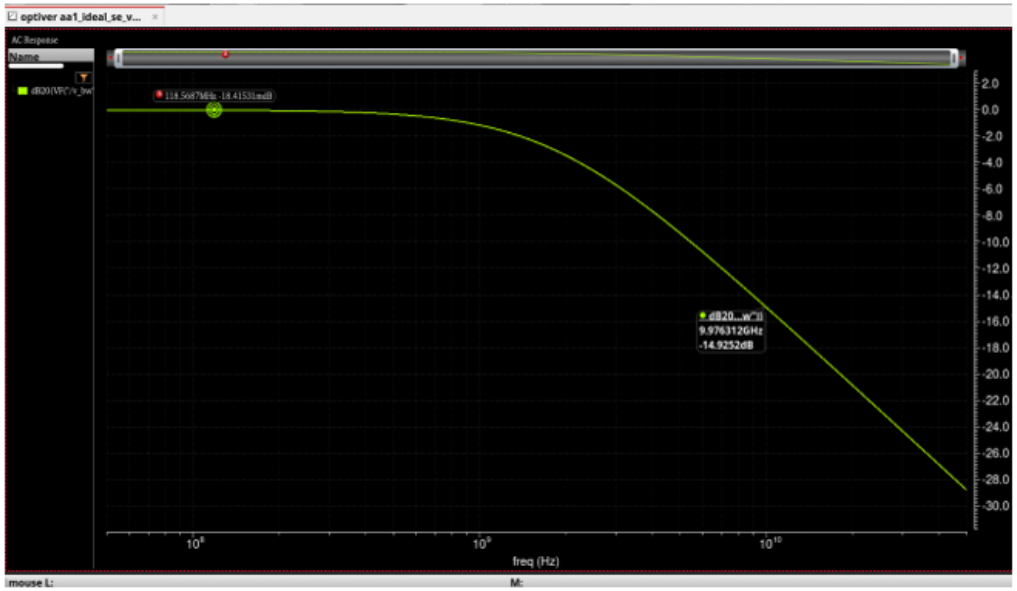


Figure 32: Loss in a 20cm line using simple RC filer: AC analysis

20cm line TF for 10gbit data
-15dB at 10Ghz

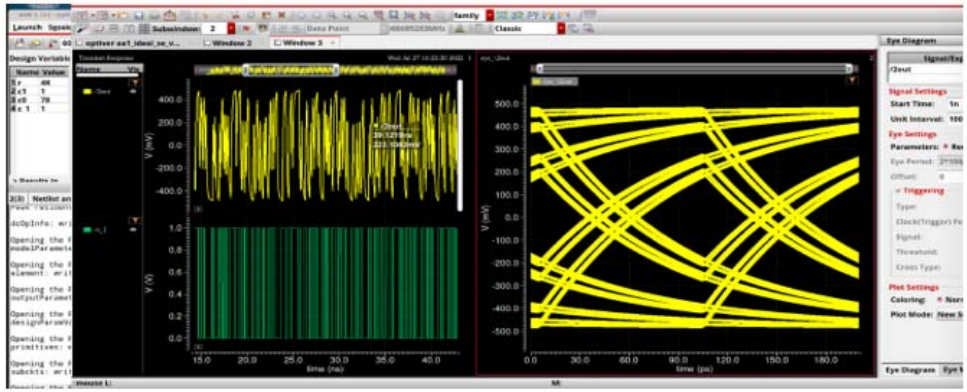


Figure 33: First run non equalized line

Second run with equalization using C1 showing, in red color, is how the line is equalized better.

	Name	
1	r	4K
2	c1	19
3	c0	60
4	c 1	1

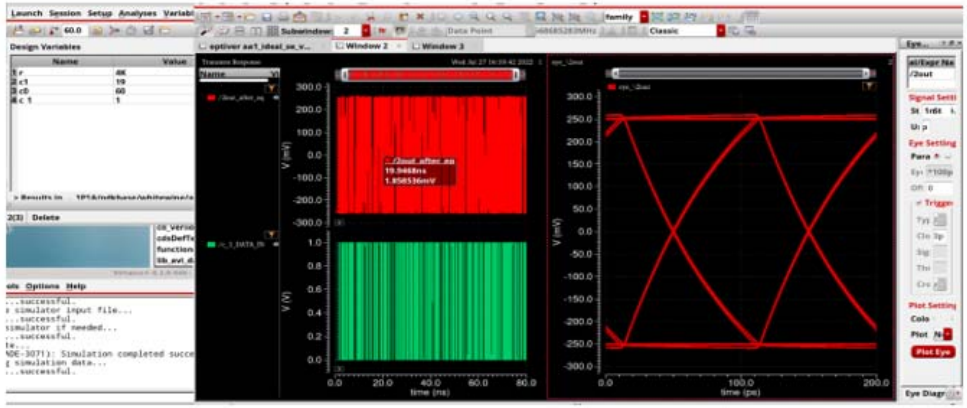
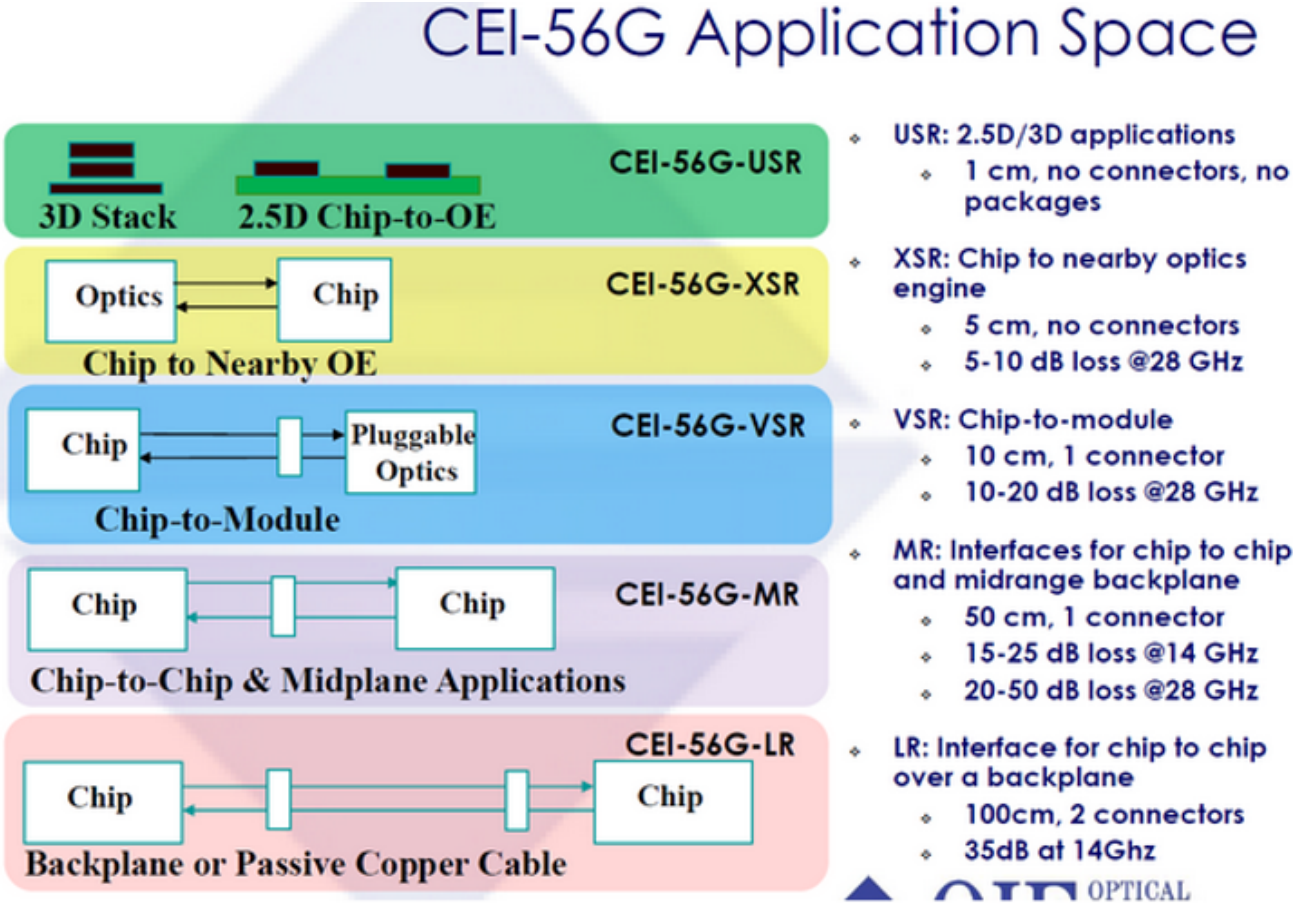


Figure 34: Second run with equalization using C1

Line length and applications



1m “KR” is also challenge

Line model

The basic equations governing the line shown below.

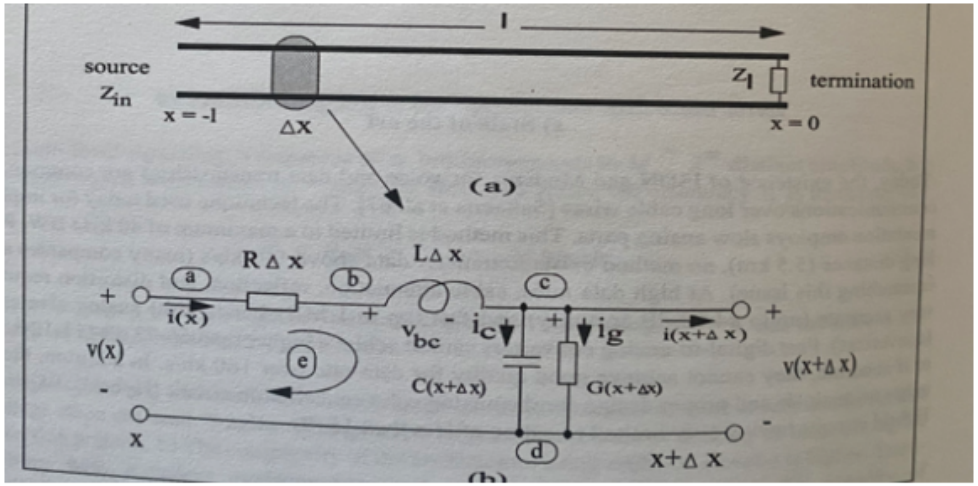


Figure 28: a uniform transmission line b) lumped parameters

Break the line to segments.

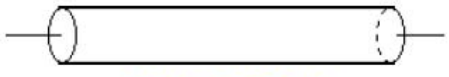
$$\frac{\partial^2 v}{\partial x^2} = RGv + (RC+LG)\frac{\partial v}{\partial t} + LC\frac{\partial^2 v}{\partial t^2}$$

$$\frac{\partial^2 i}{\partial x^2} = RGi + (RC+LG)\frac{\partial i}{\partial t} + LC\frac{\partial^2 i}{\partial t^2}$$

The solution of this model gives the famous *Telegraph equations*

Cable Model

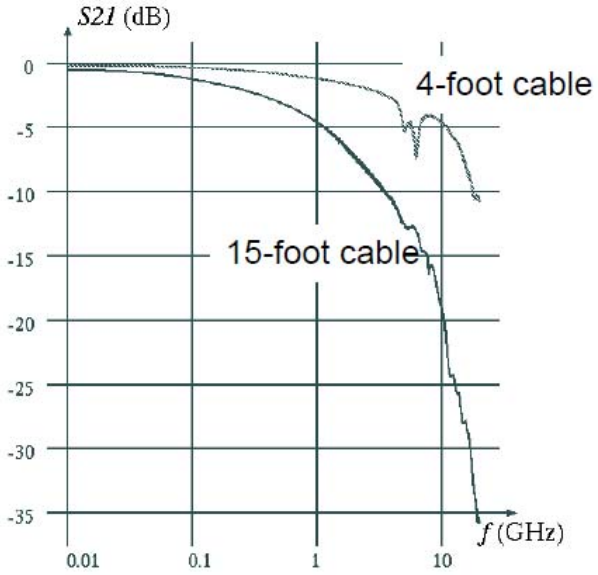
Copper Cable Model

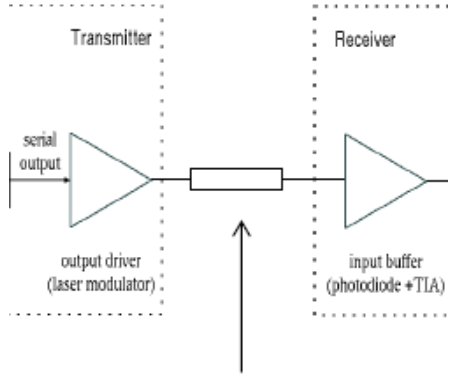


Copper Cable

$$|H(\omega)| \approx e^{-L\alpha\sqrt{\omega}}$$

Where: L is the cable length
a is a cable-dependent characteristic





Channel
(copper or fiber)

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results

The magnitude response solution of those equations assuming matched line

$$|H(f,l)| = e^{-l\alpha(f)} = e^{-Kl\frac{\sqrt{\pi f/2}}{Z_0}}$$

The above is true if:

$$Z_{in} = Z_0 \cong \sqrt{\frac{L}{C}}$$

$$|H(f,l)|_{dB} = -0.016 \cdot l \cdot \sqrt{f}$$

Eq. 1: Line response in dB the constant -0.016 is only related to cable.

CONCLUSION

Key **Rule of Thumb:**

In dB the Insertion loss double if we double the distance

In dB the Insertion loss double in frequency (actually as SQRT(f))

Latency is 30cm=1ns (in air but in FR-4 it's about 2ns.

A LOSS of about 2"/dB for FR-4 at 10GHz.

Double the length half the amplitude
Double f (at low f) not so steep
Double f (at high f) close to the amplitude

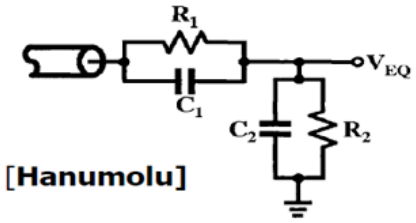
Receiver

Receiver front: terminations, equalization, vga.

Rx equalization.

Passive CTLE

- Passive structures offer excellent linearity, but no gain at Nyquist frequency



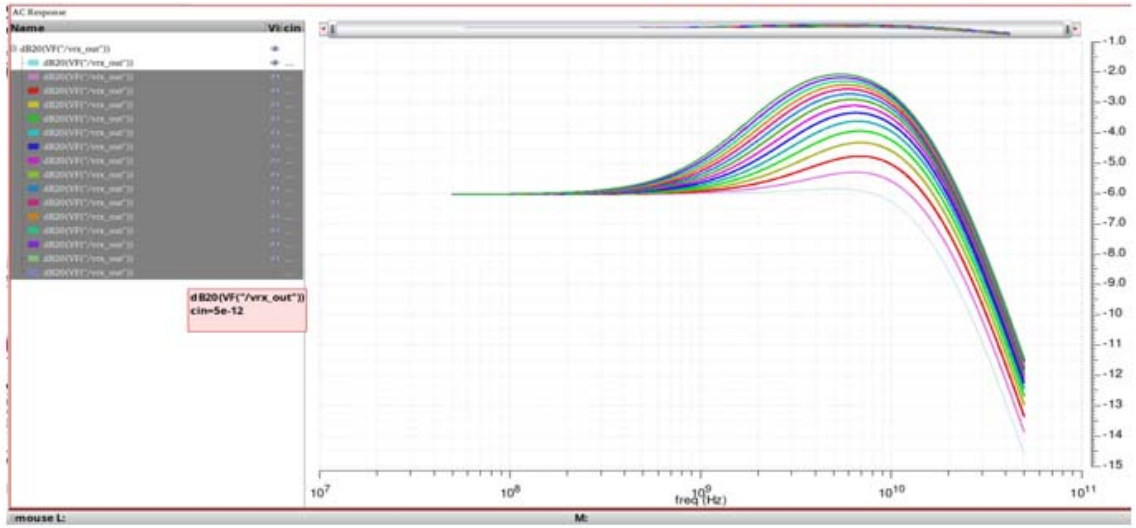
[Hanumolu]

$$H(s)=\frac{R_2}{R_1+R_2}\frac{1+R_1C_1s}{1+\frac{R_1R_2}{R_1+R_2}(C_1+C_2)s}$$

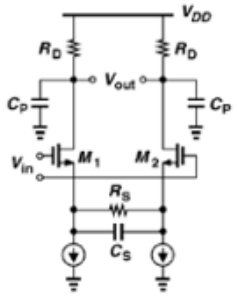
$$\omega_z=\frac{1}{R_1C_1},\qquad \omega_p=\frac{1}{\frac{R_1R_2}{R_1+R_2}(C_1+C_2)}$$

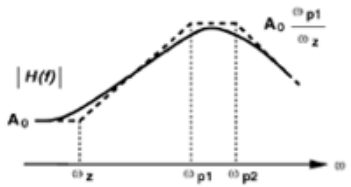
$$\textbf{DC gain}=\frac{R_2}{R_1+R_2},\quad \textbf{HF gain}=\frac{C_1}{C_1+C_2}$$

$$\textbf{Peaking}=\frac{\textbf{HF gain}}{\textbf{DC gain}}=\frac{\omega_p}{\omega_z}=\frac{R_1+R_2}{R_2}\frac{C_1}{C_1+C_2}$$



[Gondi JSSC 2007]





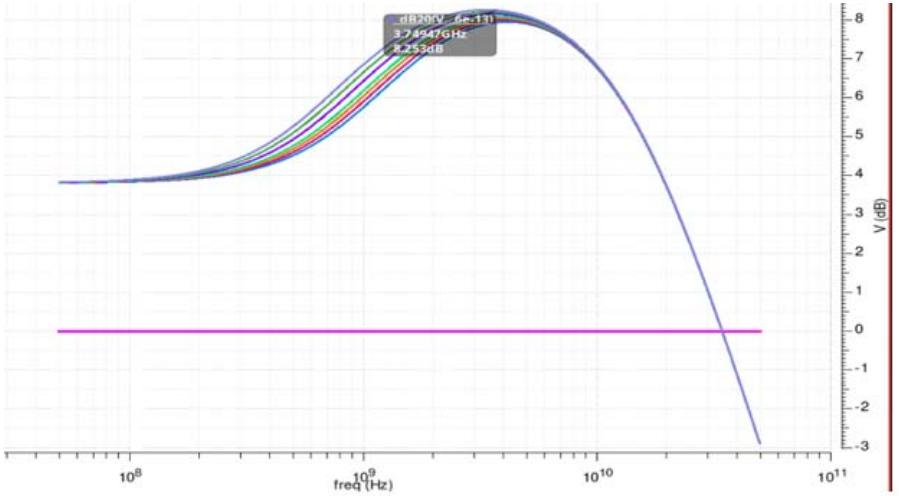
$$H(s) = \frac{g_m}{C_P} \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + g_m R_S/2}{R_S C_S}\right)\left(s + \frac{1}{R_D C_P}\right)}$$

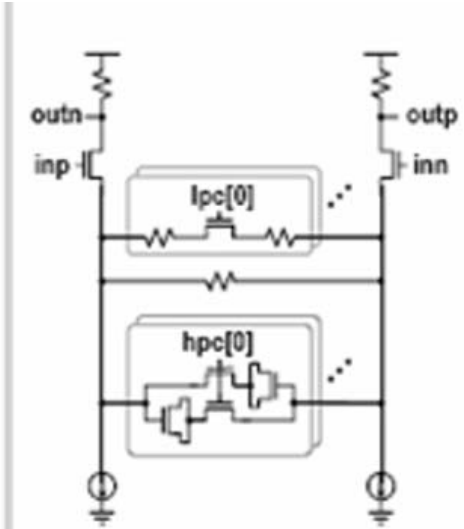
$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{p1} = \frac{1 + g_m R_S/2}{R_S C_S}, \quad \omega_{p2} = \frac{1}{R_D C_P}$$

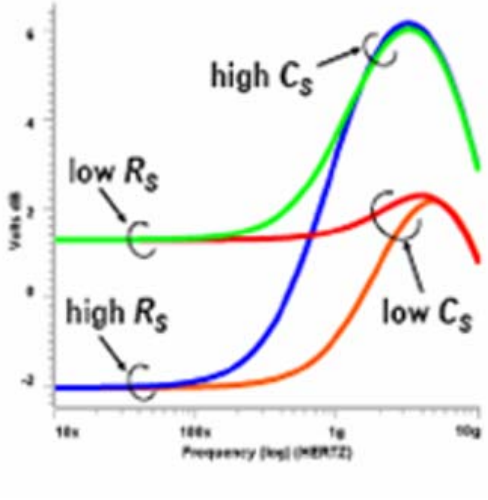
$$\text{DC gain} = \frac{g_m R_D}{1 + g_m R_S/2}, \quad \text{Ideal peak gain} = g_m R_D$$

$$\text{Ideal Peaking} = \frac{\text{Ideal peak gain}}{\text{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_S/2$$

14



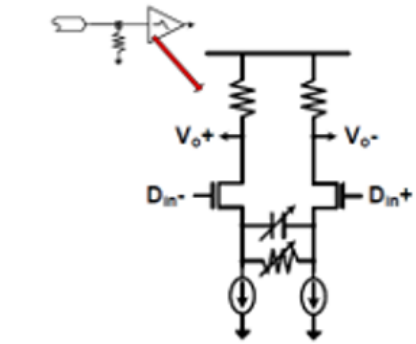


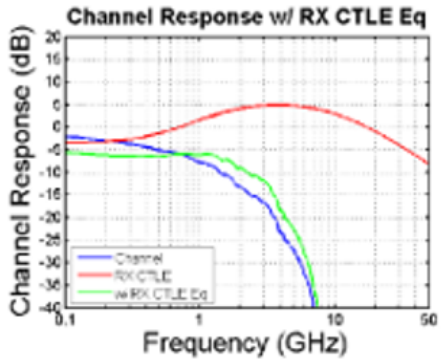


More equalization in Rx- active CTLE

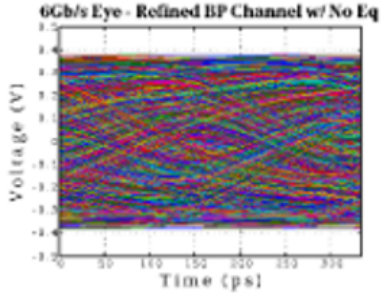
Active CTLE

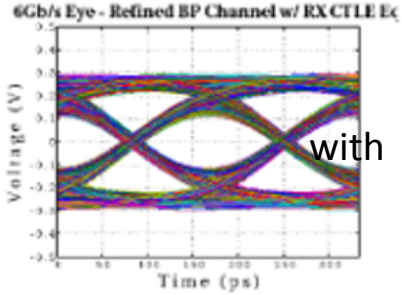
Below shown a high pass linear filter used as a CTLE. 2 transistors to convert the voltage input to current injected into the Vo+ and Vo-. Are used. The sources of the two transistors now uses a filter R and C which can be though as impedance varying in frequency. This *open loop* amplifier has a gain and Band width all related to the load resistance and the source filter.





without



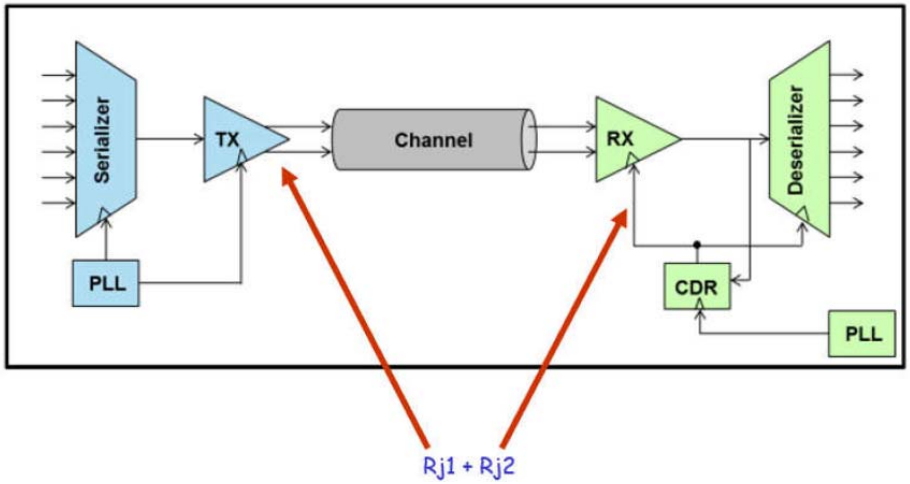


with

CDR

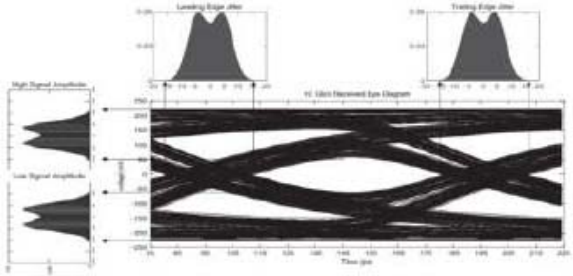
Already reviewed it basics ..

So lets just go over jitter..and..BER



PLL BERs and Jitter..

- Jitter at a given BER is computed considering both leading and trailing edges



$$BER_{total}(t) = 0.5\left[erfc\left(\frac{t - DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right) + erfc\left(\frac{t + DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right)\right],\quad BER_{trans}(t) = 0.5\left[erfc\left(\frac{UI - t - DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right) + erfc\left(\frac{UI}{\sqrt{2}\sigma_{RJ}}\right)\right]$$

where $erfc(t) = \frac{2}{\sqrt{\pi}}\int_{t}^{\infty} e^{-x^2} dx$

TABLE 13-1. Q_{BER} as a Function of the Bit Error Rate

BER	Q_{BER}	BER	Q_{BER}	BER
1×10^{-3}	6.180	1×10^{-10}	12.723	1×10^{-17}
1×10^{-4}	7.438	1×10^{-11}	13.412	1×10^{-18}
1×10^{-5}	8.530	1×10^{-12}	14.069	1×10^{-19}
1×10^{-6}	9.507	1×10^{-13}	14.698	1×10^{-20}
1×10^{-7}	10.399	1×10^{-14}	15.301	1×10^{-21}
1×10^{-8}	11.224	1×10^{-15}	15.882	1×10^{-22}
1×10^{-9}	11.996	1×10^{-16}	16.444	7.7×10^{-24}

(Random J *Qber)+DJ

System Jitter Budget

- For a system to achieve a minimum BER performance

$$UI \geq DJ_{\delta\delta}(sys) + Q_{BER}\sigma_{RMS}(sys)$$

- The convolution of the individual deterministic jitter components is approximated by linear addition of the terms

$$DJ_{\delta\delta}(sys) = \sum_{i} DJ_{\delta\delta}(i)$$

- The convolution of the individual random jitter components results in a root-sum-of-squares system rms value

$$\sigma_{RMS}(sys) = \sqrt{\sum_{i} \sigma_{RMS}^{2}(i)}$$

be careful: what is the relations of phase noise to Jitter ?- integral..

Figure 45: BER and Jitter relations

Data comes with Tx jitter +Tx. buffer+CTLE And Recovered clock from CDR Clock (VCO+shaped).

- For a system to achieve a minimum BER performance

$$UI \geq DJ_{\delta\delta}(sys) + Q_{BER}\sigma_{RMS}(sys)$$

SerDes pll budget

97 ps

10.3125Gbps

Margin=48.5 ps

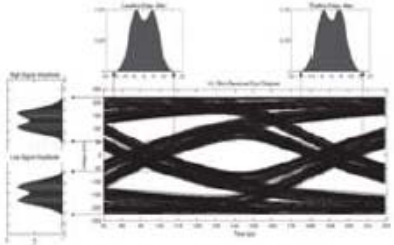
Min Data

CDR Clock

ckj=pll jiter rms per side

48.5ps=(14*2ckj)+12ps(ISI)+8ps(set/hold)+10ps(unsymerty)

- Jitter at a given BER is computed considering both leading and trailing edges



$$BER_{-}(t) = 0.5\left[\operatorname{erfc}\left(\frac{t - DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right) + \operatorname{erfc}\left(\frac{t + DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right)\right],\quad BER_{+}(t) = 0.5\left[\operatorname{erfc}\left(\frac{UI - t - DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right) + \operatorname{erfc}\left(\frac{UI - t + DJ_{\delta\delta}/2}{\sqrt{2}\sigma_{RJ}}\right)\right]$$

where $\operatorname{erfc}(x) = \frac{2}{\sqrt{\pi}}\int_{x}^{\infty} e^{-t^2}\,dt$

TABLE 13-1. Q_{BER} as a Function of the Bit Error Rate

BER	Q_{BER}	BER	Q_{BER}
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1×10^{-7}	10.399	1×10^{-14}	15.301
1×10^{-8}	11.224	1×10^{-15}	15.882
1×10^{-9}	11.996	1×10^{-16}	16.444

Solve for ckj-> PLL max jitter= 660fsx2=1.2ps
T say keep it under 400fs

E N D

And.. Good luck (with some hard work) on the project