Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 10

Over Sampling ADCs : Sigma Delta - Loops and Architectures

SNR CALCULATIONS

www.gigalogchip.com

Agenda

Sigma Delta –System Non Nyquist Converters

Why Over sample

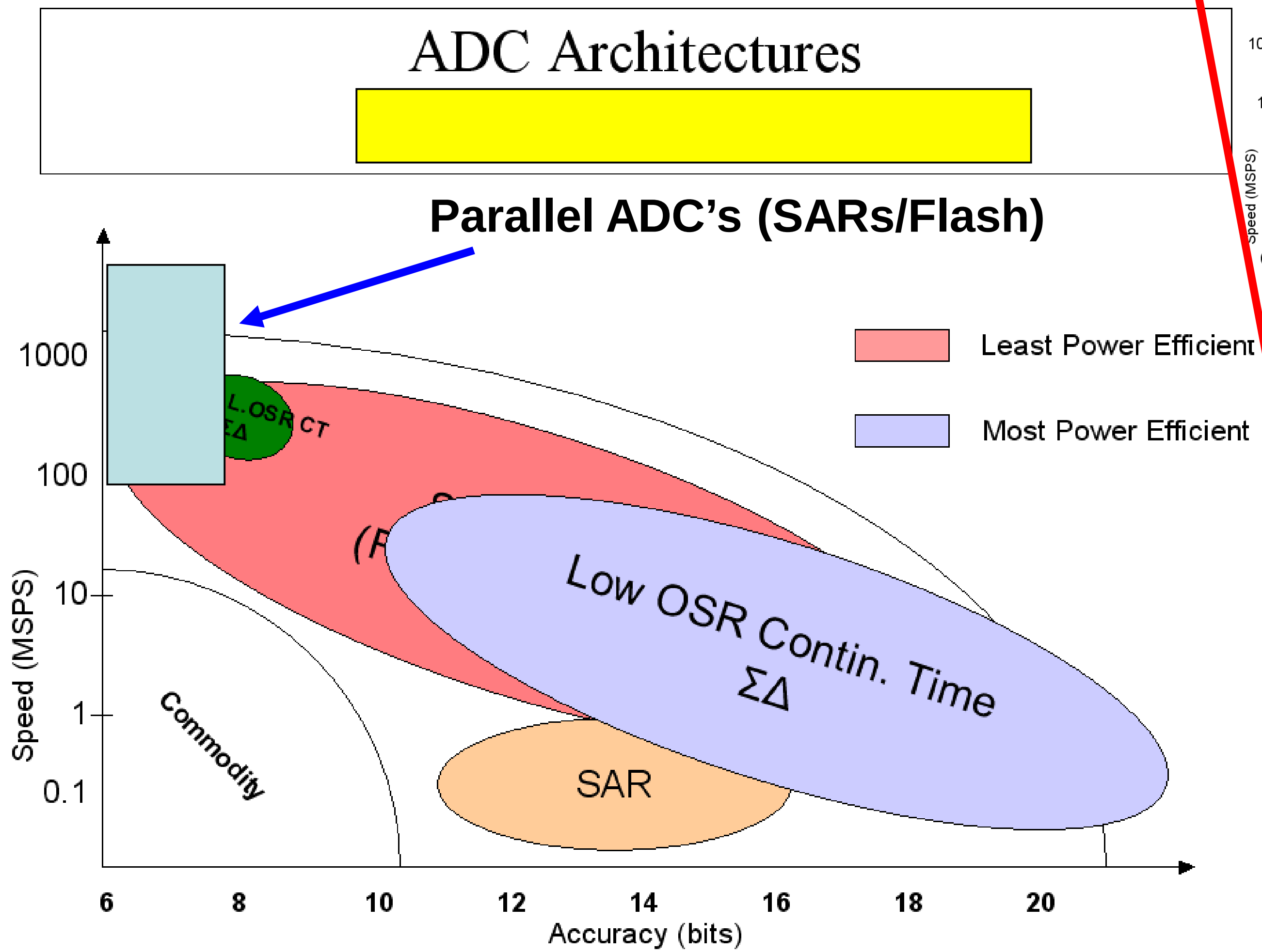
Basic Loops, Z transform

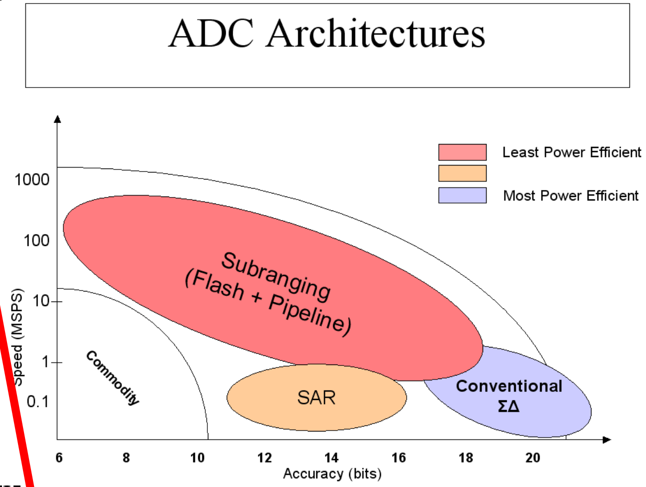
Noise Transfer

Multi-Loops

Multi Bit Multi Loops

SD- Location in the ADCs- >2002





Lecture 9
ADC's 'before 2002'

BASIC SD LOOP

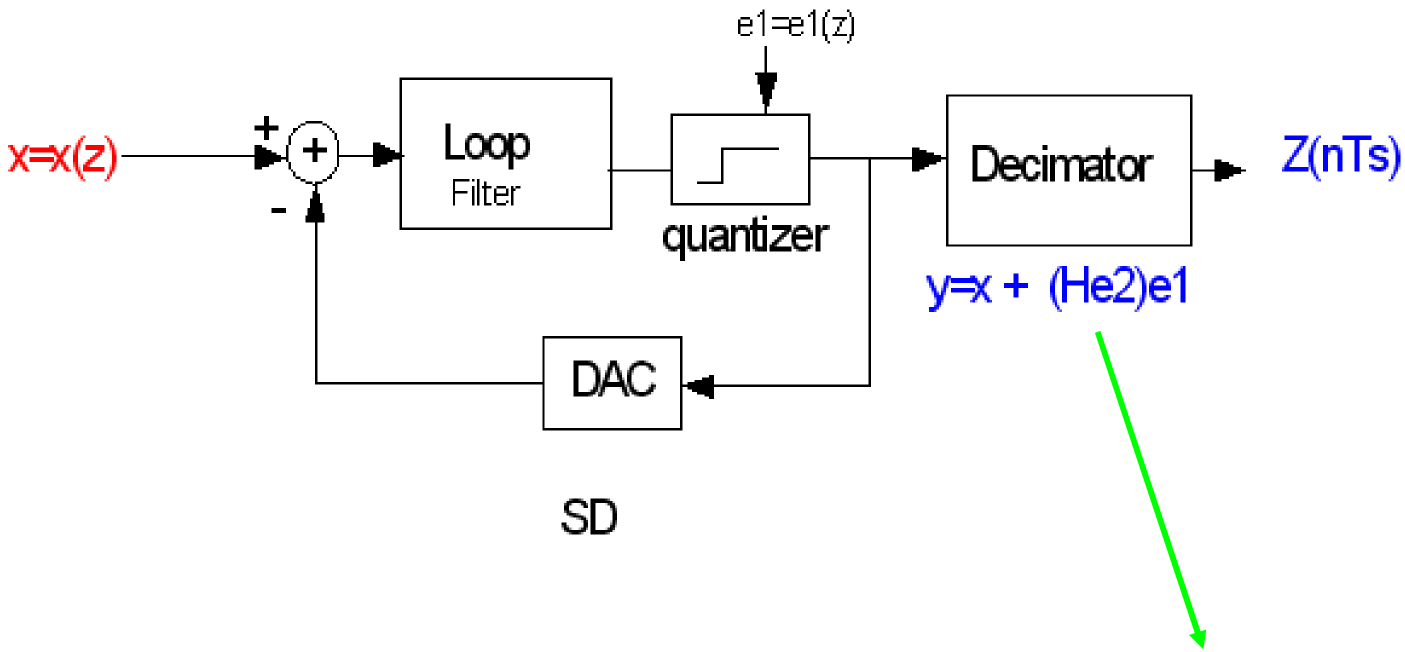


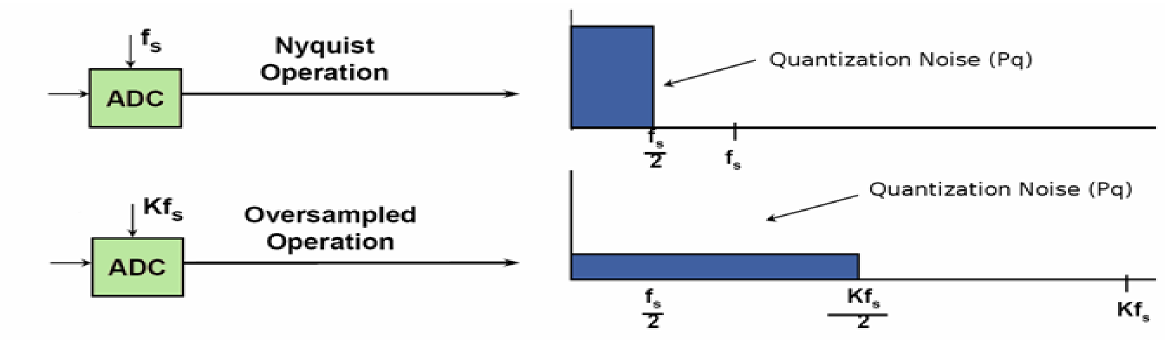
Figure out He2

Why Over sample

MAIN OLD RESON LINEARITY IS INFINITE!

Quantization Noise

Nyquist vs Over-sampling Operation



∑-Delta architectures use oversampling; Normally, pipeline architectures do not

TRAIDING DIGITIZING RATE FOR BITS TO GET EQUAL QUANTIZATION NOISE IN A FIXED BAND

SNR INCREASE ===> f (10 log fs1/fs2)
2x→ 10log2= 3dB

SNR AND OVERSAMPLING

When the noise is shaped equally (quantization noise)
2 x fs – Half noise power increase in SNR by 3dB
4 x fs - same as 1 bit performance increase
N x fs – 10log(n) increase in performance

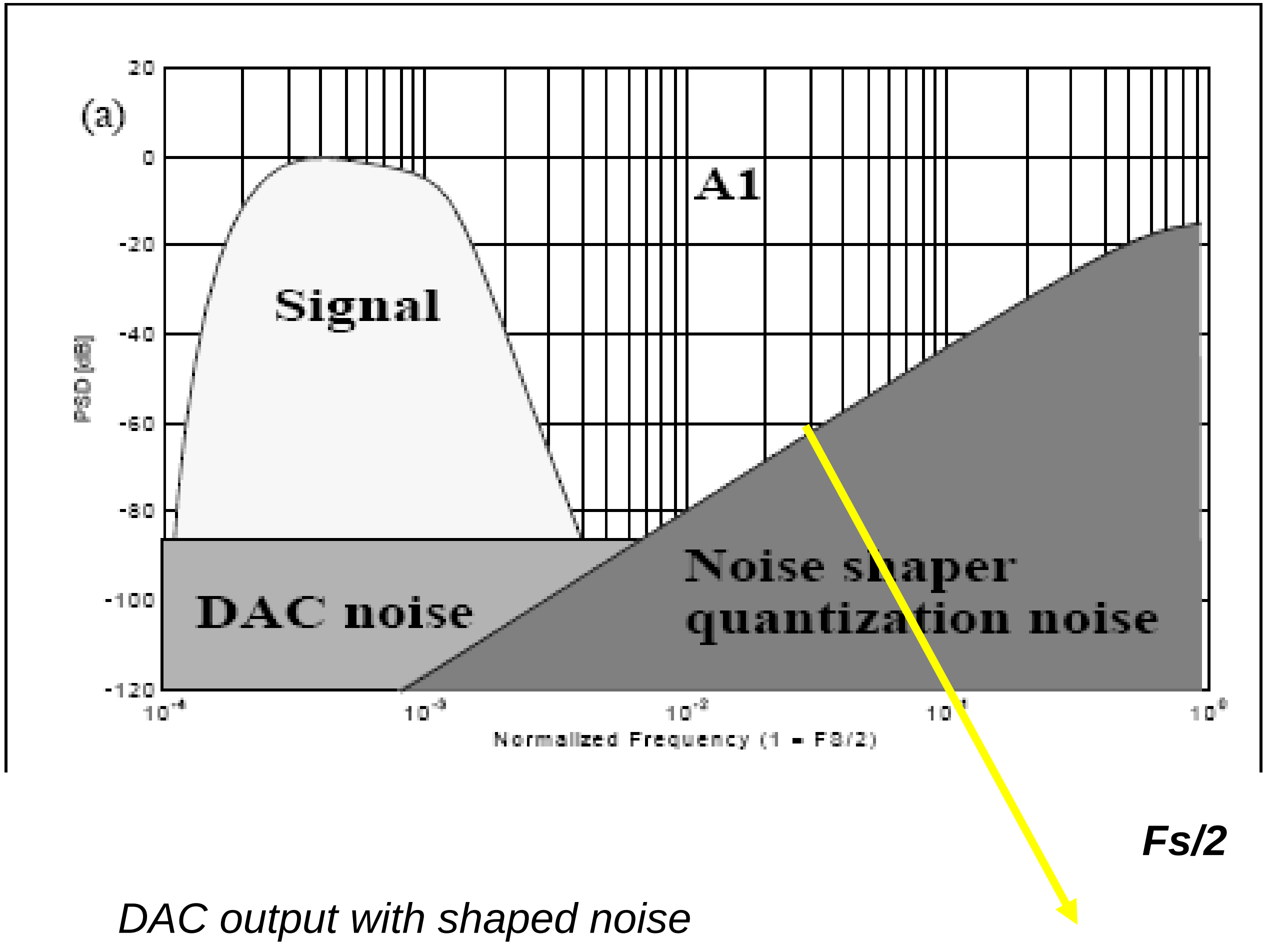
Example:
Use 8 bit converter over sample by 16 get 10 bit SNR

But is it the best we can do?

Poor return on investment
(clock frequency increased - if noise spread equally

Can we shape the noise in band ?

Can we shape the noise ?



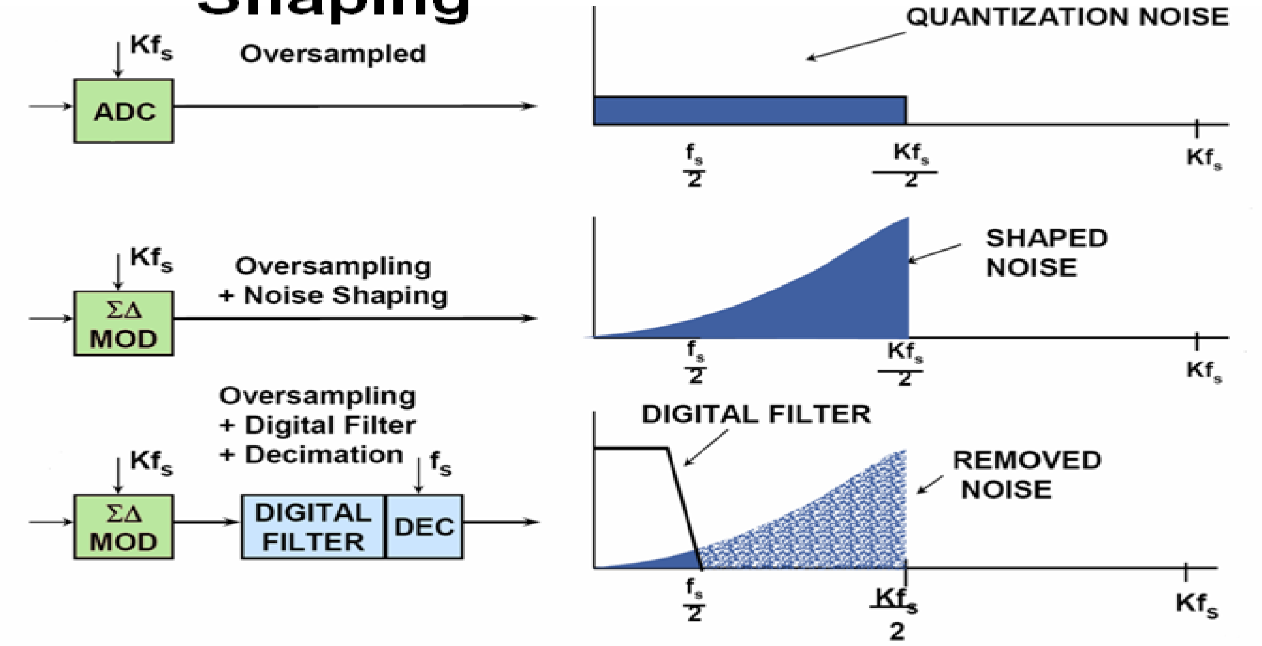
Fs/2

DAC output with shaped noise
(same for adc shaped digital noise)

We may need analog filter..

Quantization Noise

The benefits of Noise Shaping



We will need digital filter..

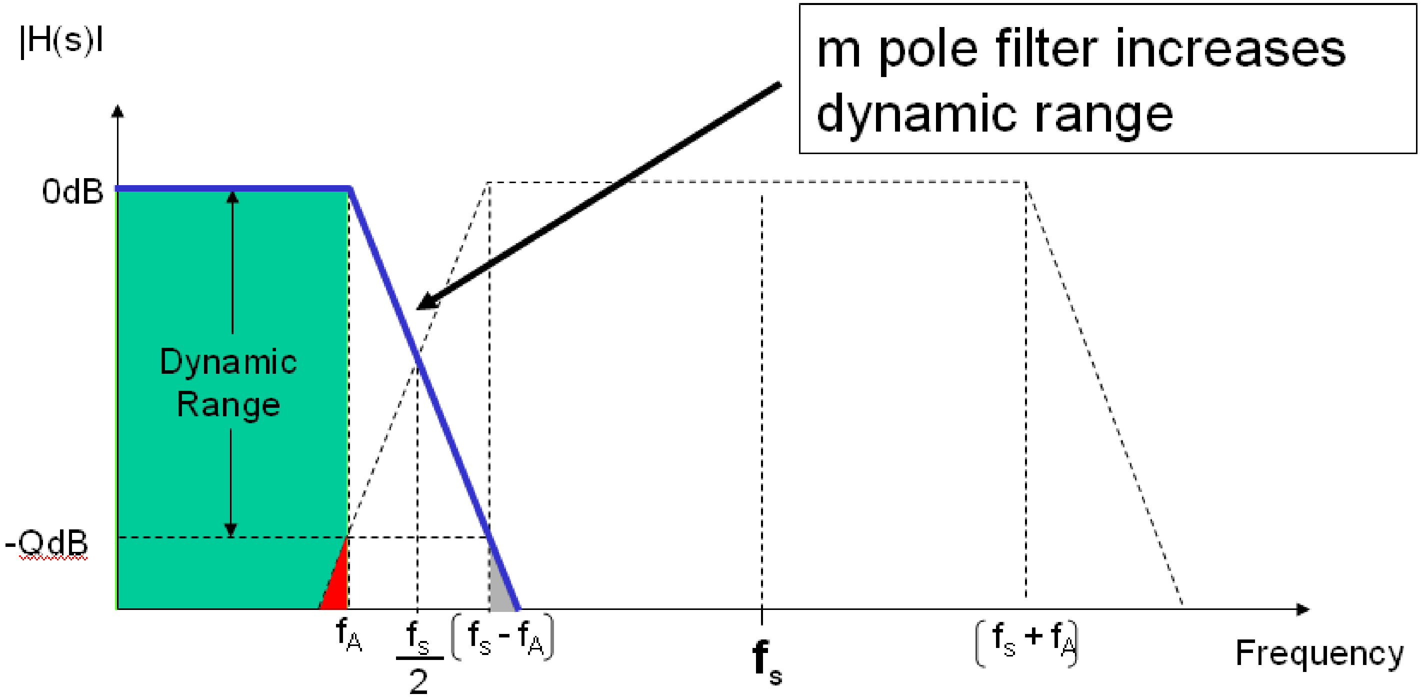
Additional why's…
Sigma Delta Converter "love digital noise"..

Anti-alias filter relaxed
No S/H- Reduced analog block requirements
Easy re design for new technology, Low Voltage design
Low power- Good FOM
Fewer DAC bits

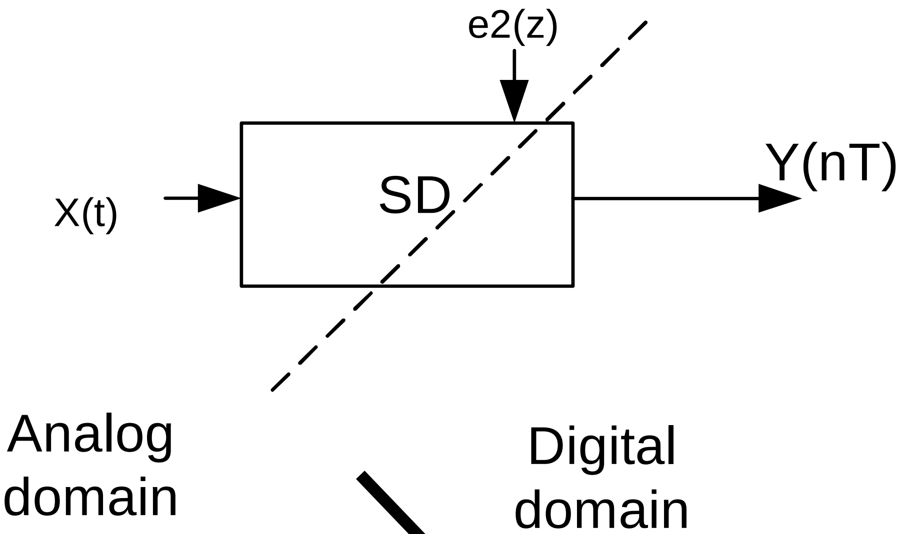
But, the minuses are: a feed back path, amplifiers..
and over sampling needed..

Nice: DONT FORGET WE CAN GET INFINITE LINEARITY !
But… Need much faster sampling clock

Relaxed Input Filter



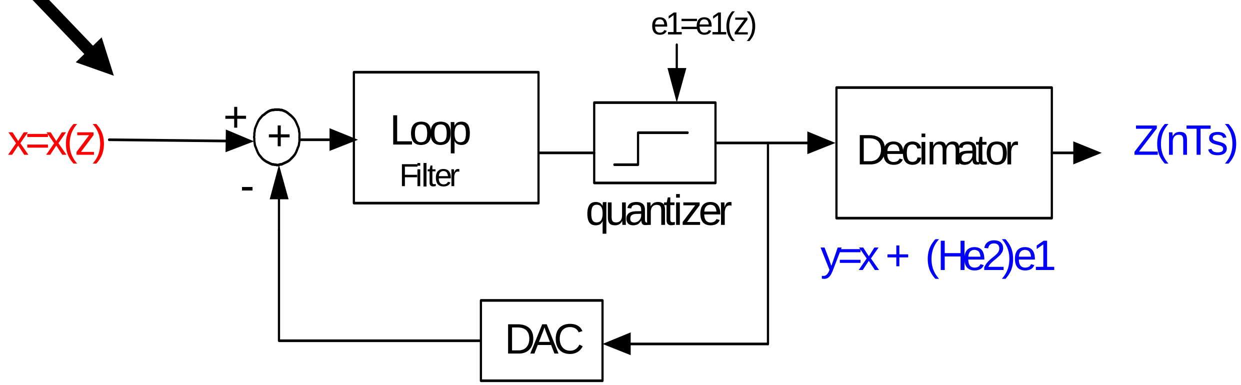
Basic Loop- how does it work



No more open loop: stability must be watched for

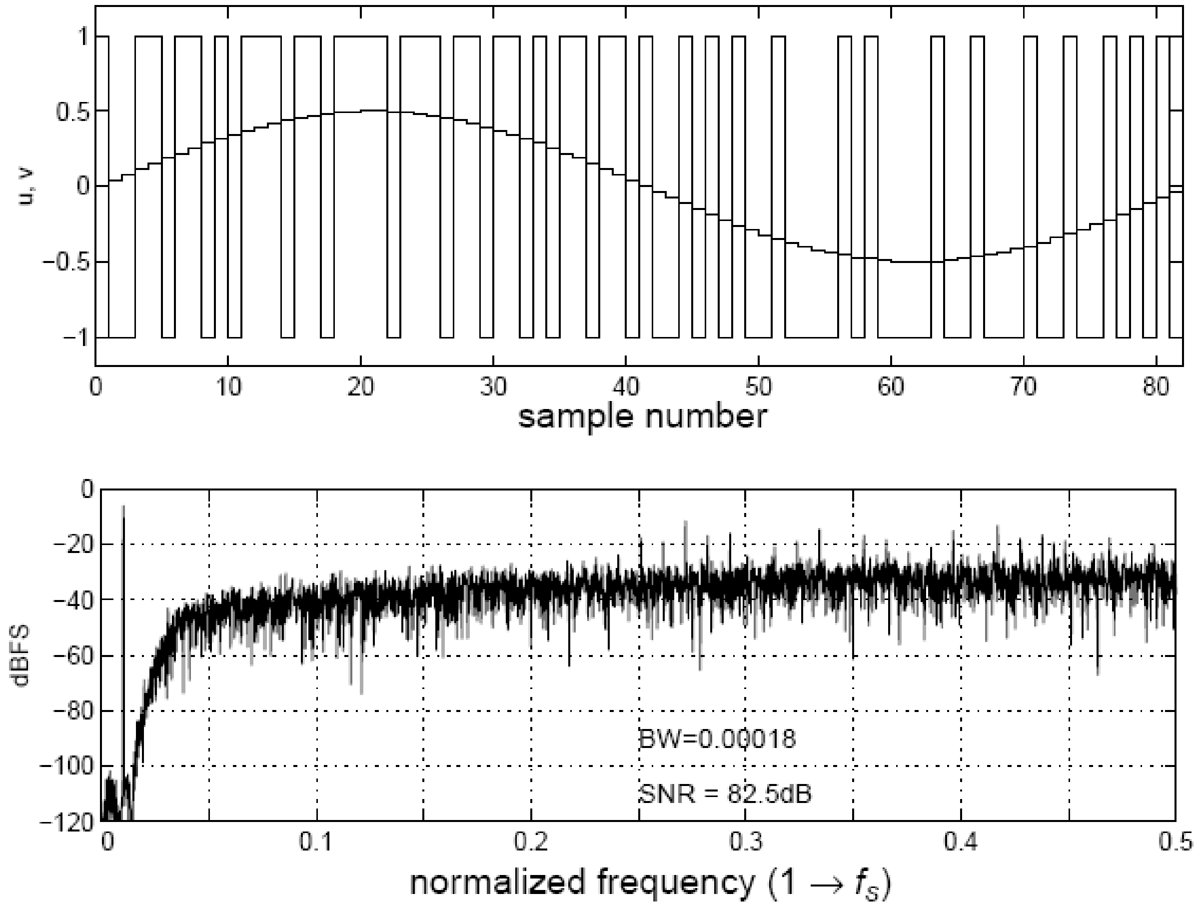
Clocked at 2 places at least.

Place the quantizer with filtering inside the ADC loop. What is a good loop filter? why?



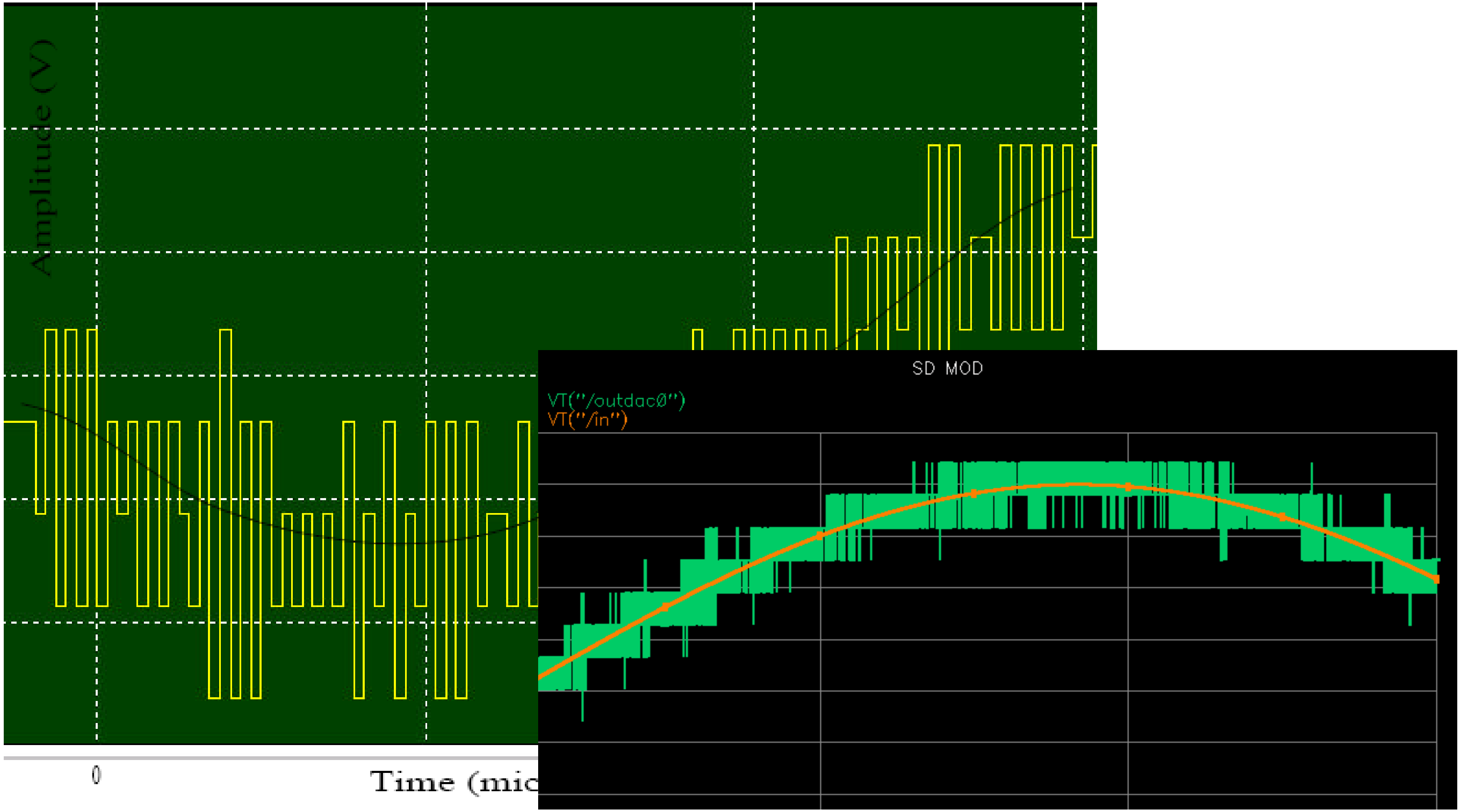
BASIC SD LOOP

Example Simulation



Example 2 - Multi bit SD- adc

Time domain multi bit over sample converter
(converting digital bits to levels..)

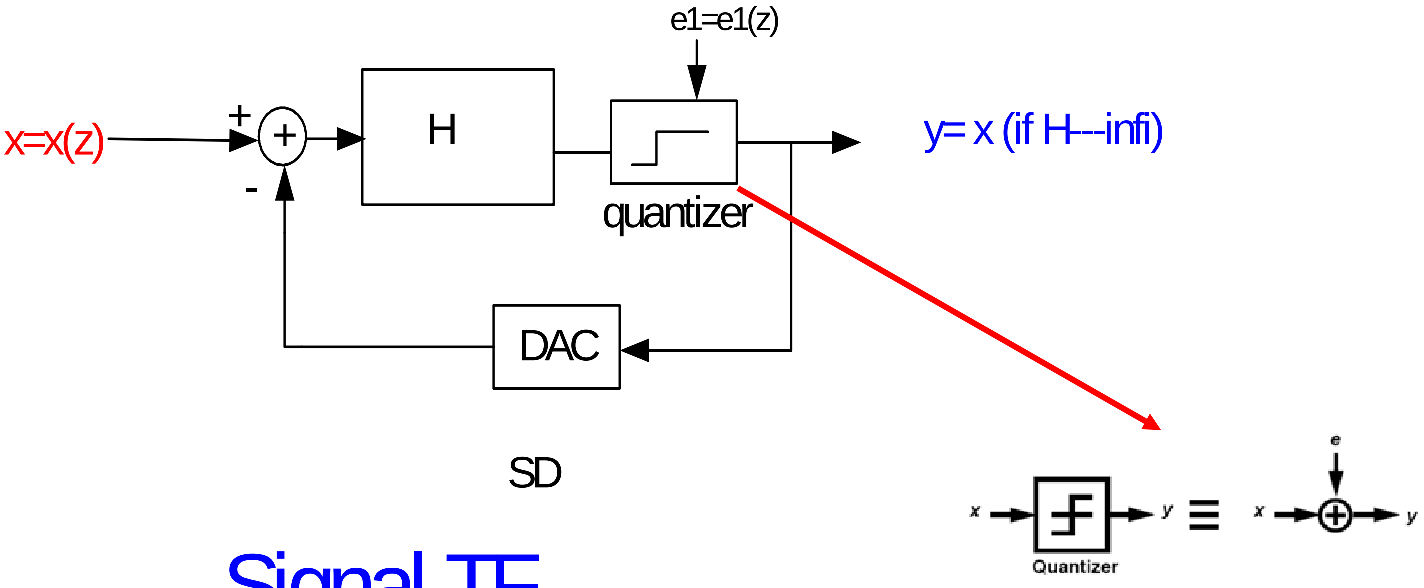


NEXT :

Analyze SD structures, review few loops and..

HOW TO CALCULATE LOOP QUALITY: SNR

Basic SD T. Function

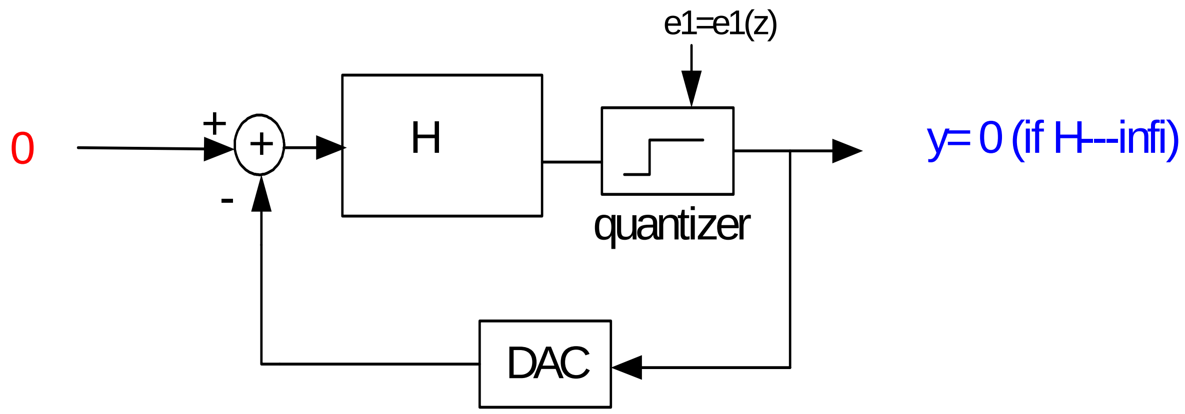


Signal TF

Can be 1 comparator (covered Lecture 8
Can be set of comparators- Flash ADCs

Vout/Vin = H / 1 + H

if H (v. large) goes to infinite T.F = 1



SD

Noise (quant) TF

Vout/Vin = 1 / 1 + H

about the filter H

Let's assume its good to use an integrator in the loop

SD can be implemented using time continuous filters (integrators) but also using switch capacitor- discrete time..

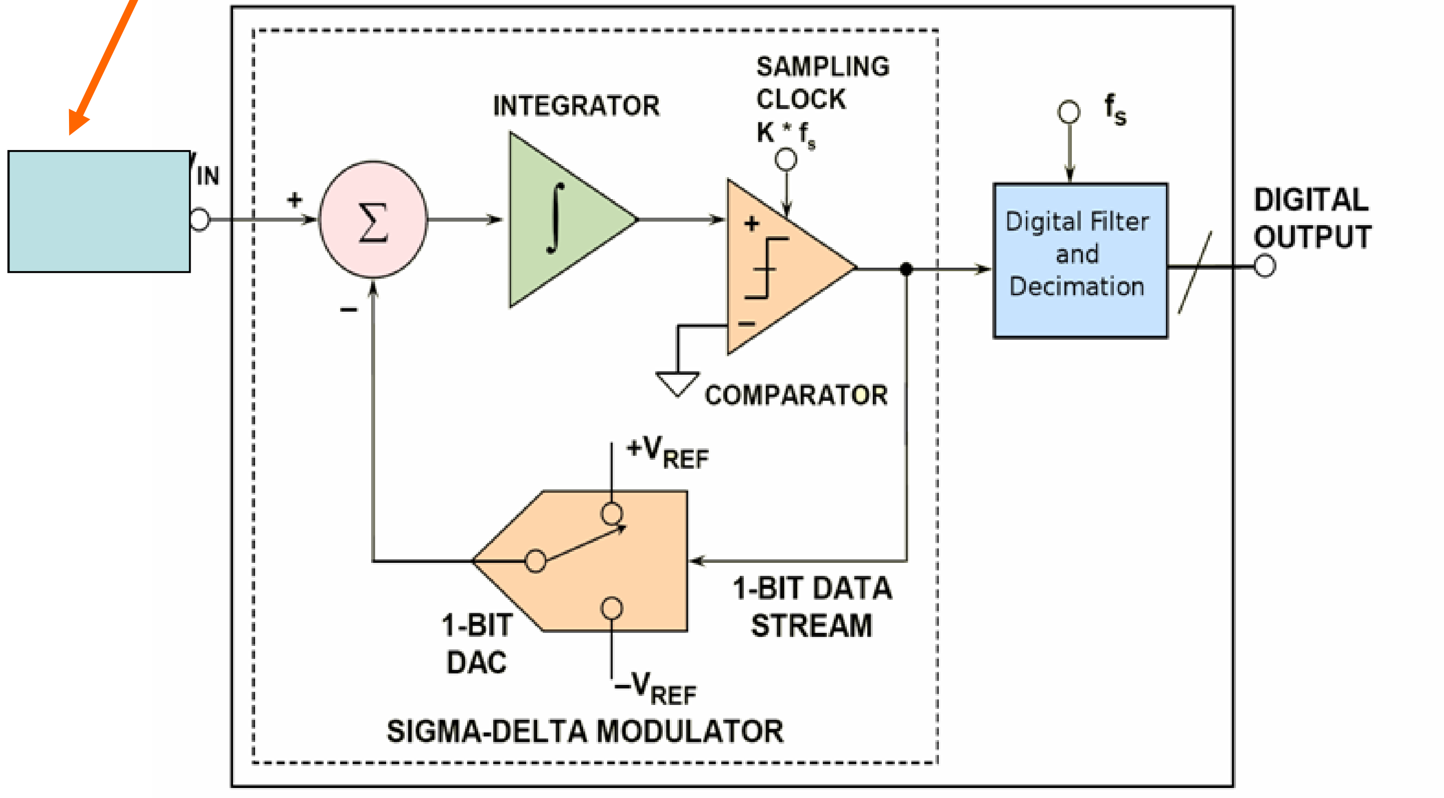
To further study of SD I will switch back and force from time domain to Discrete domain- some calculations are easier to explain in one domain or the other.

Look first at analog sigma delta simple 1 loop

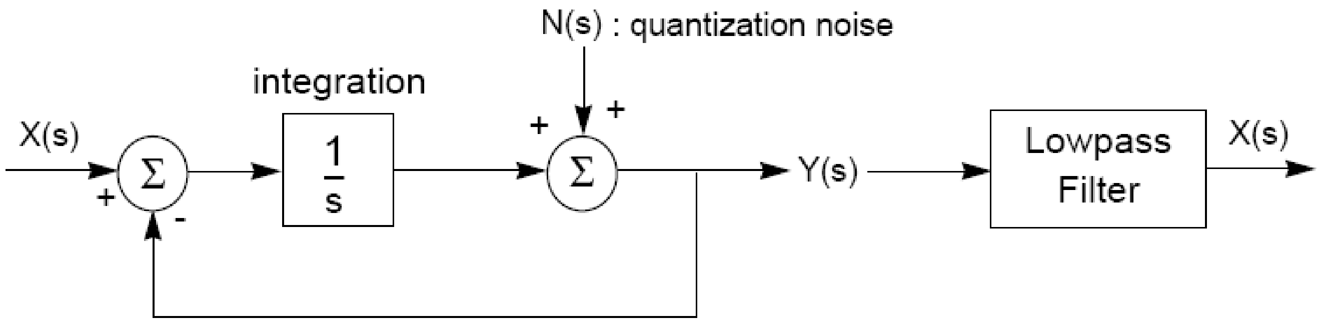
CT- ΣΔ ADC

Simple filter here

Block diagram



SD analog model for TF

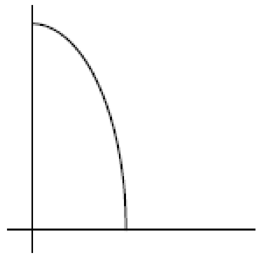


Integrator in open loop is LPF
In closed loop

Signal Transfer Function: (when N(s) = 0)

$$Y(s) = [X(s) - Y(s)]\ \frac{1}{s}$$

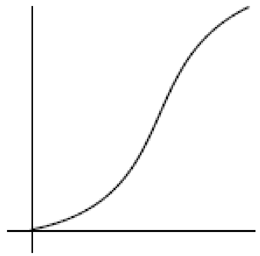
$$\frac{Y(s)}{X(s)} = \frac{\frac{1}{s}}{1 + \frac{1}{s}} = \frac{1}{s+1}$$: lowpass filter



Noise Transfer Function: (when X(s) = 0)

$$Y(s) = -Y(s)\frac{1}{s} + N(s)$$

$$\frac{Y(s)}{N(s)} = \frac{1}{1 + \frac{1}{s}} = \frac{s}{s+1}$$: highpass filter

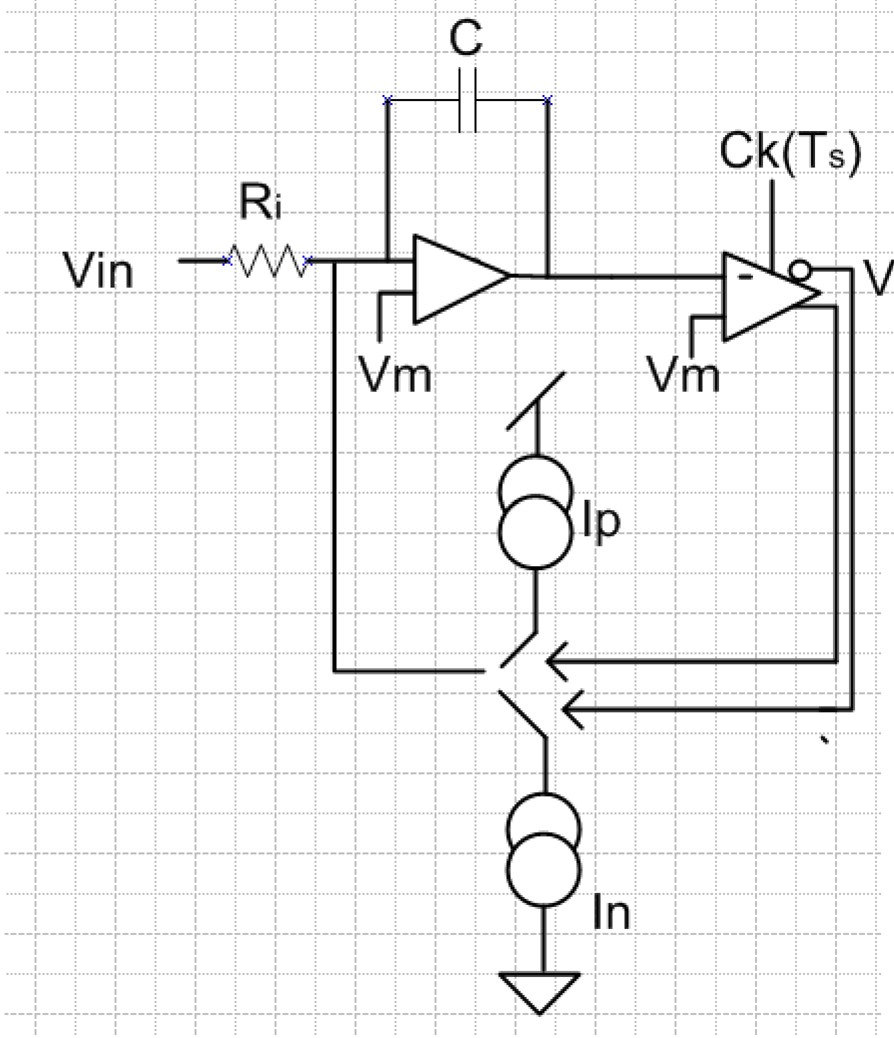


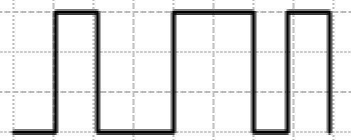
But the story is a bit more complicated:
Loop delay, DAC TF is not constant

Noise is H passed shaped

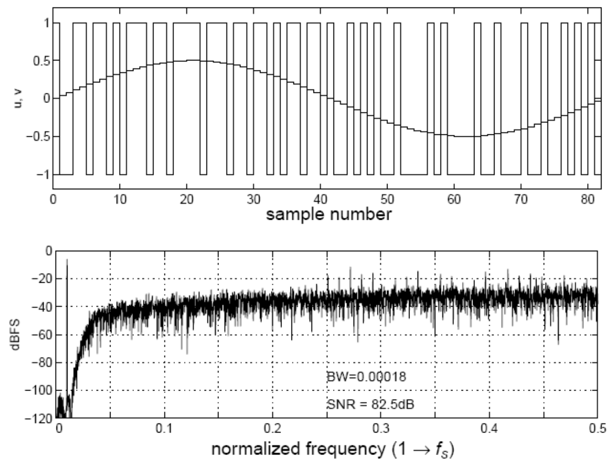
SD continuous analog blocks

Detail design example in lect11





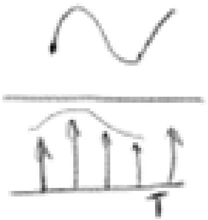
Example Simulation



SD - Noise analysis Vs. loop order

SUMMARY → Z TRANSFORMATION

1) TAKE $f(t)$



$f(t)$

2) CREATE $f^*(t)$ $\quad f^*(t) = f(t)\sum_{k=0}^{\infty} \delta(t-kT)$

3) TAKE Laplace Transform of $f^*(t) = F^*(s) = \sum_{k=0}^{\infty} f(kT)e^{-kT}$

4) Replace S by $\frac{1}{T}\ln(z)$

IF $z \triangleq e^{Ts} = e^{j\omega T} \Rightarrow F(z) = Z[f(t)] \triangleq F^*(s)\Big|_{s=\frac{1}{T}\ln z} = \sum_{k=0}^{\infty} f(kT)z^{-k}$

Transfer to distinct values- X(nT)

Differences eq. can be easily described:
Y(n) = X(n-1) + Y(n-1)

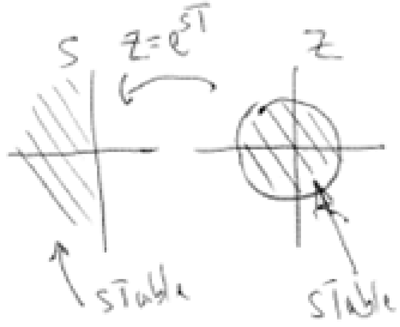
Quick look at Z domain

$s = \frac{1}{T}\ln z$

$f(t)$	$F(s)$	$F(z)$
$\delta(t)$	1	1
$u(t)$	$1/s$	$\frac{1}{1-z^{-1}}$
t	$\frac{1}{s^2}$	$\frac{Tz}{(z-1)^2}$
t^2	$\frac{2}{s^3}$	$\frac{Tz(z+1)}{(z-1)^3}$
e^{-at}	$\frac{1}{s+a}$	$\frac{z}{z-e^{aT}}$
$1-e^{at}$	$\frac{a}{s(s+a)}$	$\frac{z(1-e^{aT})}{(z-1)\,z-e^{aT}}$
a^t	$\frac{1}{s-\ln a}$	$\frac{z}{z-a}$

Integrator (→ $\frac{1}{1-z^{-1}}$)

← MOST IMPORT for SD.



$x(k) \xrightarrow{Z} X(z)$

$X(z) \rightarrow \boxed{z^{-M}} \rightarrow Y(z) = z^{-M}\cdot X(z)$

$x(k-m) \xrightarrow{Z} z^{-m}\, X(z)$

$a^k\, x(k) \xrightarrow{Z} X\left(\frac{z}{a}\right)$ scaling by a.

$k\, x(k) \xrightarrow{Z} -z\frac{dX(z)}{dz}$ $\left\{\begin{matrix} k<0 \\ x(k)=0 \end{matrix}\right\}$

FROM Z TO Difference equations

$$X(z) \longrightarrow \boxed{z^{-m}} \longrightarrow Y(z) = z^{-m} \cdot X(z)$$

$$x[k] \xrightarrow{z} X(z)$$

$$x[k-m] \xrightarrow{z} z^{-m} \cdot X(z)$$

Linearity Property

Given $x[k]$, $y[k]$, which are all zero for $k<0$.

Then:

$$x[k] \xrightarrow{z} X(z)$$
$$y[k] \xrightarrow{z} Y(z)$$

and:

$$\boxed{a \cdot x[k] + b \cdot y[k] \xrightarrow{z} a \cdot X(z) + b \cdot Y(z)}$$

"Multiplication by a^k" Property.

Given $x[k]$ where $x[k]=0$ for $k<0$ and a=constant

Then:

$$\boxed{a^k \cdot x[k] \xrightarrow{z} X\left(\frac{z}{a}\right)}$$

... corresponds to scaling by 'a' in the z-domain.

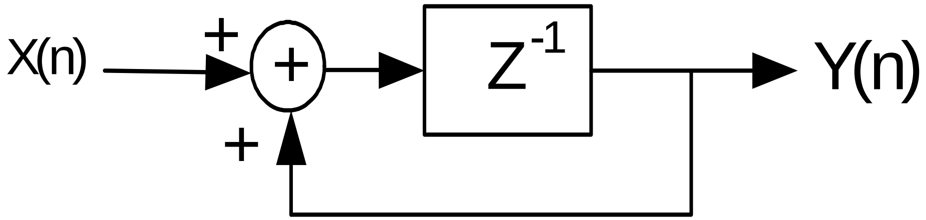
"Multiplication with k" Property

Given $x[k] = 0$ for $k<0$

Then:

$$\boxed{k \cdot x[k] \xrightarrow{z} -z \cdot \frac{dX(z)}{dz}}$$

From "z" to difference equations

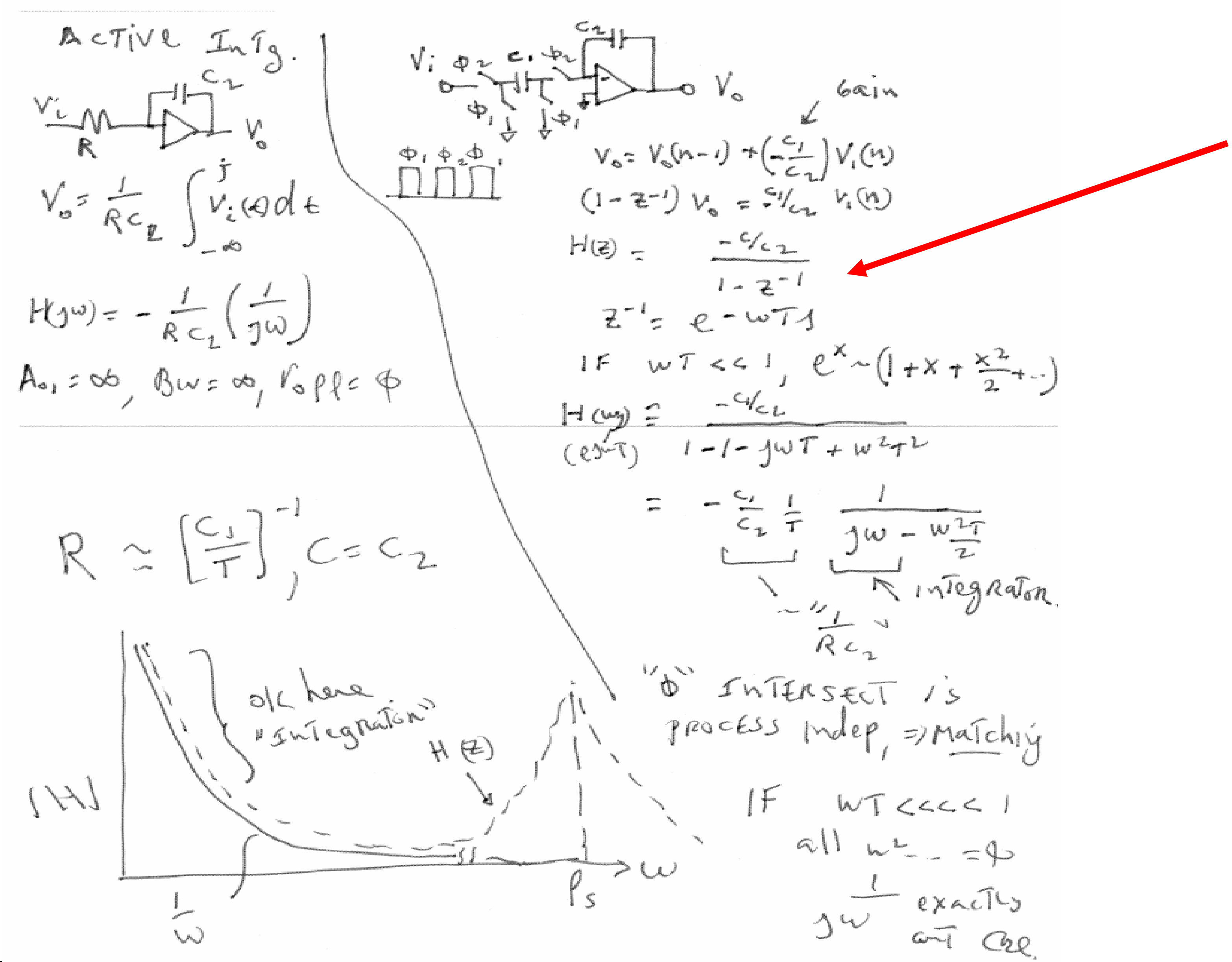


Discrete time integrator

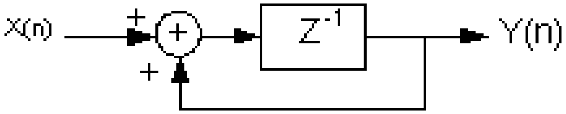
$$H = Z^{-1} / \quad 1 - Z^{-1}$$

Differences eq:
Y(n) = X(n-1) + Y(n-1)

Example: Z domain Vs. Time domain integrator ?

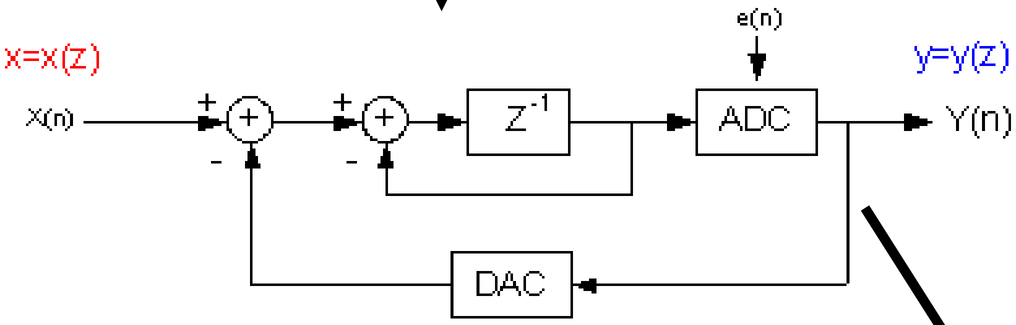


build the SD: lets put the integrator in the loop/s

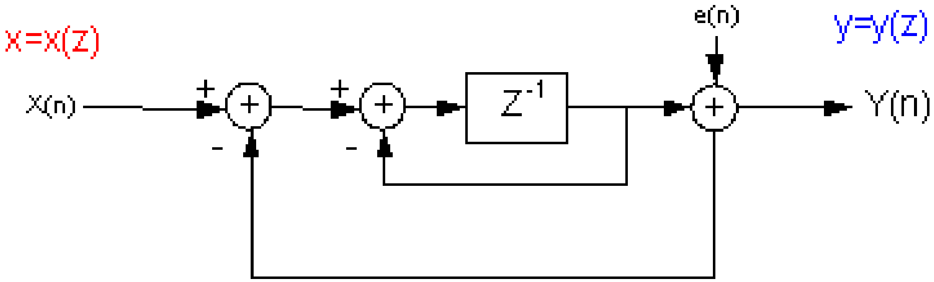


$H = Z^{-1} / \quad 1- Z^{-}$

Discrete time integrator

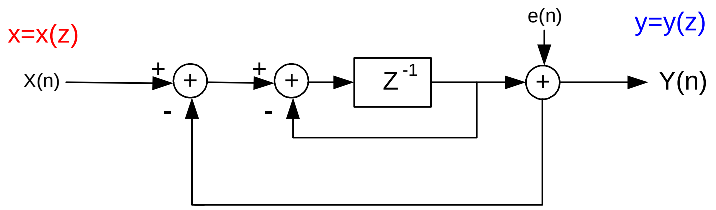


1st order SD



1st order SD
model

build the SD: TF calculations 1 Loop



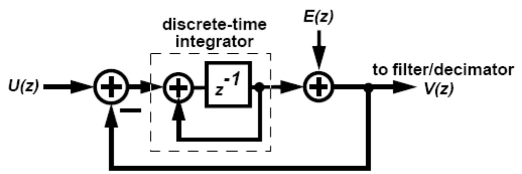
1st order SD model

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z)$$

$$Y(z) = H_x(z)X(z) + H_e(z)E(z)$$

with $H_x(z) = z^{-1}$ and $H_e(z) = (1 - z^{-1})$

First-Order Modulator



- Noise Transfer Function (NTF):

$$\rightarrow H(z) = \frac{V(z)}{E(z)} = \frac{1}{1 - L(z)} = \frac{1}{1 + \left(\frac{z^{-1}}{1 - z^{-1}}\right)} = 1 - z^{-1}$$

- Signal Transfer Function (STF):

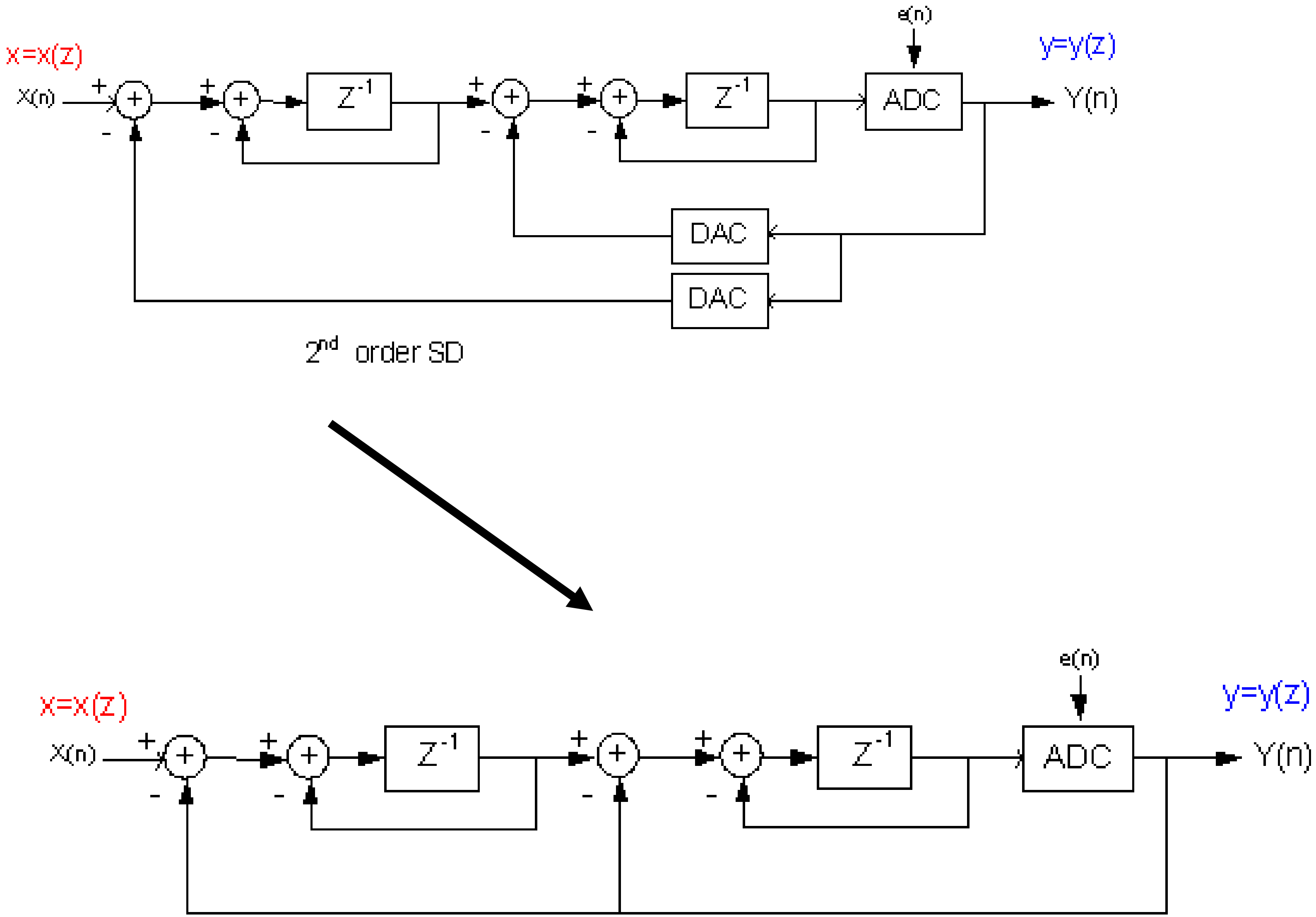
$$\rightarrow (z) = \frac{V(z)}{U(z)} = \frac{\left(\frac{z^{-1}}{1 - z^{-1}}\right)}{1 + \left(\frac{z^{-1}}{1 - z^{-1}}\right)} = z^{-1}$$

Same way

in time domain (n)

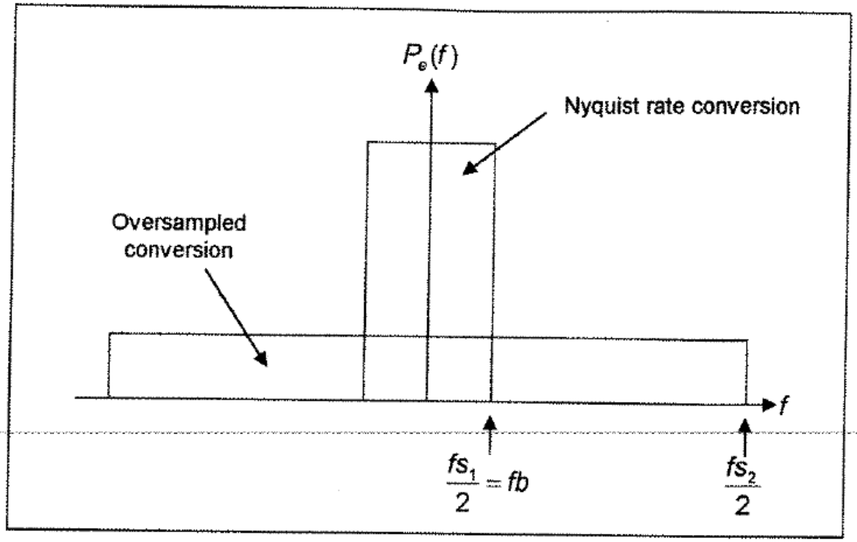
$$y[n] = x[n-1] + e[n] - e[n-1]$$

output is delayed input and High passed the error e.


e(n)
y=y(z)
x=x(z)
X(n)
Z -1
ADC
Y(n)
DAC
DAC
2nd order SD
e(n)
y=y(z)
x=x(z)
X(n)
Z -1
Z -1
ADC
Y(n)

HOW TO CALCULATE LOOP SNR

Uniform distribution of noise



$$\sigma_e^2 = \frac{\Delta^2}{12} = \frac{1}{12}\left(\frac{2V}{2^N - 1}\right)^2 \cong \frac{1}{12}\left(\frac{2V}{2^N}\right)^2$$

$$SNR = 10\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right)$$

The noise density power spectra density is

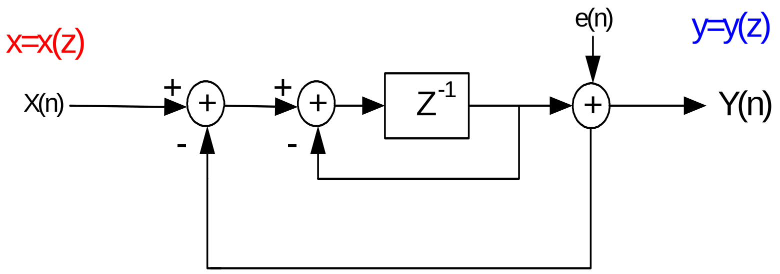
$$N(f) = \frac{\Delta^2}{12} * \frac{1}{fs}$$

$$\sigma_{ey}^2 = \int_{-fb}^{fb} P_{ey}(f)df = 2.\int_0^{fb} P_{ey}(f)df = \int_0^{fb} \frac{2\sigma_e^2}{fs}df = \sigma_e^2\left(\frac{2fb}{fs}\right)$$

$M = \frac{fs}{2fb}$ is called the OverSampling Ratio (OSR)

noise improvements: 3 dB/ octave

SNR Calculations for 1st order SD with integrator in the loop



1st order SD model

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z)$$

$$Y(z) = H_x(z)X(z) + H_e(z)E(z)$$

with $H_x(z) = z^{-1}$ and $H_e(z) = (1 - z^{-1})$

SNR calculations Z= exp (ST)
Look only at the magnitude

$$\sigma_{ey}^2 = \int_{-fb}^{fb} P_{ey}(f)df = 2.\int_{0}^{fb} P_{ey}(f)df = \int_{0}^{fb} P_e(f).\left|H_e(f)\right|^2 df = \int_{0}^{fb} \frac{\sigma_e^2}{fs}\left|1 - e^{-j\omega\tau}\right|^2 df$$

$$\sigma_{ey}^2 = \sigma_e^2 \frac{\pi^2}{3}\left(\frac{2fb}{fs}\right)^3$$

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^2}{3}\right) + 9.03r$$

~9db/ octave : doubling the sampling frequency reference to twice the maximum signal BW.

Remember DAC and ADC in the loop makes the delta LSB noise 6.02 x number of bits

$$NTF(z) = 1 - z^{-1} \tag{5.17}$$

For DC values, the noise transfer function is zero, thereby exactly producing $X(z)$. The shaping function, $1 - z^{-1}$, is analyzed using the transformation from the z domain to the s domain given by: $Z = e^{sT_s} = e^{jwT_s}$, where T_s is the sampling rate. The magnitude of the shaping function on $e(z)$ is written as $\left|1 - z^{-1}\right|$, and is calculated as

$$: \left|1 - e^{-jwT_S}\right| = \sqrt{[1 - \cos(wT_S) + j\sin(wT_S)][1 - \cos(wT_S) - j\sin wT_S]} \tag{5.18}$$

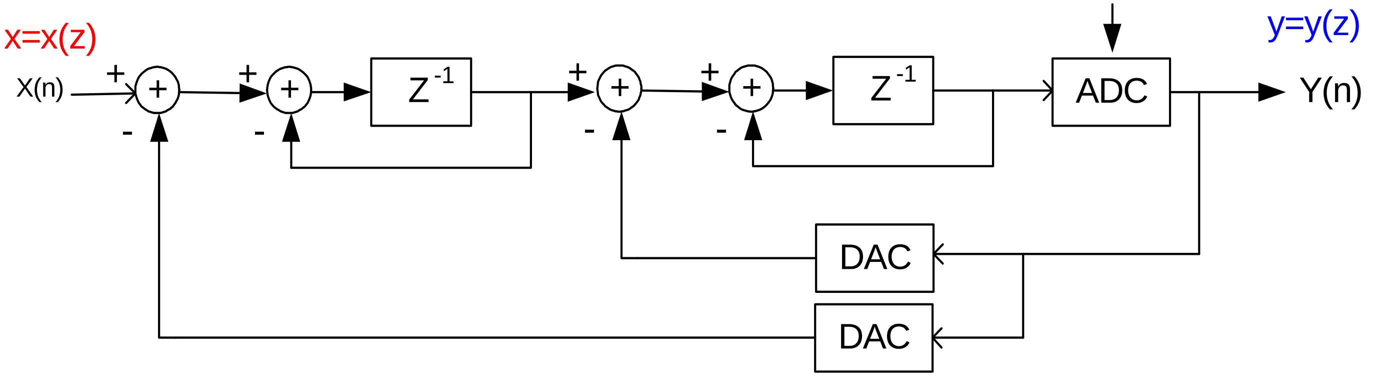
Combining the geometric terms of Eq. (5.18) yields,

$$|NTF(f)| = \sqrt{2 - 2\cos(2\pi f T_S)} \tag{5.19}$$

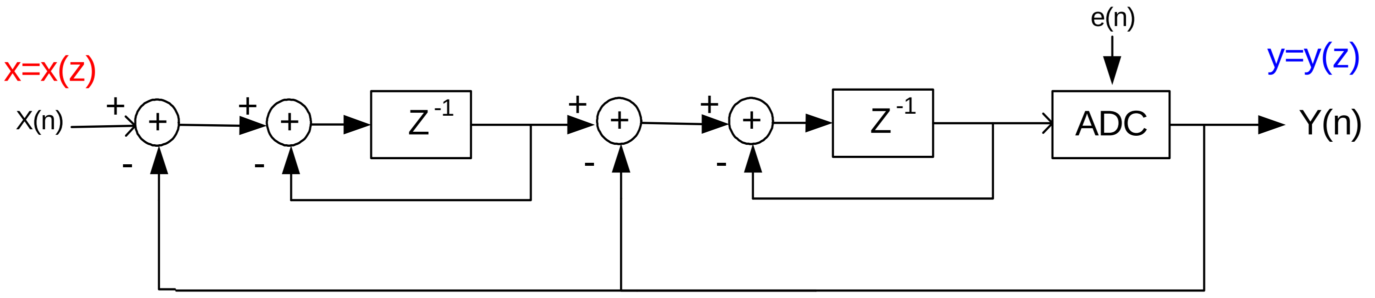
For a first order noise shaper, the noise power level improvement between any two frequencies, f and $2f$ is given by squaring and integrating Eq. (5.19) from f to $2f$

$$\int_f^{2f} NTF(f)^2 \, df = 2 - \frac{2\sin(2\pi T_S)}{2\pi T_s} = \quad 8.8 \text{ dB/octave} \tag{5.20}$$

SNR for 2nd order SD with integrator in the loop



2^{nd} order SD



2^{nd} order SD
model

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z)$$

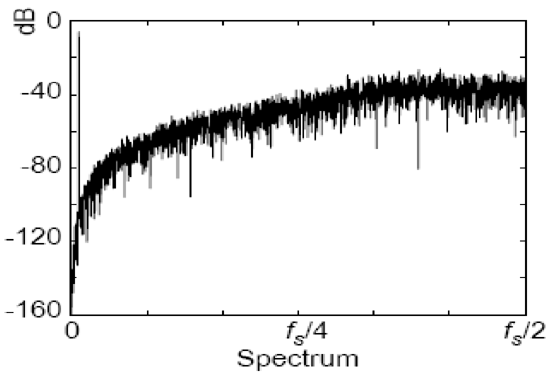
$$Y(z) = H_x(z)X(z) + H_e(z)E(z)$$

with $H_x(z) = z^{-1}$ and $H_e(z) = (1 - z^{-1})^2$

$$y[n] = x[n-1] + e[n] - 2e[n-1] + e[n-2]$$

$$\sigma_{ey}^2 = \int_{-fb}^{fb} P_{ey}(f)df = 2\int_{0}^{fb} P_{ey}(f)df = \int_{0}^{fb} P_e(f).\left|H_e(f)\right|^2 df = \int_{0}^{fb} \frac{\sigma_e^2}{fs}\left|1-2e^{-j\varpi\tau}+e^{-j2\varpi\tau}\right|^2 df$$

$$\sigma_{ey}^2 = \sigma_e^2 \frac{\pi^4}{5}\left(\frac{2fb}{fs}\right)^5$$



if r is the number of octaves

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^4}{5}\right) + 15.05r$$

For every doubling of the OSR, SNR improves by 15dB

Source : miki thesis

The advantage of the NS is that the noise is spread out to the higher frequencies to a location where the signal band is not used. The general form of the $NTF(z)$ is given by

$$NTF(z) = (1 - z^{-1})^{p} \qquad (5.24)$$

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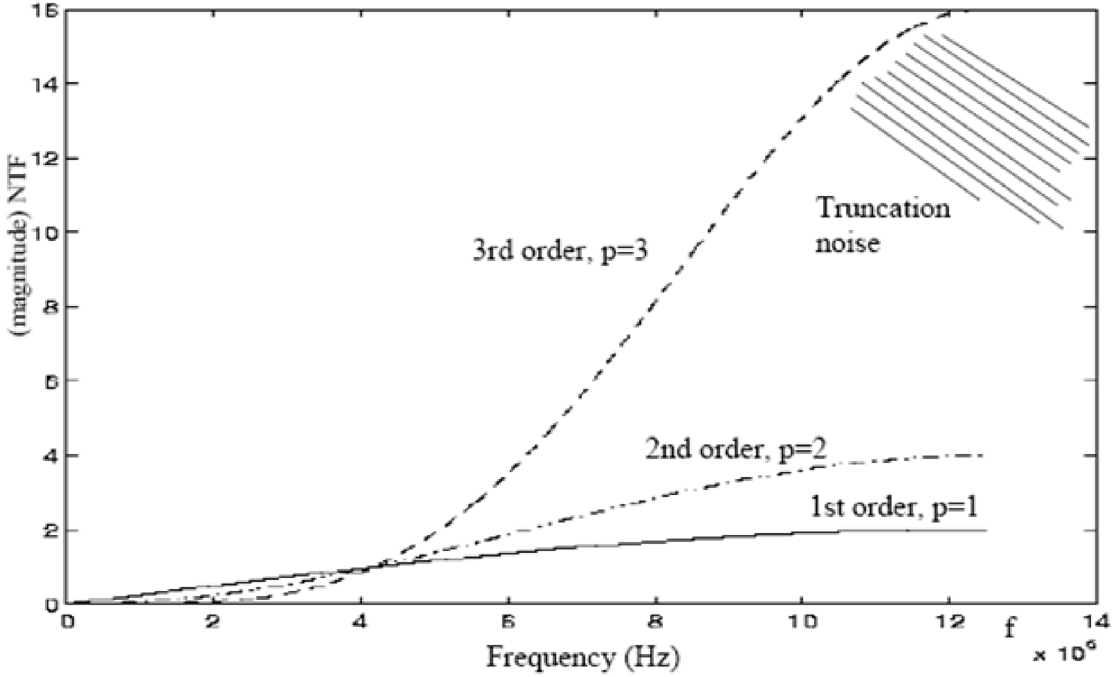


Figure 27: Simulation plot of NS truncated error coefficient

Modulator Performance

- 1st-order modulator:
  - 1st-order highpass NTF
  - 9-dB SNR increase per octave OSR
  - i.e. 1.5 bits/octave!
    (compared with 0.5-bit/octave for white noise)
- 2nd-order modulator:
  - 2nd-order highpass NTF
  - 15-dB SNR increase per octave OSR
  - i.e. 2.5 bits/octave!
- *N*th-order modulator:
  - *N*th-order highpass NTF
  - $6N+3$ dB SNR increase per octave OSR
  - i.e. $N+0.5$ bits/octave!

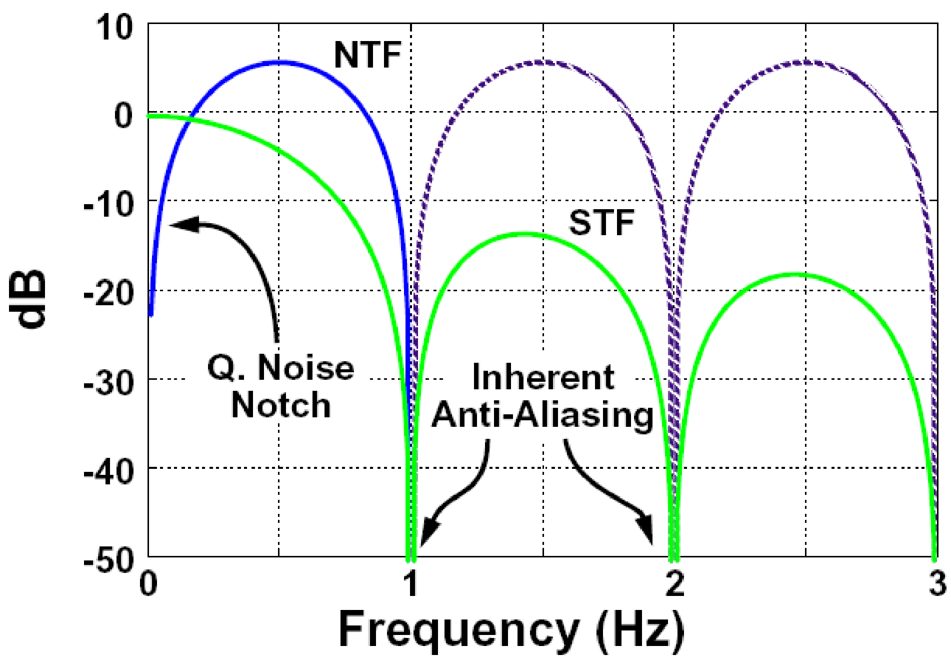
$$SNR_{max} = 10\log\left[\frac{3}{2}(2^{B}-1)^{2}\frac{(2L+1)M^{2L+1}}{\pi^{2L}}\right]$$

$M = \frac{f_s}{2f_B}$ = Oversampling Ratio

L = Modulator Order

B = Internal Quantizer Resolution

Frequency Responses



What is really going on:

For 1st order the integrator become LPF and the 1-z-1 is 2-coswt to the N

DESIGN EXAMPLE: (assume a's all 1)

Spec: VFs=1v,
Design an ADC for : SNR>86dB, (>14b), fin=0-8KHz,
Extra constrain: Power <2ma, Vdd=3.3v.

Objective:
We need to determin: Loop Order , DAC number of bits, smf Fclock

Option I SigmaD ADC SNR(quantization) CALCULATION

miki

DACS Number of Bits: $B := 5.0$

Oversampling Ratio: $R := 128$

ADC Order: $n := 1$

Overload Voltage: $V := 0.75$

Integrator loop coefficients: $a0 := 1.0$ $a1 := 1.0$ $a2 := 1.0$ $a3 := 1$

Fin maximum: $Fin := 8 \times 10^{3}$

Boltzman condt and Temp: $Kb := 1.38 \times 10^{-23}$ $Temp := 293$

1. 1st-order SDM, 5-bit -Quantizer, fs=2.048 MHz, Fin=8 KHz

SNR- Equation

Maximum SNR

$$SNRpk := \left[(2)^{B} - 1\right]^{2} \cdot (2n+1) \cdot \left(\frac{R}{\pi}\right)^{(2n+1)} \cdot a0 \cdot a1 \cdot a2 \cdot a3 \cdot \left(\frac{3 \cdot \pi}{2}\right) \cdot V$$

$SNRpk = 6.892 \times 10^{8}$

In dB

$$SNRdBpk := 10 \cdot \log(SNRpk)$$

$SNRdBpk = 88.383$

Thermal Noise Requirements

If we make the converter with switch cap then the noise…

$$Cin := 1 \times 10^{-12}$$

$$Vnqcap := \left(\frac{Kb}{Cin}\right)^{0.5}\left[\left(\frac{Temp}{Fin}\right)^{0.5}\right]\cdot\frac{1}{1} \qquad Vnqcap = 7.109 \times 10^{-7}$$

$$Vnqcap := \left(\frac{Kb}{Cin}\right)^{0.5}\left[\left(\frac{Temp}{1}\right)^{0.5}\right]\cdot\frac{1}{1} \qquad Vnqcap = 6.359 \times 10^{-5}$$

$$SNRdBcap := 20\cdot\log\left(\frac{V}{Vnqcap}\right) \qquad SNRdBcap = 81.434 \text{ dB}$$

$$Fck := 2\cdot R\cdot Fin \qquad Fck = 2.048 \times 10^{6}$$

$$SNRdBcap := 20\cdot\log\left[\left(\frac{V}{Vnqcap}\right)\left[\left(\frac{Fck}{2.Fin}\right)^{0.5}\right]\cdot\frac{1}{1}\right] \qquad SNRdBcap = 102.506 \text{ dB}$$

The capacitance noise concern to 8 KHz so we get 102dB

Option II SigmaD ADC SNR(quantization) CALCULATION

miki

DACS Number of Bits
$B := 1.0$

Oversampling Ratio
$R := 1024$

ADC Order
$n := 1$

Overload Voltage
$V := 0.75$

Integrator loop coefficients

$a0 := 1.0 \quad a1 := 1.0 \quad a2 := 1.0 \quad a3 := 1$

Fin maximum

$Fin := 8 \times 10^{3}$

Boltzman condt and Temp

$Kb := 1.38 \times 10^{-23} \quad Temp := 293$

1st-order SDM, 1-bit -Quantizer, fs=16.138 MHz, Fin=8 KHz

SNR- Equation

Maximum SNR

$$SNRpk := \left[(2)^{B} - 1\right]^{2} \cdot (2n+1) \cdot \left(\frac{R}{\pi}\right)^{(2n+1)} \cdot a0 \cdot a1 \cdot a2 \cdot a3 \cdot \left(\frac{3 \cdot \pi}{2}\right) \cdot V$$

$SNRpk = 3.672 \times 10^{8}$

In dB

$$SNRdBpk := 10 \cdot \log(SNRpk)$$

$SNRdBpk = 85.649$

Option III SigmaD ADC SNR(quantization) CALCULATION

miki

DACS Number of Bits
$\mathbf{B} := 1.0$

Oversampling Ratio
$\mathbf{R} := 128$

ADC Order
$\mathbf{n} := 2$

Overload Voltage
$\mathbf{V} := 0.75$

Integrator loop coefficients

$\mathbf{a0} := 1.0$ $\mathbf{a1} := 1.0$ $\mathbf{a2} := 1.0$ $\mathbf{a3} := 1$

Fin maximum
$\mathbf{Fin} := 8 \times 10^{3}$

Boltzman condt and Temp
$\mathbf{Kb} := 1.38 \times 10^{-23}$ $\mathbf{Temp} := 293$

2nd order SDM, 1-bit -Quantizer, fs=2.048 MHz, Fin=8 KHz

SNR- Equation

Maximum SNR

$$\mathbf{SNRpk} := \left[(2)^{\mathbf{B}} - 1\right]^2 \cdot (2\mathbf{n}+1) \cdot \left(\frac{\mathbf{R}}{\pi}\right)^{(2\mathbf{n}+1)} \cdot \mathbf{a0} \cdot \mathbf{a1} \cdot \mathbf{a2} \cdot \mathbf{a3} \cdot \left(\frac{3 \cdot \pi}{2}\right) \cdot \mathbf{V}$$

$\mathbf{SNRpk} = 1.984 \times 10^{9}$

In dB

$$\mathbf{SNRdBpk} := 10 \cdot \log(\mathbf{SNRpk})$$

$\mathbf{SNRdBpk} = 92.976$

End Lecture 10

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