Welcome to
046188 Winter semester 2012
Mixed Signal Electronic Circuits
Instructor: Dr. M. Moyal

Lecture 9

SUCCSSESIVE APROXIMATION ADC: Operation

Design of Time Continuous SARs

Design of Switch C SAR

Error sources

EXAM DAY 23/6/09 14 pm ! Available question on project

www.gigalogchip.com

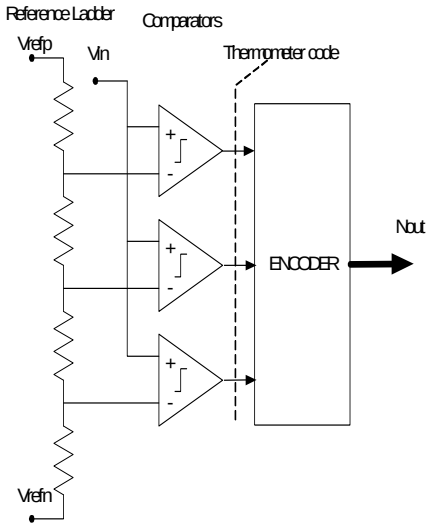
Agenda

ADC Architectures

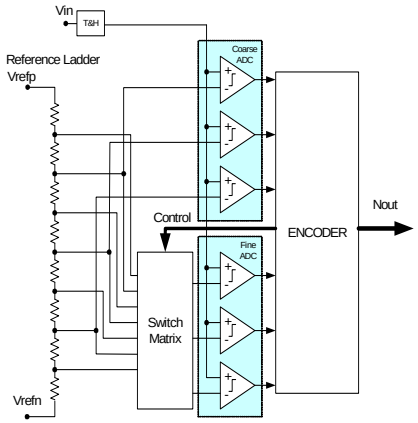
SAR ADCs

Error Sources

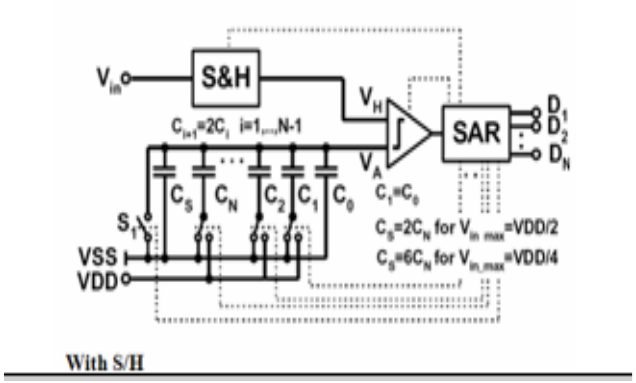
Common Data Acquisition Architectures



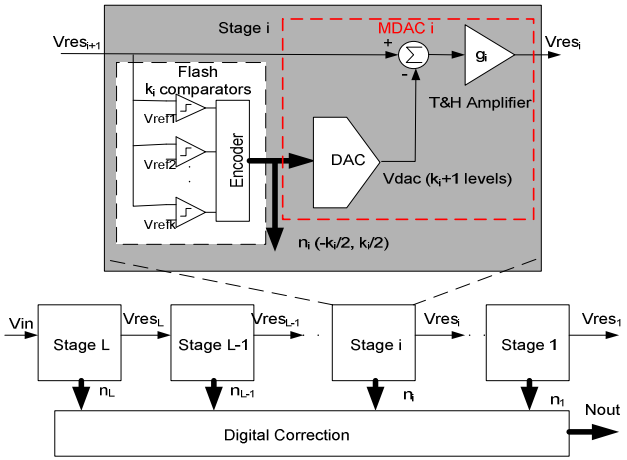
FLASH ADC



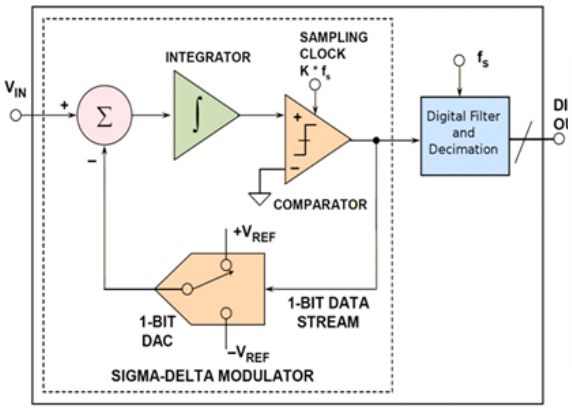
Sub ranging



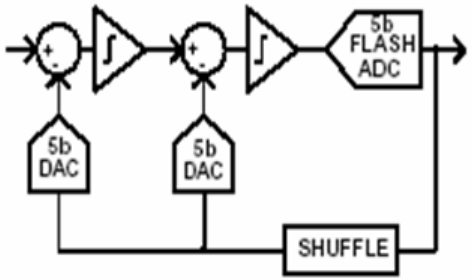
SAR



Pipe Line



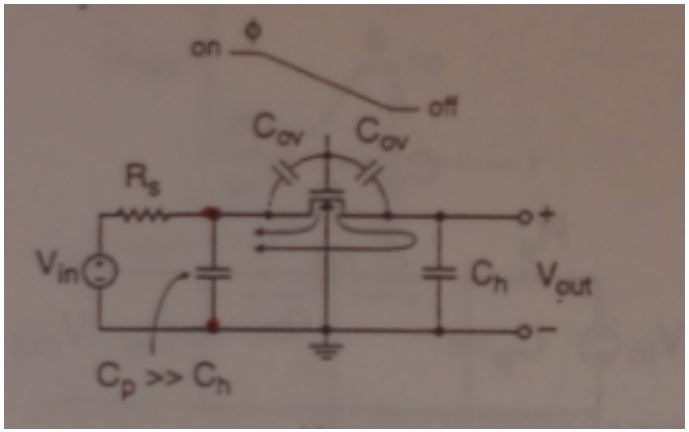
Sigma Delta



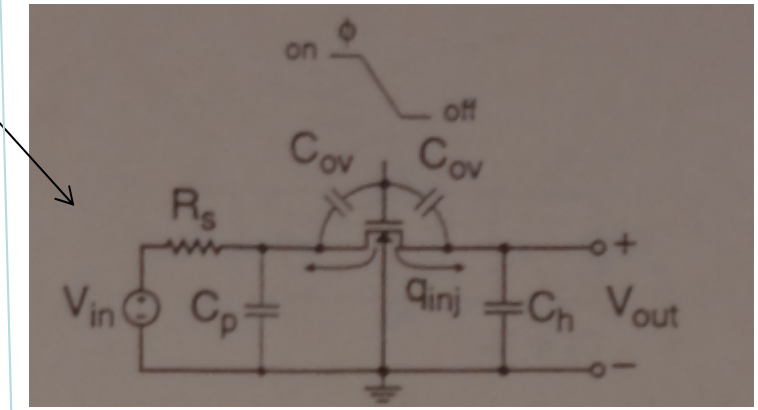
SD multi bits

Short summary/review of lect 8- s/h..

$$\Delta V = \alpha \frac{C_{ov}}{C_{ov} + C_h} V_{swing} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{leak} T_h}{C_h}$$



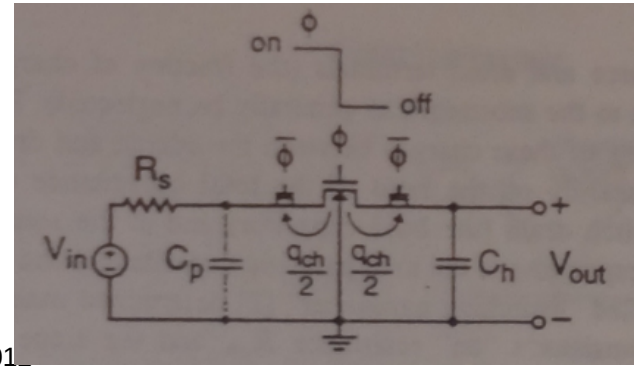
Slow clock Charge almost 0



Cp=Ch

Fast clock Charge split

$$q_{inj} = C_{ox} \times W \times L \times (V_H - V_{in} - V_T)$$



Cp=Ch reduced charge injection

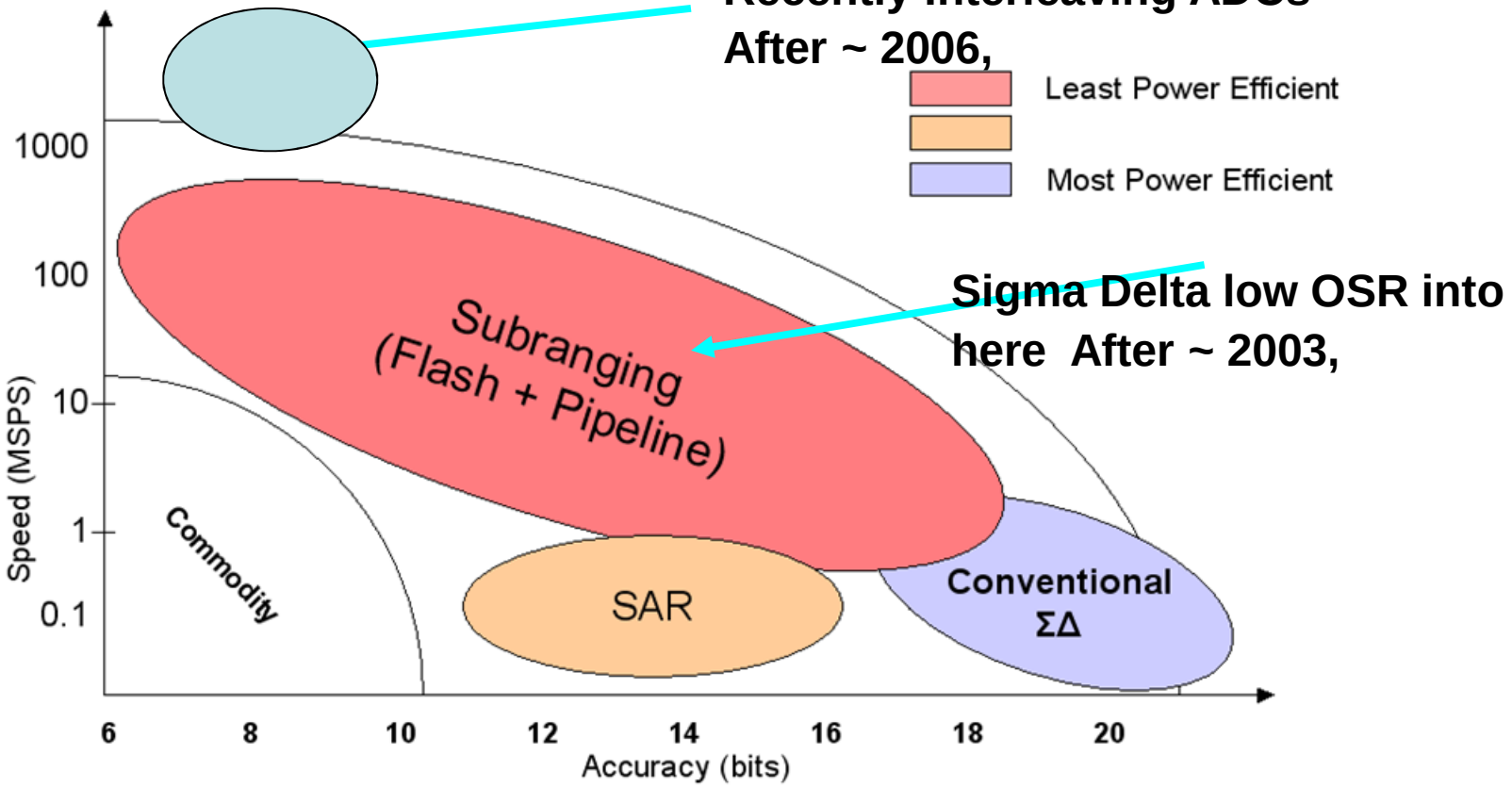
Fast clock add short w/2

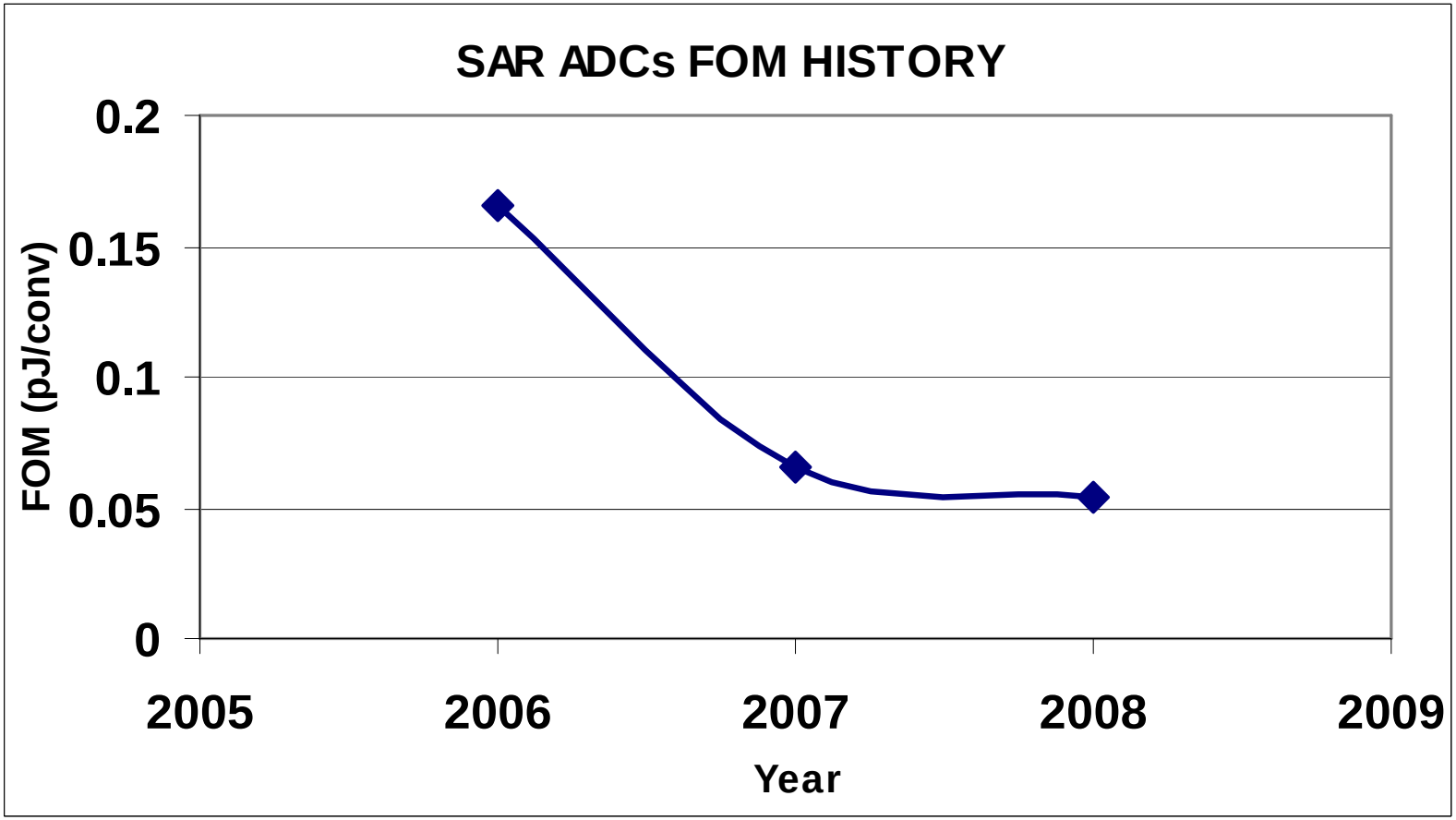
Source: C. Temes

Which ADC to use and why

miki Technion

ADC Architectures





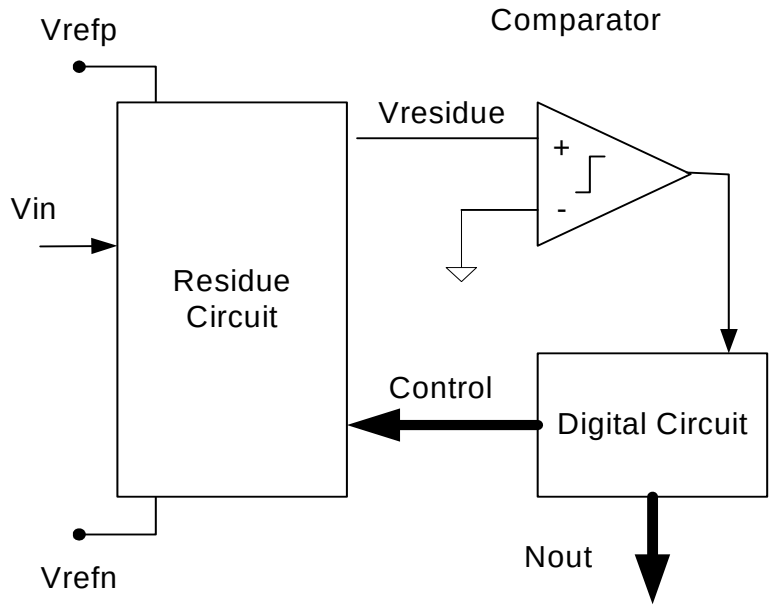
2006 ➔ 12b & 100Ks/s (180nm CMOS)

2007 ➔ 9b & 50Ms/s (90nm CMOS)

2008 ➔ 9b & 40Ms/s (90nm CMOS)

$$\text{Energy/Decision} = \frac{Power}{SamplingRate \cdot 2^{Nbit}}$$

Generic ADC:



V residue is a function of Vin – Vref .
THE RESIDUE SETS THE SOURCE OF LINEARITY ERRORS
THE COMPARATOR SET THE SOURCE OF SPEED (Offset may be a problem)

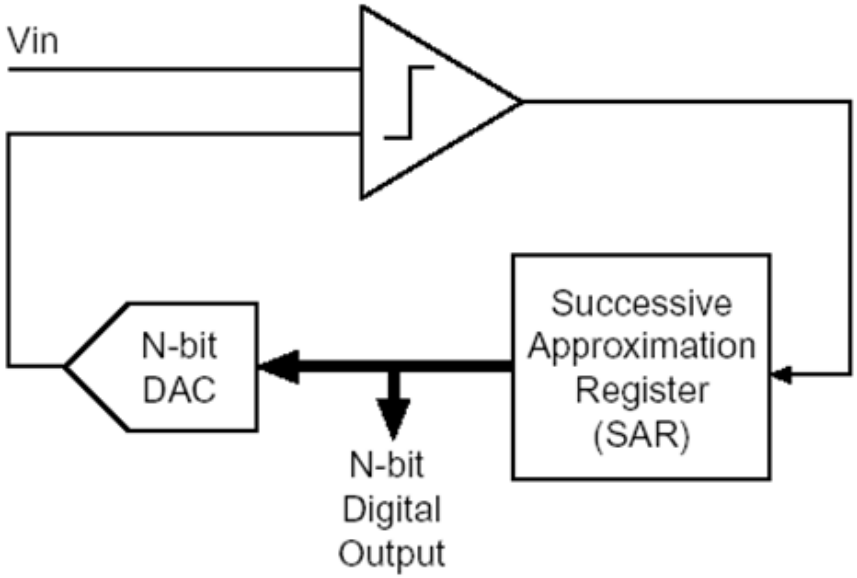
Must check always:
Distortion (non linearity's) and ckt noise.
Speed and Power

Successive approximation ADC

If Ts is twice maximum BW

And if N =desire bits

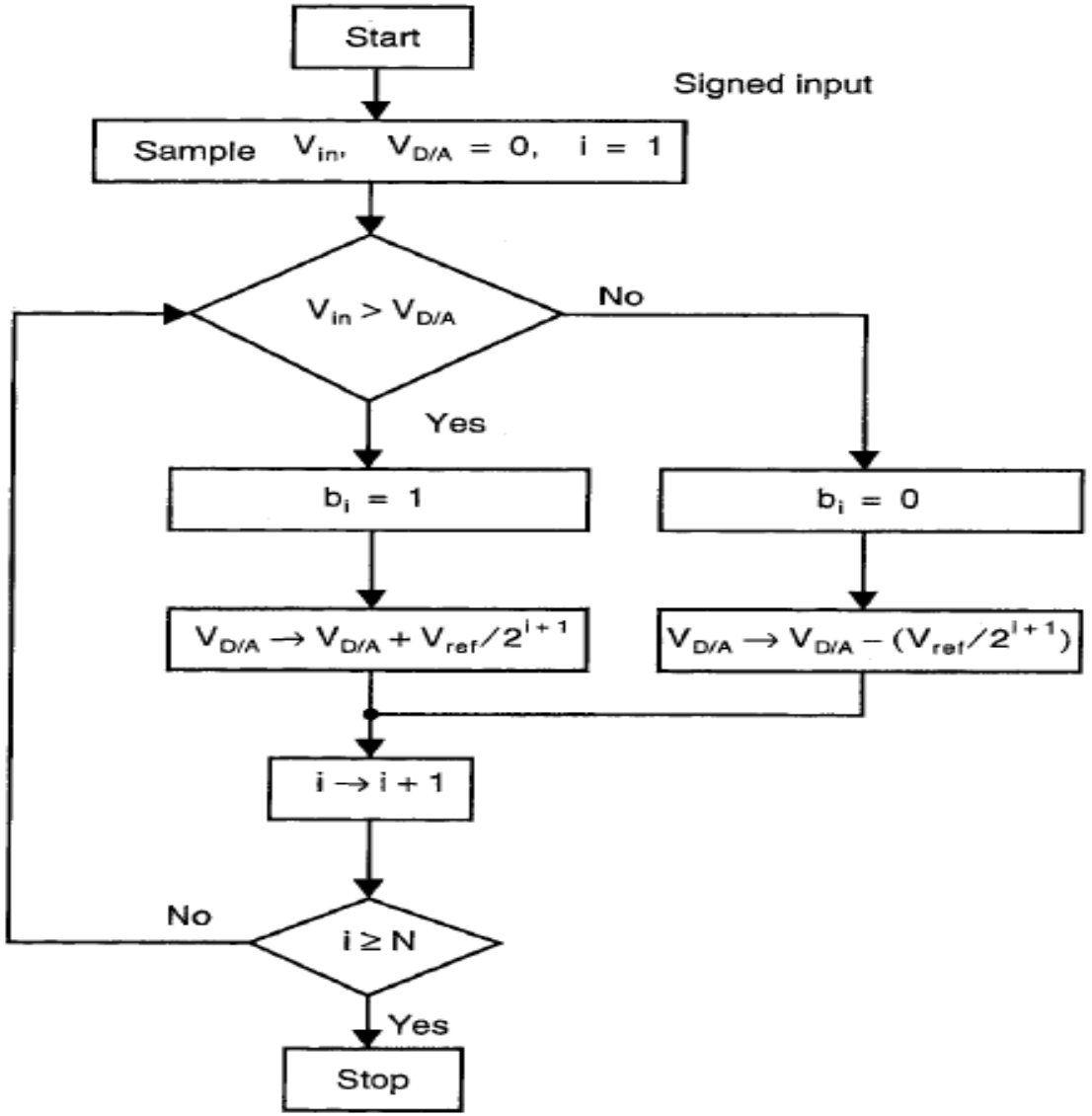
It requires minimum of p= N xTs passes to generate N bit
Output words limiting the through put
It requires N-bit accurate DAC
It requires faster settling elements



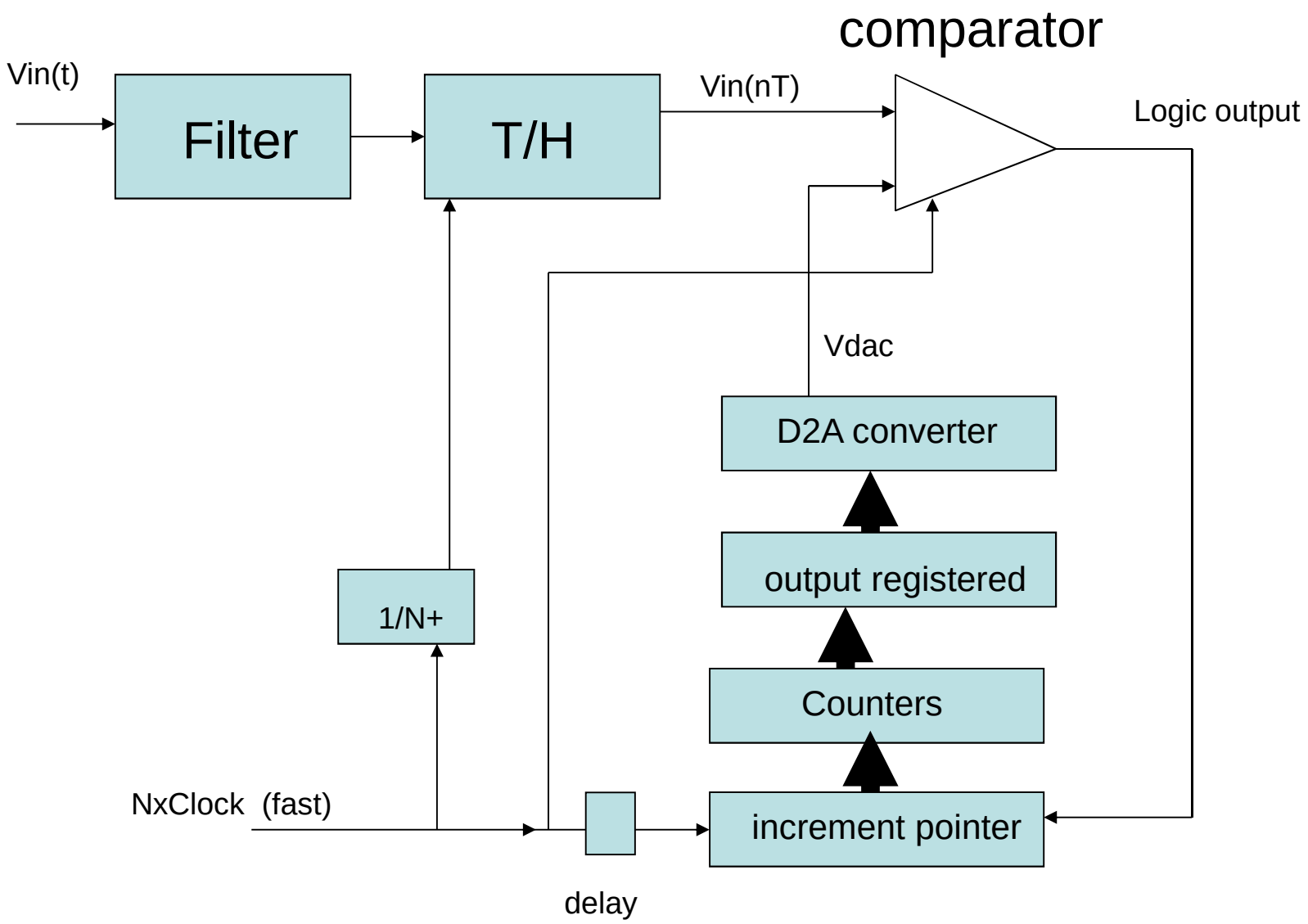
Strict timing is involved- transforming analog to digital each cycle

Comparator runs inside an open loop circuit
therefore stability and closed loop Band width is not an issue.

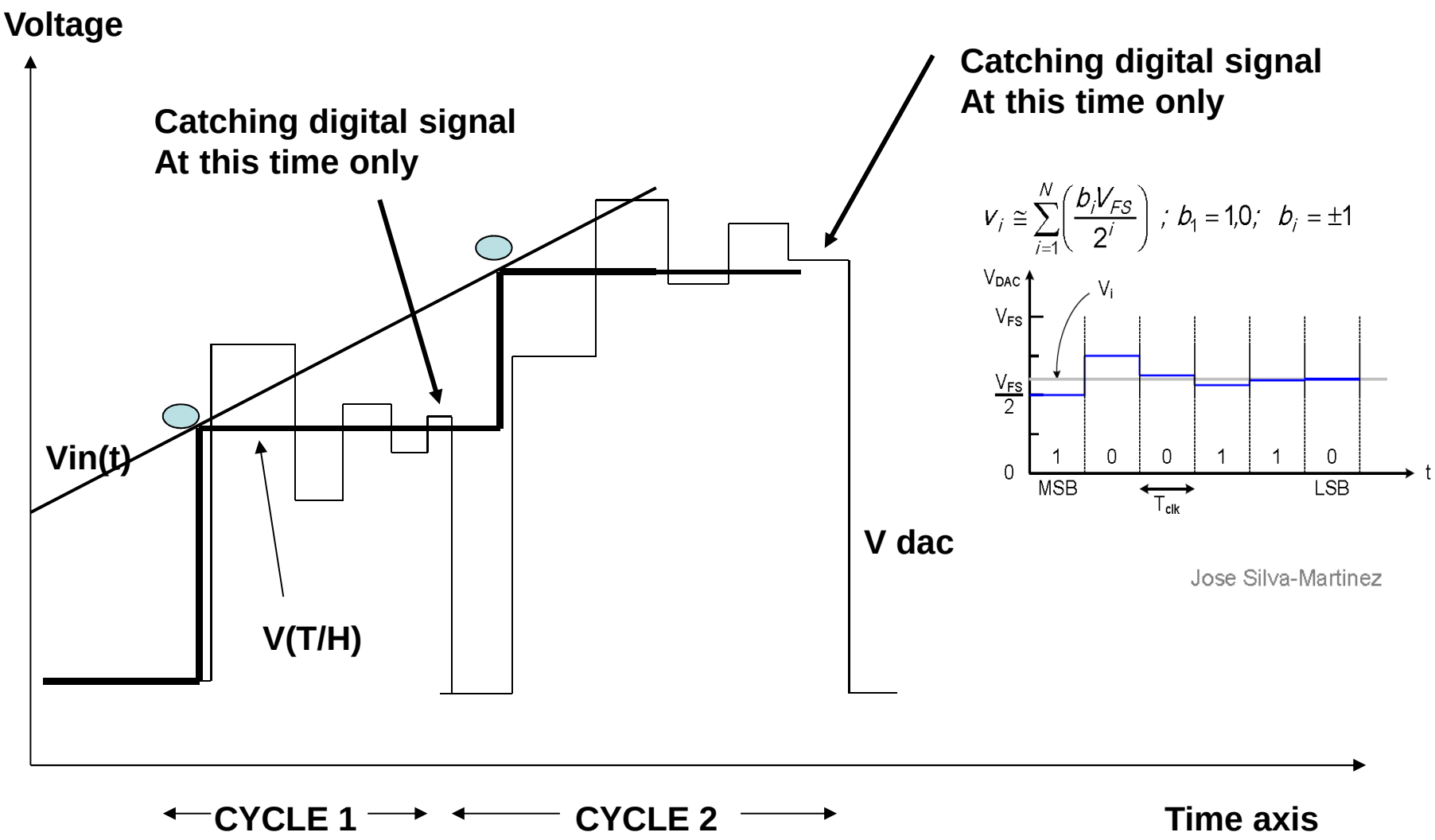
FLOW GRAPH OF SAR ADC



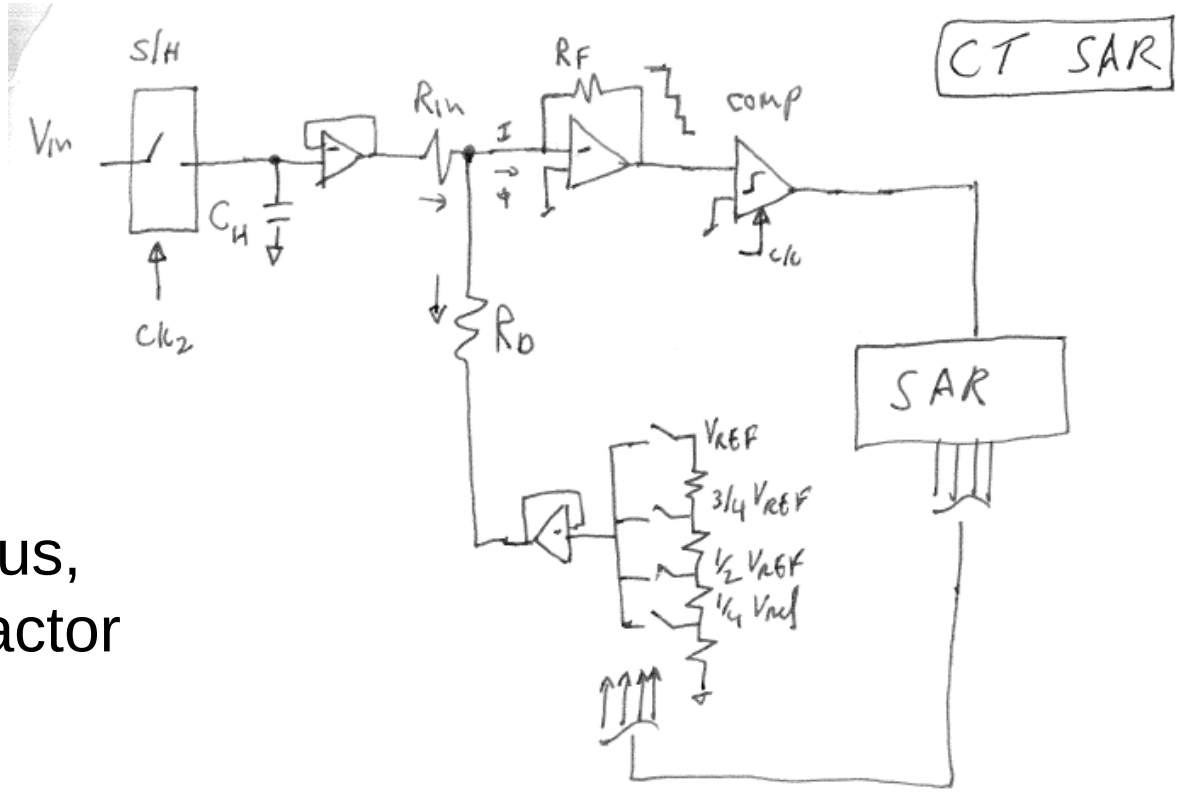
SAR ADC details



SAR ADC timing look



SAR Operation/Design



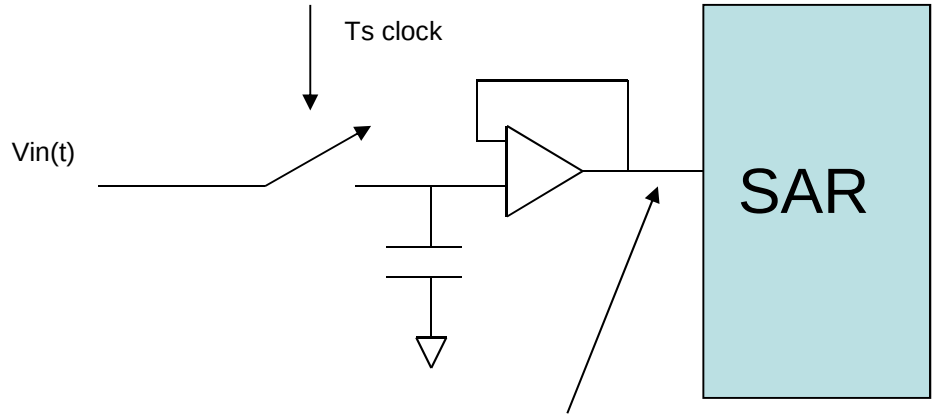
Continuous,
w. sub tractor

① AT Full Scale Figure out $R_D \Rightarrow \frac{V_{in_{max}}}{R_{in}} = \frac{V_{REF}}{R_D}$

$$R_D = \left[\frac{V_{in\,F.Scale}}{V_{REF}}\right]^{-1} \cdot R_{in}$$

Time continuous SAR block

1st step sample and hold

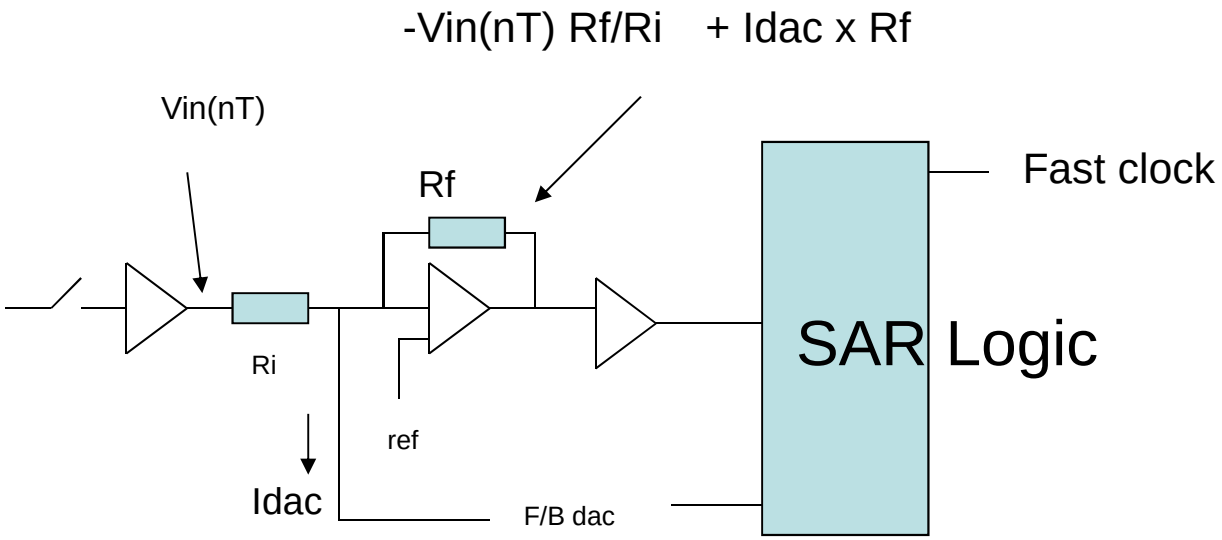


Covered in lecture 8

We know the errors,
We know the speed needed
We can proceed to build the block

Example, SAR Analog loop

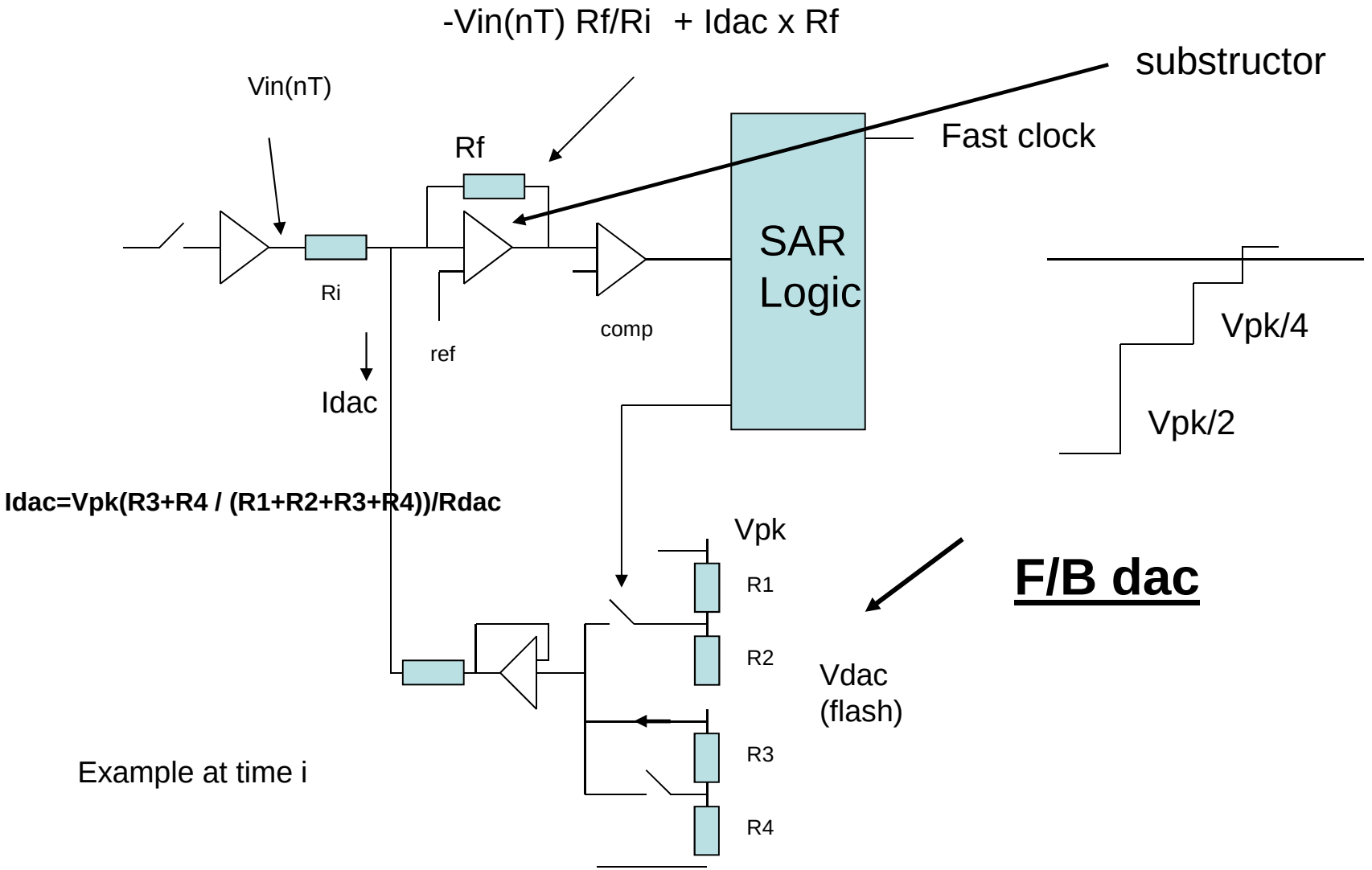
2nd step the sampled voltage part is being converted to I



Next how to build Idac

Example cont, SAR Idac feed back geneararition

3rd step the Iin and Idac is compared around the loop n times



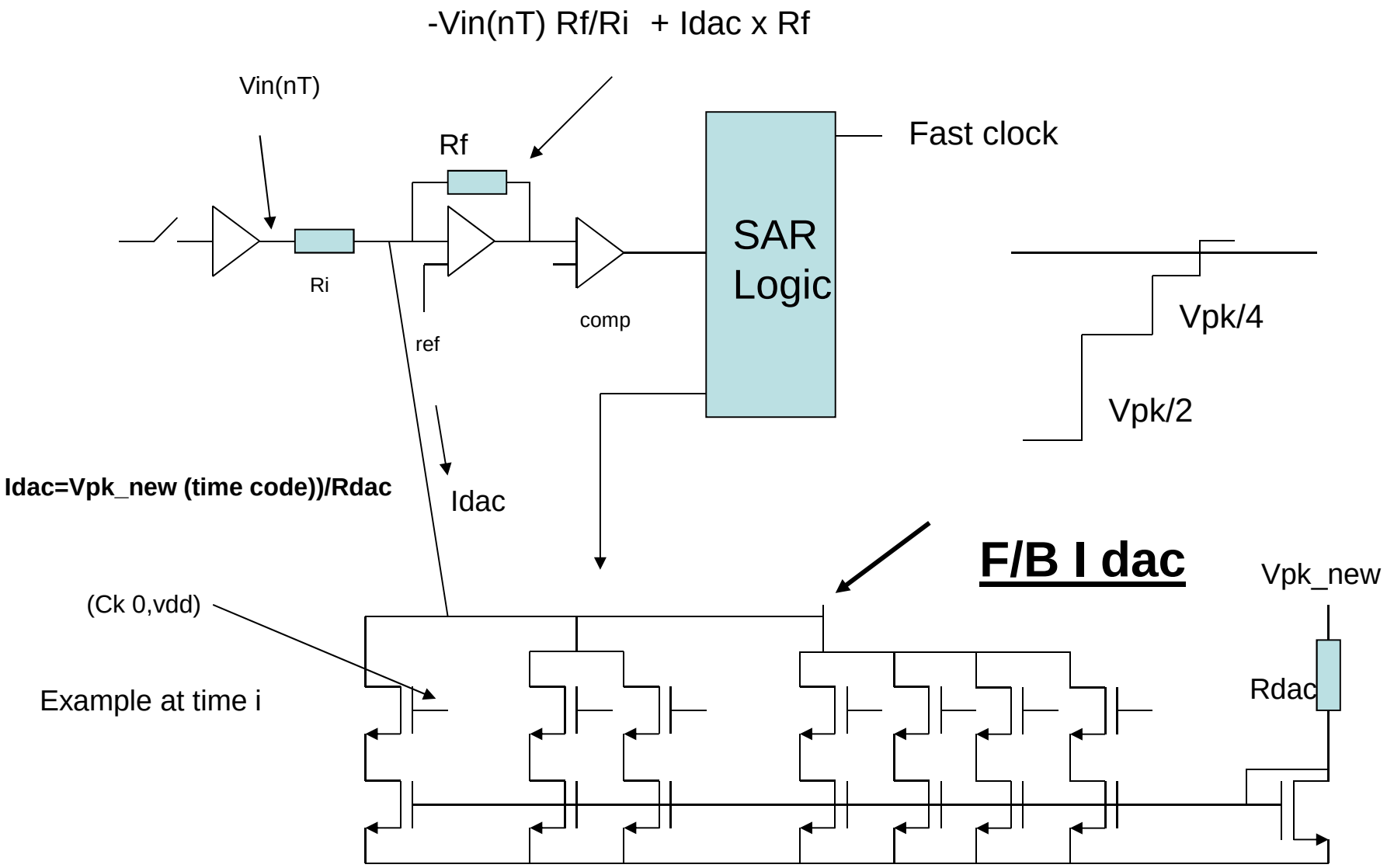
SAR DAC – use another alternative to R-Ladder

Go to DAC lecture pick another type ?

We got transistors they are small

Current is always easy to generate with transistors

SAR DAC – another dac – speed and area improvment



SAR DAC – another dac – speed and area improvment

Lets look at other DAC in SAR approach.

Speed issues: BW amplifier,
Subtraction with amplifier
s/h- or track and hold.
Area

Can we do it other way ?
Lead to a simpler architecture
No amplifiers ! !
With capacitors we can easily subtract
Speed per cycle may be faster

SAR – another dac – speed and area improvment

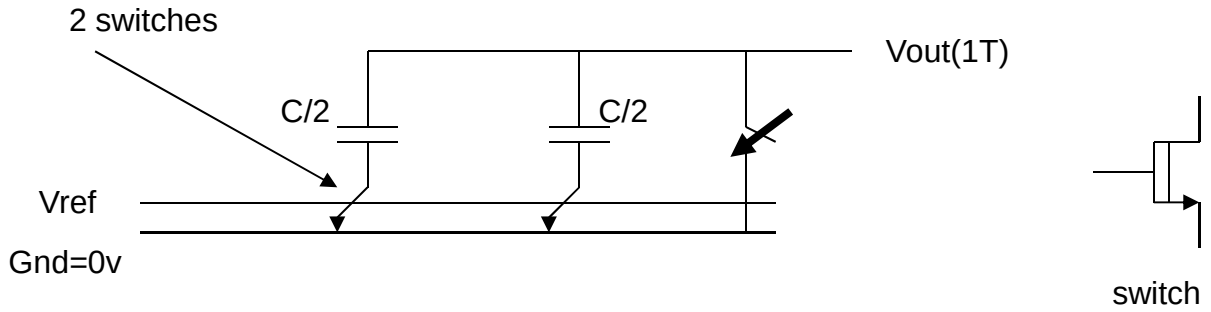
We want to generate

Vref/2….	1st clock cycle
Vref/2 +/- Vref/4..	2nd clock cycle
Vref/2 +/- Vref/4 +/-Vref/8	3rd clock cycle
.. Etc..., ,	

So lets use capacitor DAC to do this.

Charge distribution SAR DAC operation

Step 1.- clock n=1, reset everything to 0 point – “wasted state” but needed because capacitors plates are held at a “value” for DC

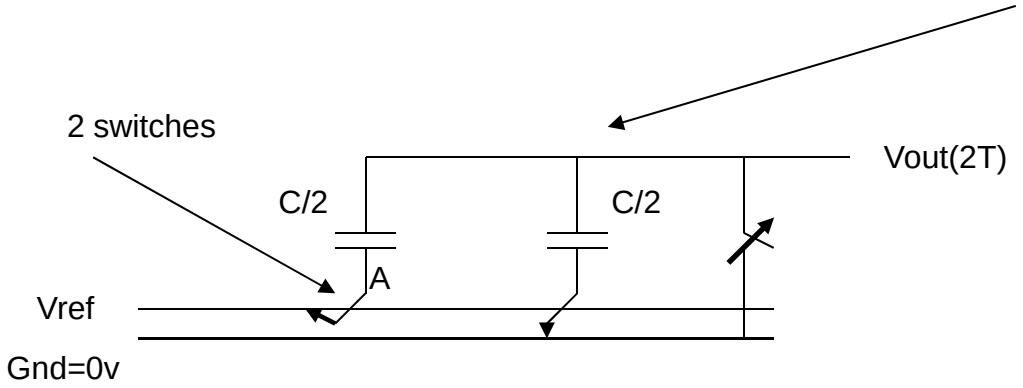


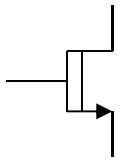
Vout = 0v all capcitors plates are shorted to 0
In reality after nRonC/2 time (Ron=1/ucox(vgs-vt)(w/l)

Generate Vref/2 to compare

Step 2.- clock n=2, generate vref/2 to compare with input

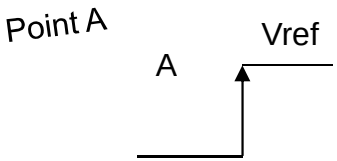
Voltage divider action





switch

Vout = 1/2vref at the end of the clock time



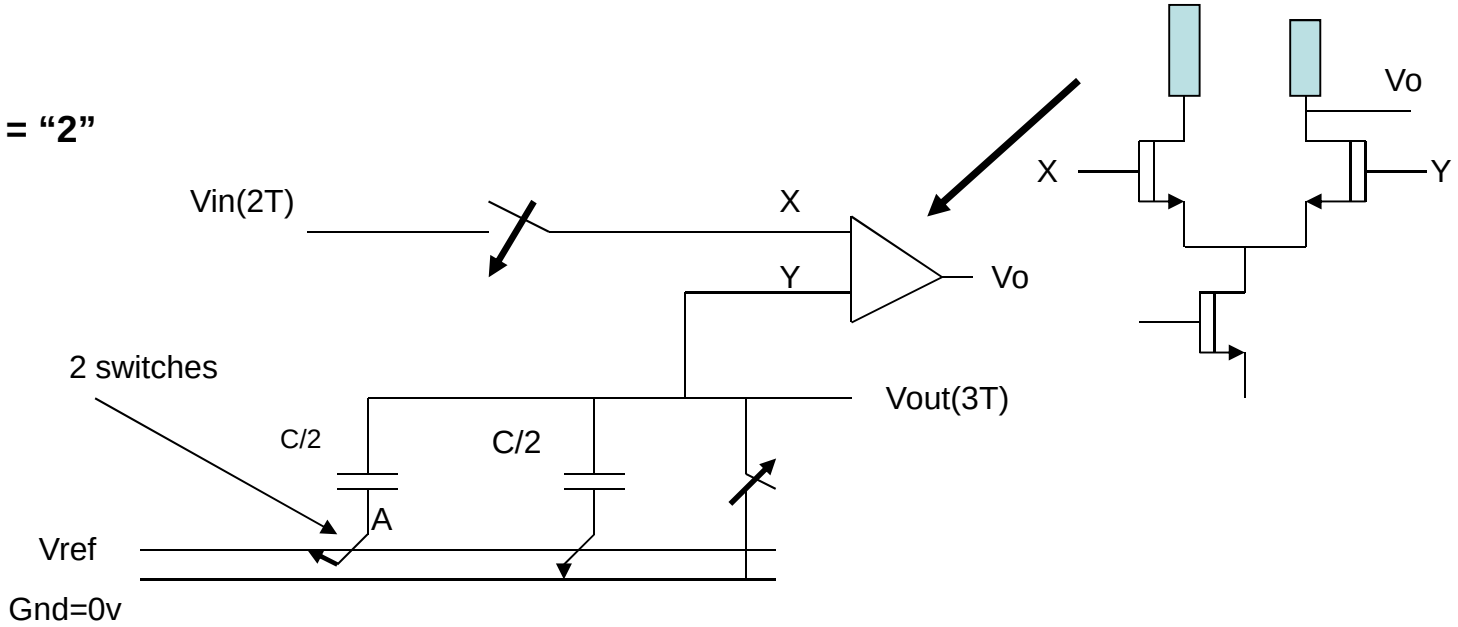
Vout(2T)= 0 + 1/S0.5C/(1/S0.5C+1/S0.5C) Vref

Vout(2T)= 1/0.5 / (1/0.5+1/0.5) Vref

Vout(2T)= Vref/2

Compare to Vref/2 and generate Vref/2 + Vref/4

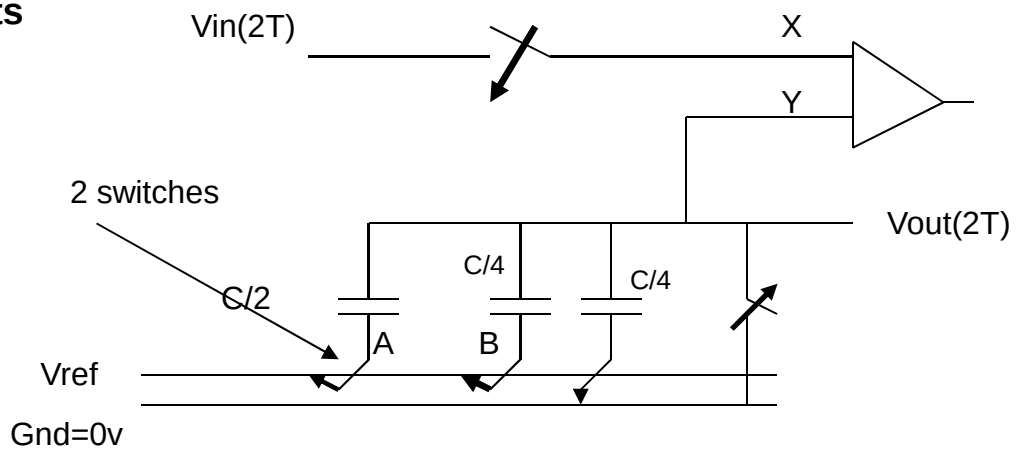
still **in time = “2”**



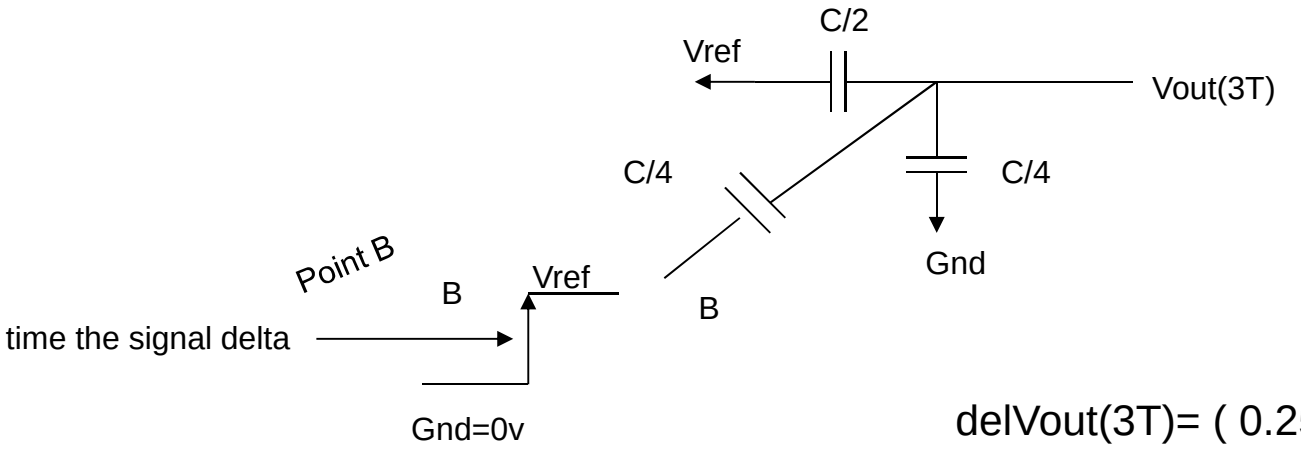
Vo =

in time = “3 ” add ¼ vref

Re arrange C to units



Time “3” Generate Vref/2 + Vref/4



delVout(3T)= (0.25C / C) Vref

Del Vout(3T)=1 /4 (time the signal delta)

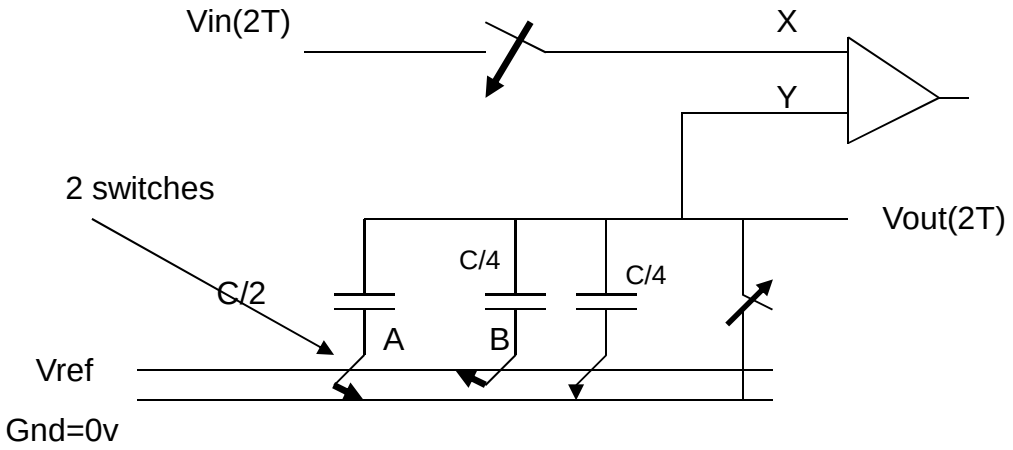
Vout(3T)= Vref(2T) + 1/4 Vref

Vout(3T)= Vref/2+Vref/4

Generate the minus ➔ Vref/2 - Vref/4

in time = “3 ” let say we want to add -¼ vref

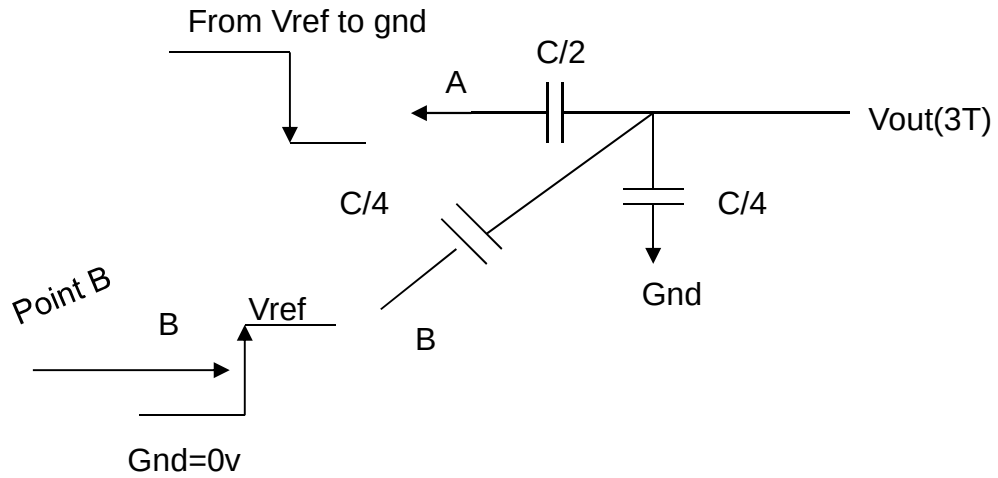
2 operations



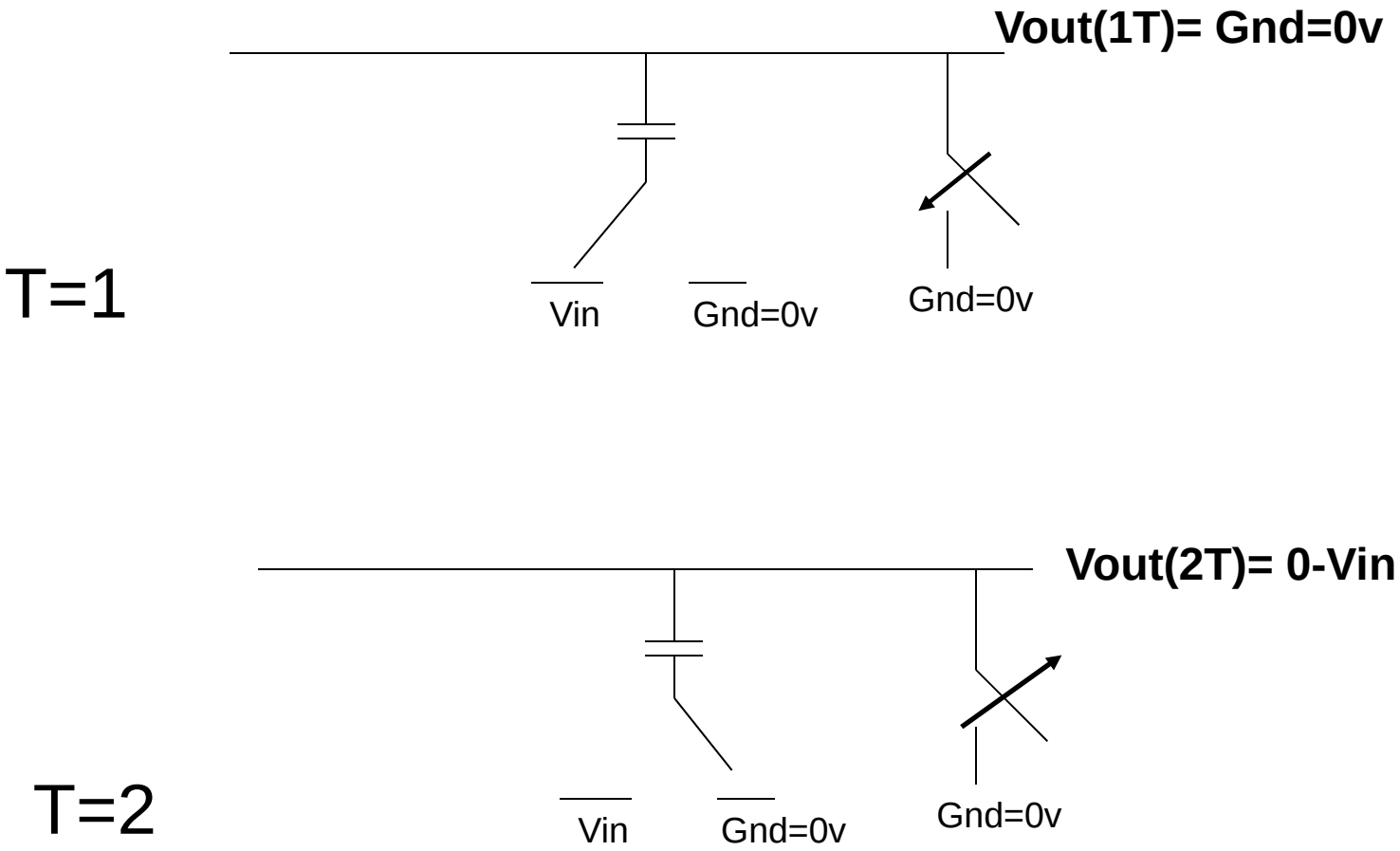
delVout(3T)= -0.5+0.25

Vout(3T)= V(2T) + -0.5+0.25

delVout(3T)= 1/4Vref

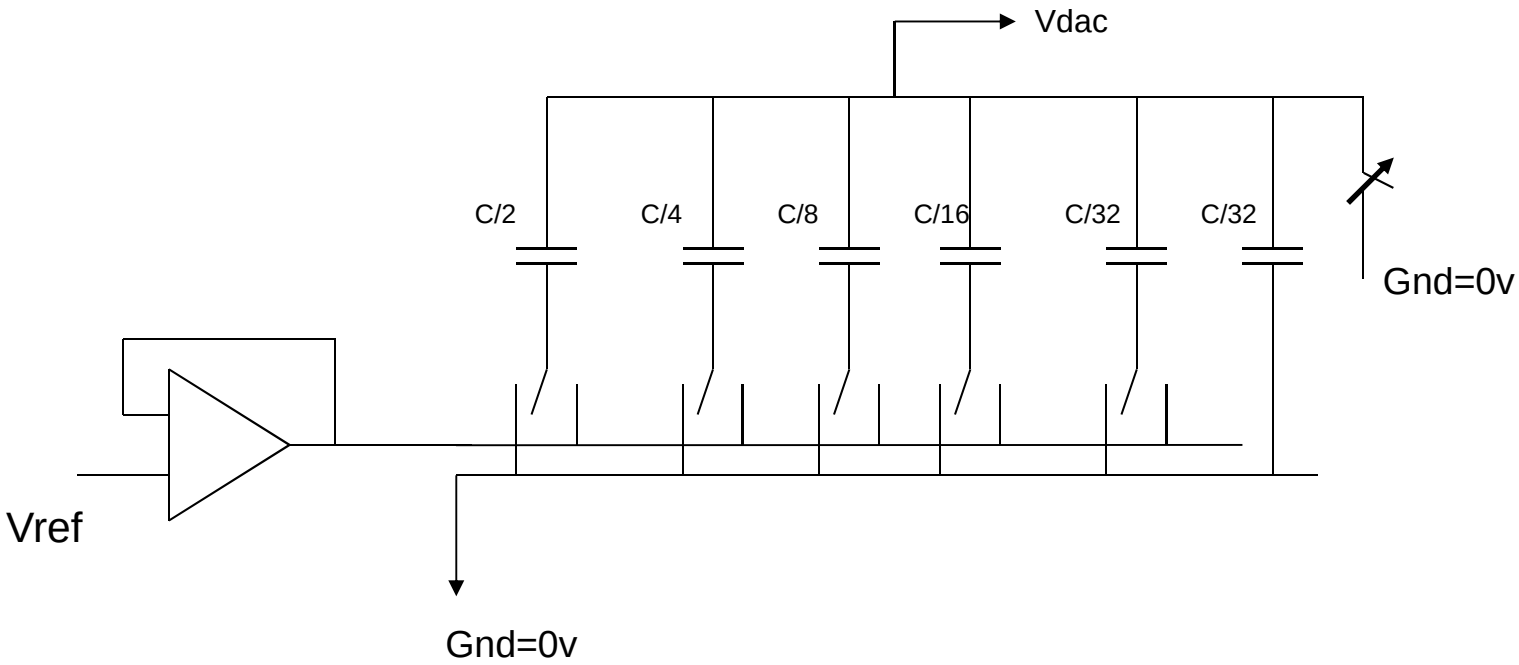


Generate the minus of the input as well easily



And on.. And on.. Until the number of bits M+1

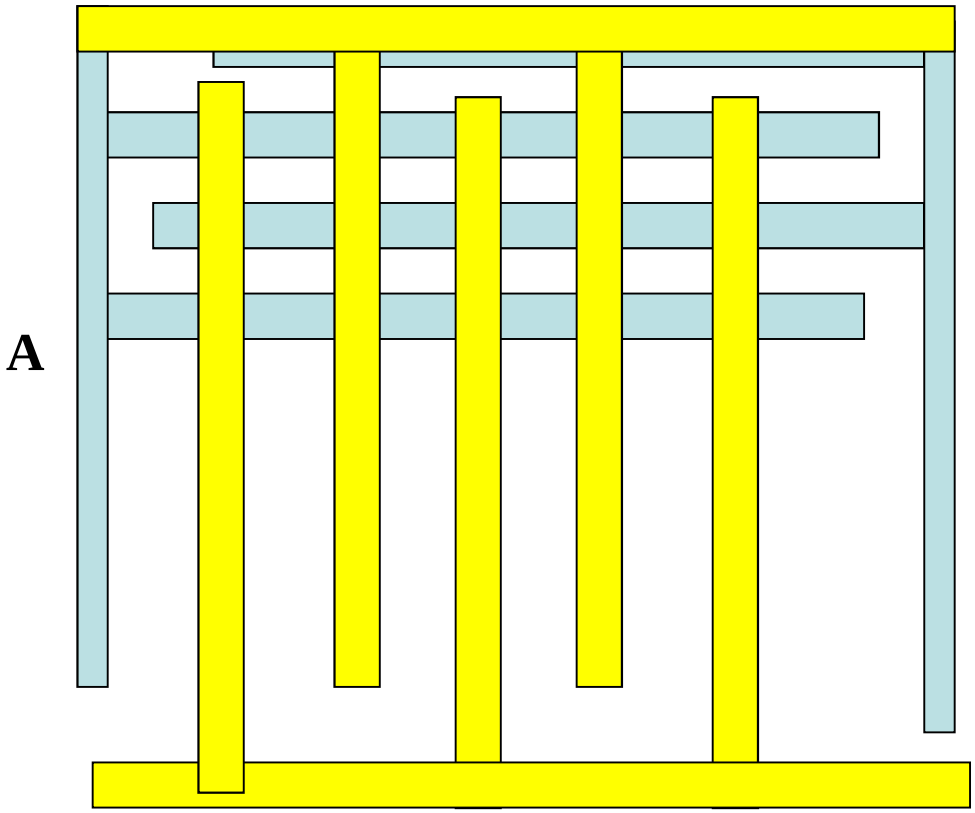
…. Let look at Charges SAR

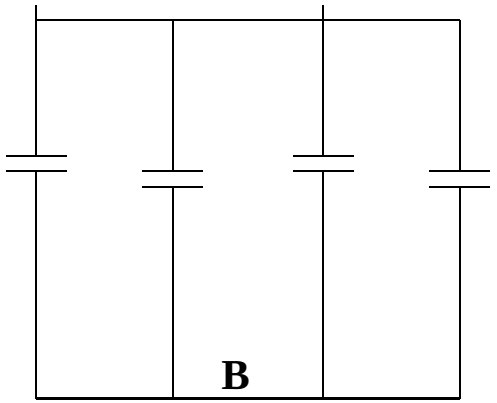


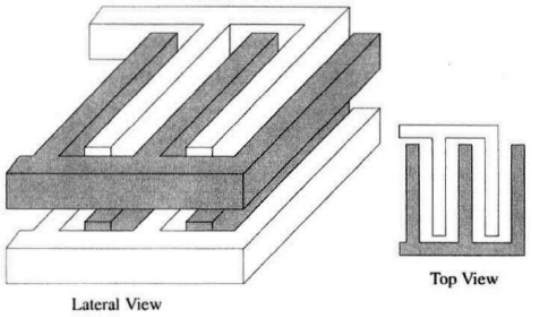
5bit dac

Fring. caps-to improve area density..)

$$C = C_o WL \longrightarrow C = C_o WL + 2C_{fr}(W + L)$$







Accuracy in silicon is low ~ +/-20%
Low temperature/V dependency
Matched well. What about plate parasitic ?

Co= 1-2 ff/uu if Metal to Metal sand witched
With Fringing effect into the picture:

Example: How low can the cap value be ?

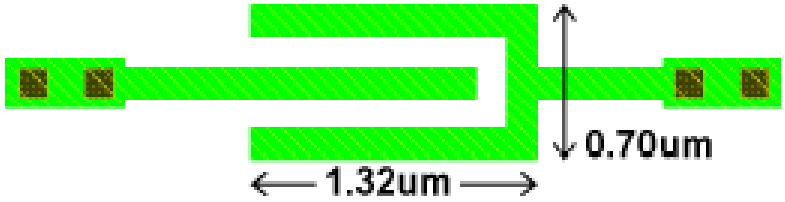


Fig. 3. 0.5fF unit capacitor implementation.

PERFORMANCE COMPARISON.

	[1]	[5]	[6]	This work
Technology	90nm	130nm	65nm	90nm
Power supply	1V	1.2V	1.2V	1V
Power	69μW	0.92mW	1.13mW	26.3μW
Sampling rate	10.24MS/s	50MS/s	100MS/s	10.24MS/s
Resolution	8bit	10bit	10bit	8bit
ENOB	7.8bit	8.5bit	9.5bit	7.7bit
FoM	30fJ/step	52fJ/step	15.5fJ/step	12fJ/step

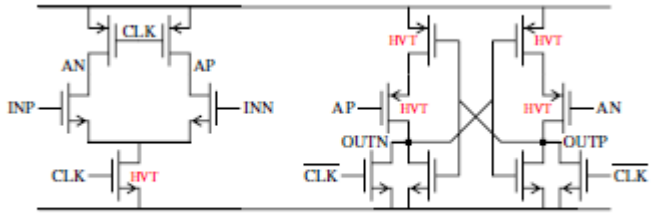


Fig. 4. High-speed, low-leakage dynamic comparator.

A 12fJ/Conversion-Step 8bit 10MS/s Asynchronous SAR ADC for Low Energy Radios

Pieter Harpe, Cui Zhou, Xiaoyan Wang, Guido Dolmans, Harmke de Groot
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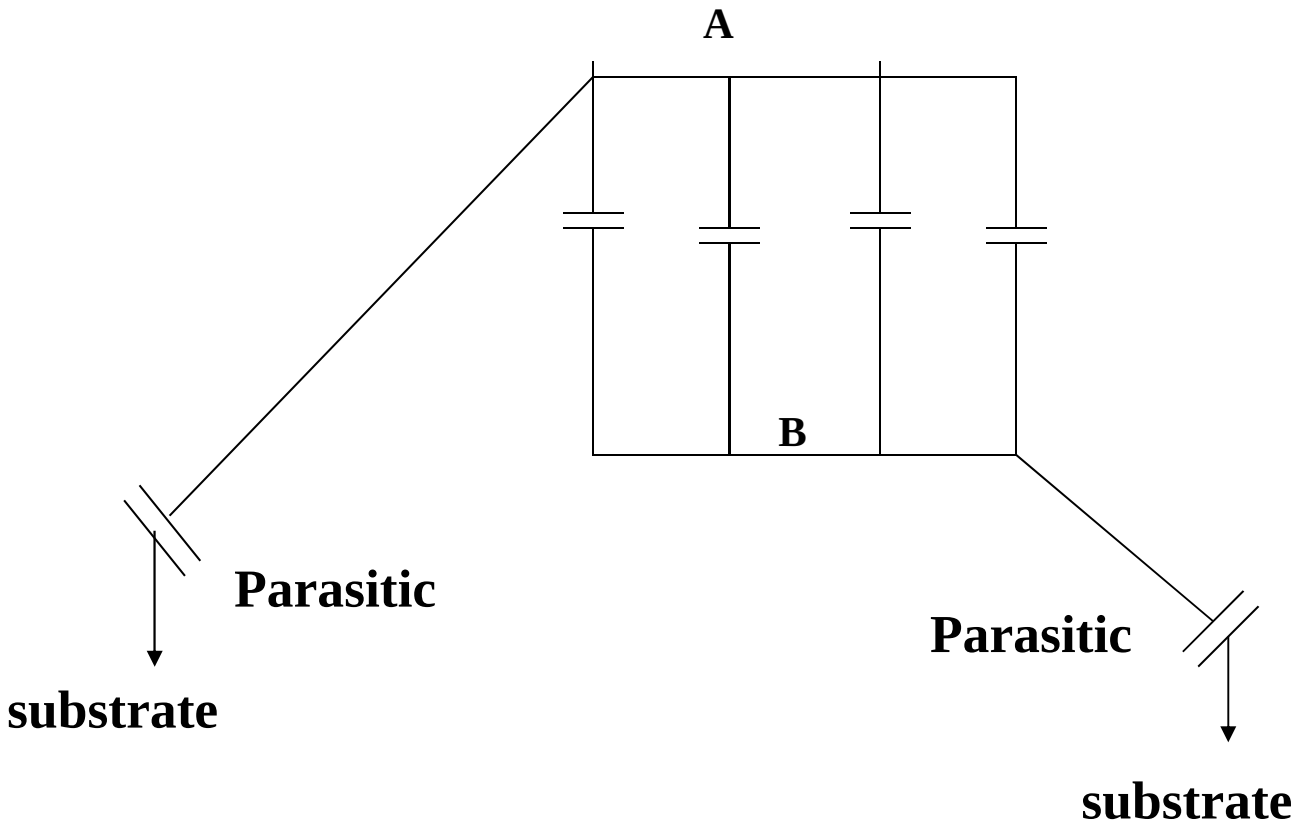
Fring. capacitors-parasitic errors..



C parasitic ~0.1-0.05C total! – how to design it out..

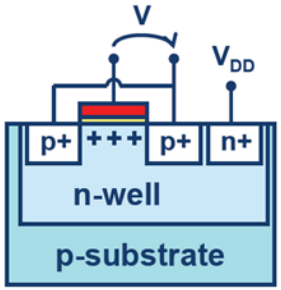
Capacitors from MOS (transistor)→be careful - watch the plates potential.

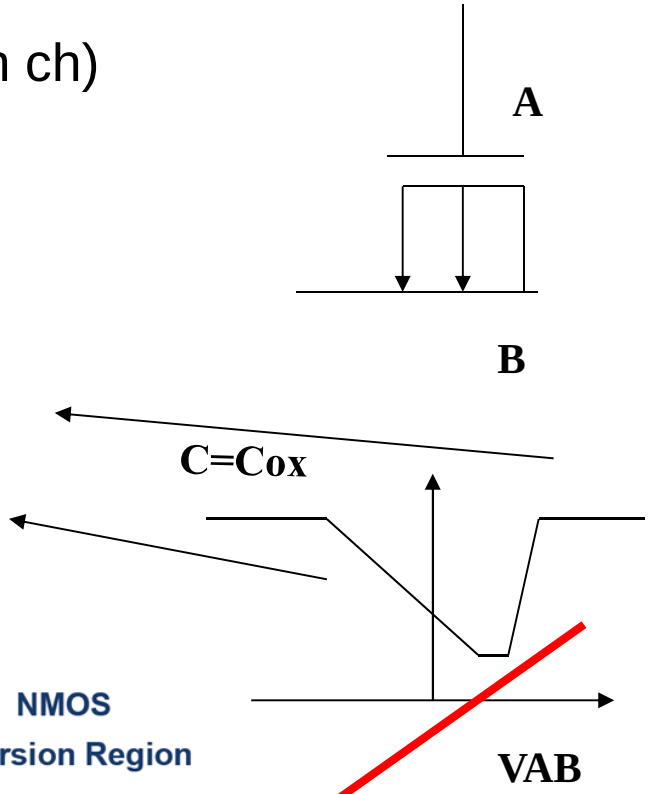
In accumulation (off)-------→ Vgs < Vt (n ch)

$$C = C_o WL$$

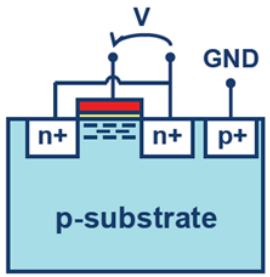
Co ~ 12ff if thin oxide is used (90nm)
Cap is to the substrate (N well probably)
In depletion (on) ---------→ Vgs >Vt

P can be in both

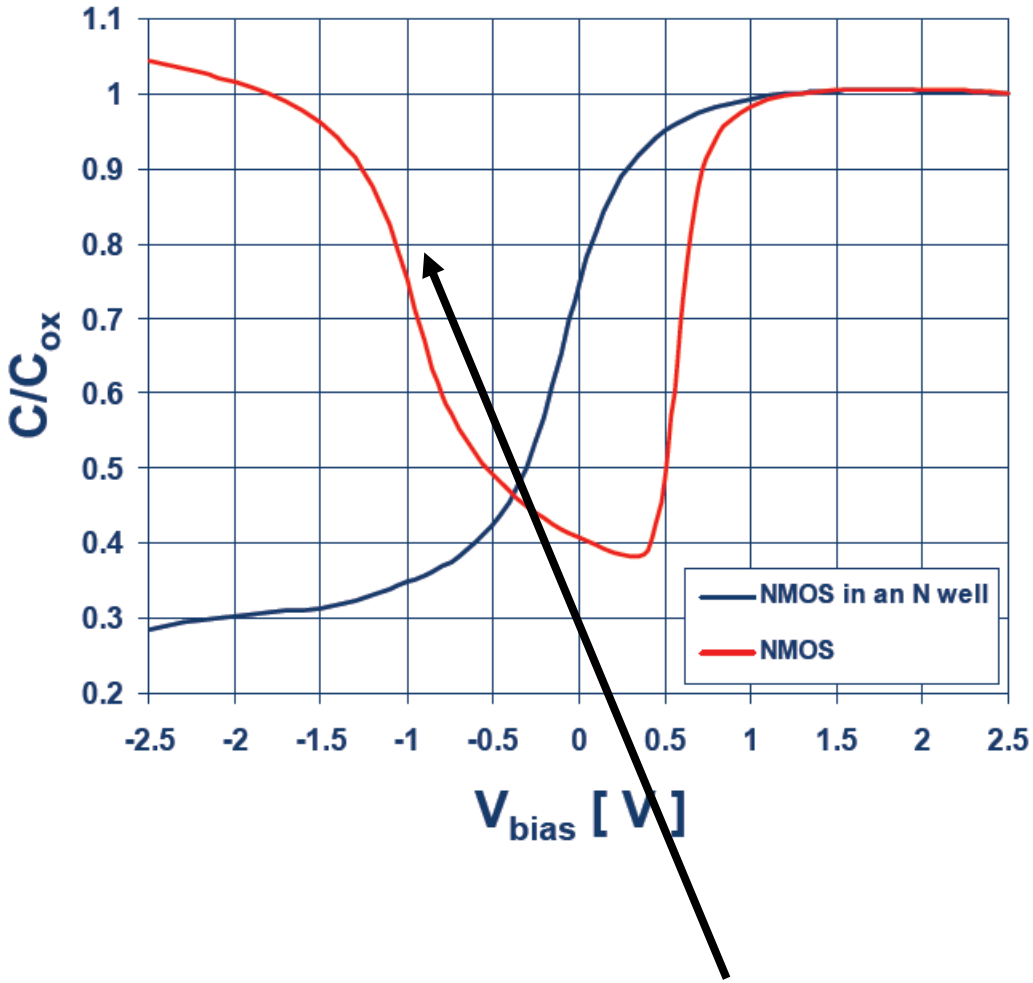




Cap is to the drain sources!
Next to Vt – C drops to ~ 0.3 its max value
It's a voltage dependent capacitor –
doesn't work good with 0 volt across it (integrator and opamp)



Silicon transistors as Capacitors



The NMOS in an N well capacitor is in accumulation for V > 0 V.

The NMOS capacitor is in inversion for V > 0.

Giovanni Anelli, CERN

Oh.. We got cap variable.. ? – ah.. Veractor..

ERRORS IN SAR ADCs

Its an accurate structure

Subtraction using caps
Low/average power: SH, one comparator, DAC, and Logic

8b-200msps is possible

But: Need Accuracy in the DAC.
Comparator offset < ~ 0.5 LSB – Easily calibrated

ACCURACY : FUNCTION OF DAC (CAPACITORS) MATCHING

MATCHING

$$C \approx \varepsilon \frac{WL}{t} \longrightarrow \left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

Once again can correlate to area with good accuracy
How is it given

1. A_deltaC/C is based on sigma of (deltaC / C)vs. 1/sqrt(WL)
typ. number 2fF/micron square

To get to the best matched number you need to :

- Use identical geometries
- Use large unity capacitance (minimize fringing)
- Use common centroid arrangement
- Use dummy capacitors
- Use shielding
- Account for the connections' contribution
- Don't run connections over capacitor
- Place capacitor in low stress areas
- Place capacitors far from power devices

ON BOARD EXAMLE

Find the LSB capacitor size (and total capacitors)
for a 12b SAR ADC Given that 10ff unit match to 0.8%. (to 1 sigma)

$C_{UNIT} = 10fF$, $\left(\frac{\Delta C}{C}\right)_{UNIT} = 0.8\%$

$$\Delta_{noise} = \sqrt{\frac{\Delta^2}{12} + \{DISTORTIONS\}^2 + \frac{kT}{C_T}}$$

1pF ~ 64e-6V/sqrtHz

Let GIVE $\{DISTORTIONS\}$ - 1/3 LSB weight.

$$\left\{\frac{\Delta C}{C}\right\}_{F.scale} = \frac{1}{3}\left[\frac{1}{2^n - 1}\right] = 0.0081\ \%$$

LSB can be a LOT worst, its scale by $\frac{1}{\sqrt{A}} - \frac{1}{\sqrt{\cdot}}$

$$\left\{\frac{\Delta C}{C}\right\}_{LSB} = [0.0081] \cdot \sqrt{2^n - 1} = 0.518\ \%$$

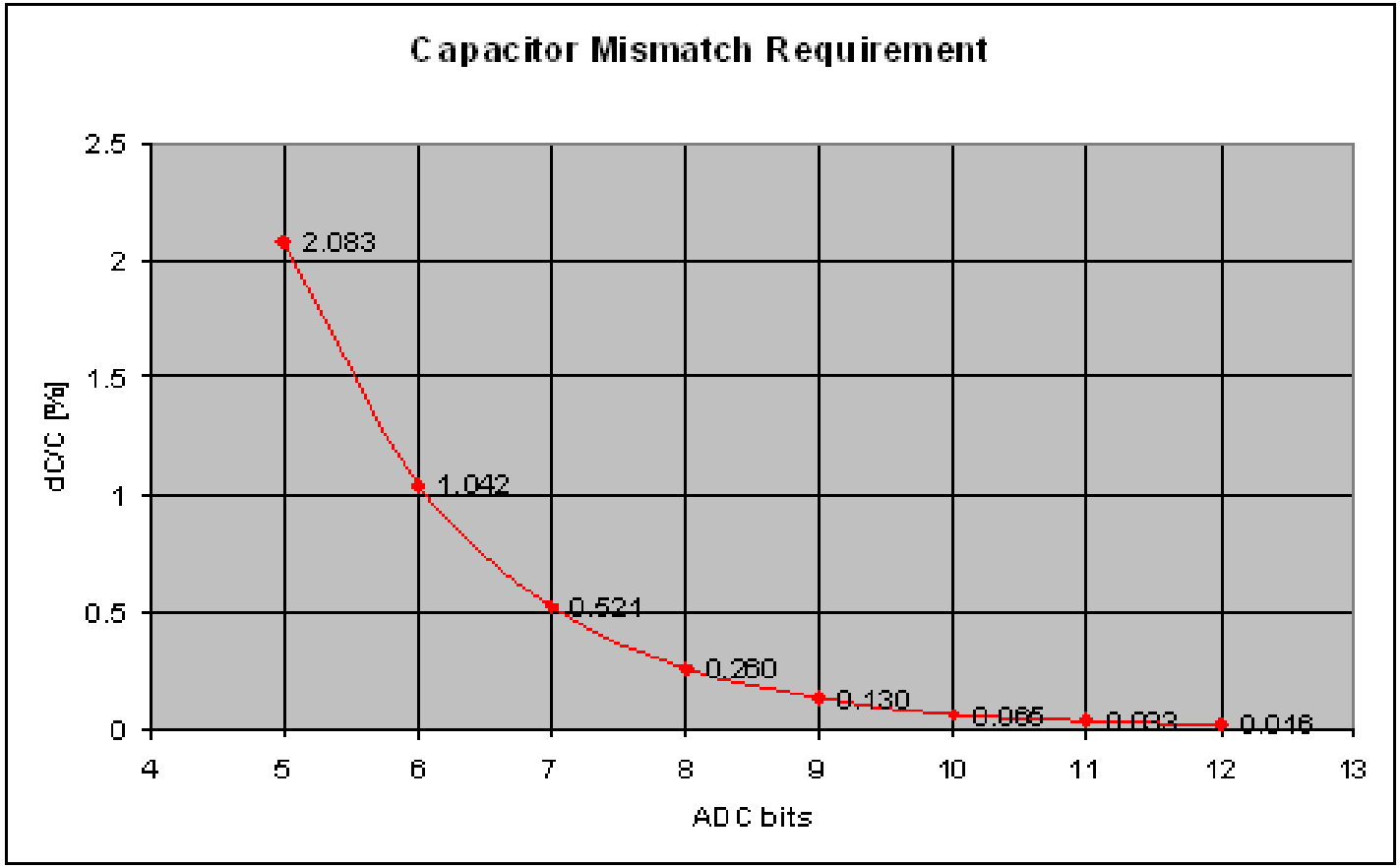
$$C_{LSB} = [C_{UNIT}]_{//}^{10fF} \cdot \left[\frac{0.8}{0.518}\right]^2 = 23.85\ fF$$

$C_{TOTAL} = 97.67pF$

NOT TO INFLUENCY the converter. !

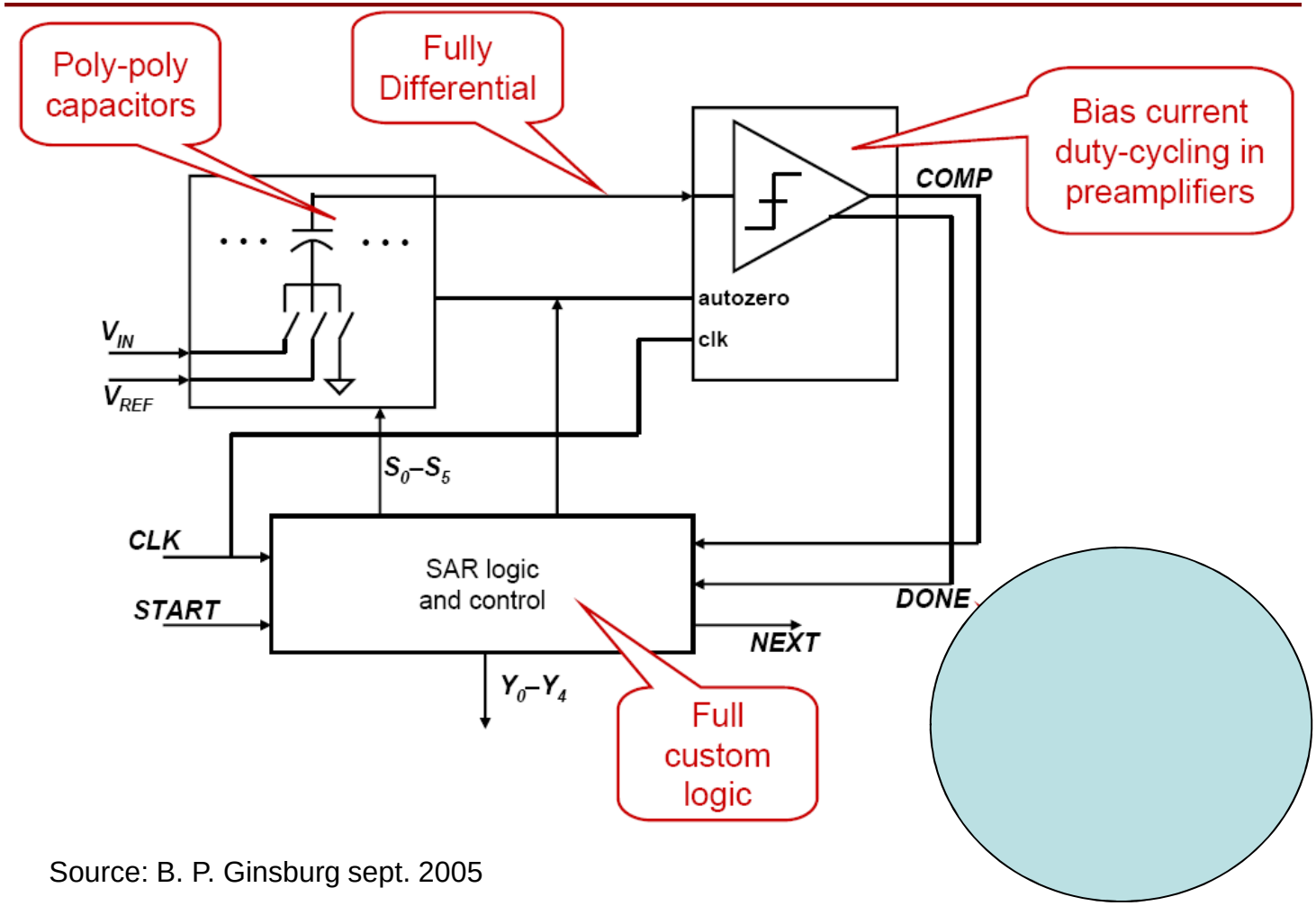
$$C_{LSB} = [C_{UNIT}] \cdot \frac{\left[\left(\frac{\Delta C}{C}\right)_{F.scale} \sqrt{2^n - 1}\right]^2}{\left[\left(\frac{\Delta C}{C}\right)_{UNIT}\right]^2}$$

Example of matching requirement on F. Scale (MSBs)



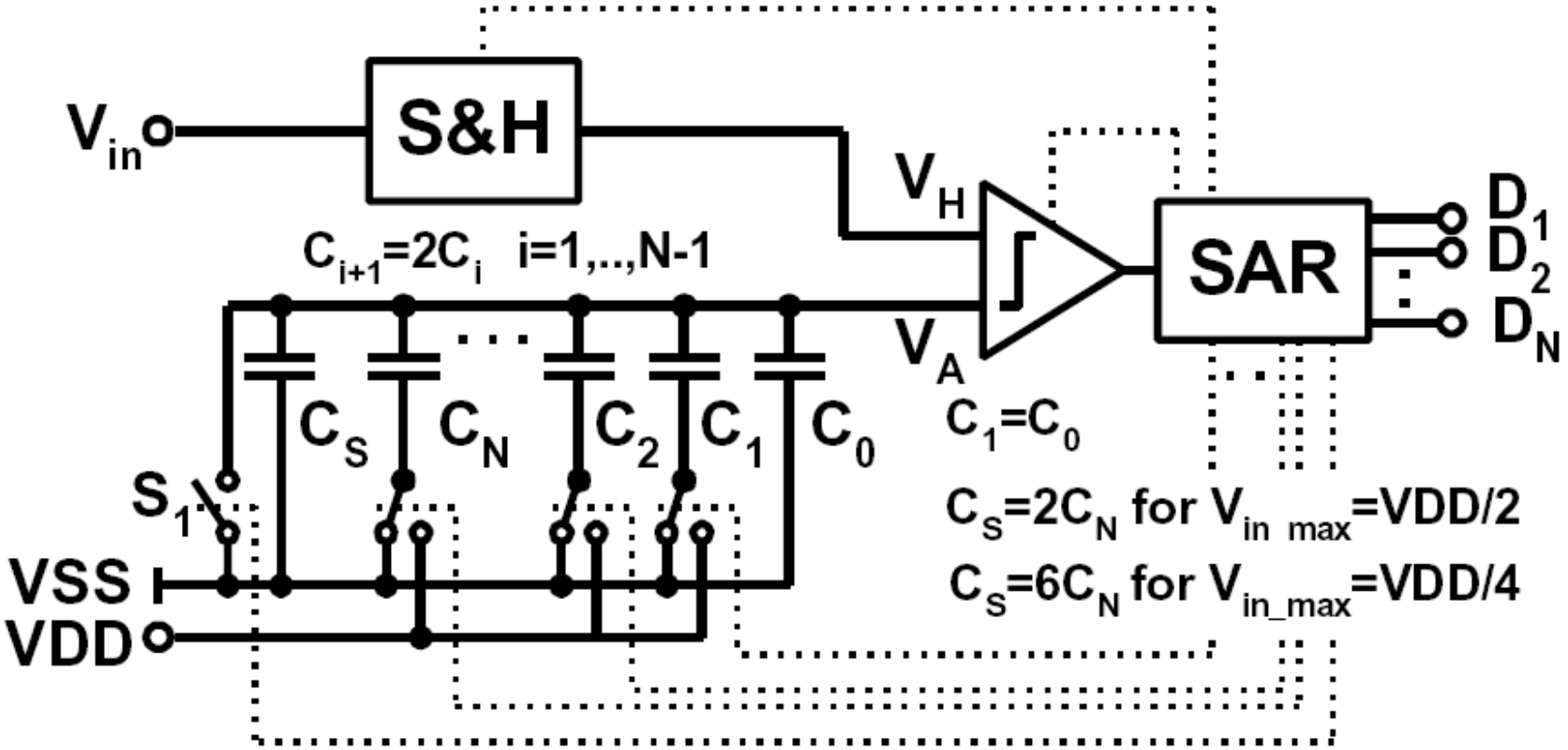
2 to the n x 2/3
(2/3 only as example not to give all the error to the linearity)

HOW TO BUILD ONE – WHAT TO LOOK FOR



Source: B. P. Ginsburg sept. 2005

Design Examples:

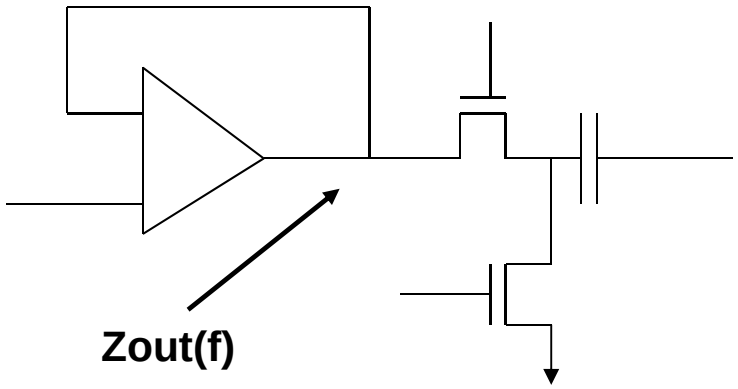


Key: Word on the references

References issues:

REFERENCE HOLDING BREF IS HARD TO DO:
During switching phase references
has to settle every clock (fast) They are op amp
driven therefore make the design almost as op-amp based

Also the comparator must settle every cycle. (faster)



Summary- C or R dac

Most time absolute value can move =+/-15% to +/-20%
and does not significantly matter but ratio's do

However, the bigger the area the better the matching
Typical values 30ff can match 3-sigma to better ~ 0.5%
Matching is area dependent generally by the root of (W x L)

In SAR there is contradiction large is good for matching however speed is degraded a lot R switch x C and its multiplied N bit for a complete cycle.

POWER/Analog componets

Without amplifiers power is set by S/H, References, 1 comparator, and digital blocks+clocks

Generally for lower number of bits – logic may be significant Area. For many bits analog set the power waist.

Logic running multiple times for each conversion and capacitor size (forcing a large drive current)

Power waist : S/H + Comparator + Refes+switching/logic

Good:
Lowest possible power- FOM
Fewer analog elements,
T/H or S/H drive low capacitance

SAR- Key Points

The Feed Back ADC (SAR) offers significant hardware savings
compared to flash ADCs because the coarse quantizer (comparator)
resolution m can be much smaller then the converter resolution. N

However, its suffer from drawbacks making it not suitable for many applications because:
It requires p= N/m passes to generate N bit output words limiting the through put
It requires N; bit accurate DAC

It requires faster settling elements

but No need amplifiers !

So if speed is a problem should we combine SARs in time ??

End Lecture 9

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