Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

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TEL AVIV UNIVERSITY אוניברסיטת תל אביב

Lecture 9

LC-PLLs and CDR Architectures

PLL- Loop stability and Jitter (transfer function)

Design Example

Lectures are placed in my site:
http://www.gigalogchip.com/lectures.html

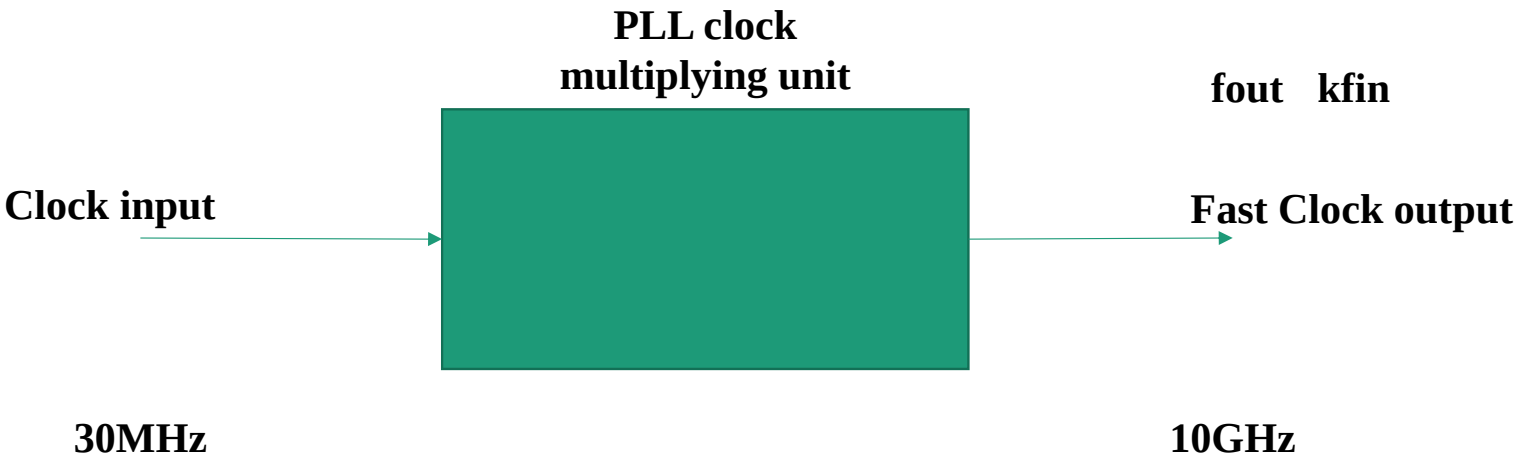
In the below site..

2 assignments, project example, all lectures
Send assignment please to my mail
miki@gigalogchip.com
can ask questions if confused.. using whats app or phone..

Lectures are placed in my site:
http://www.gigalogchip.com/lectures.html

Architecture

Motivation



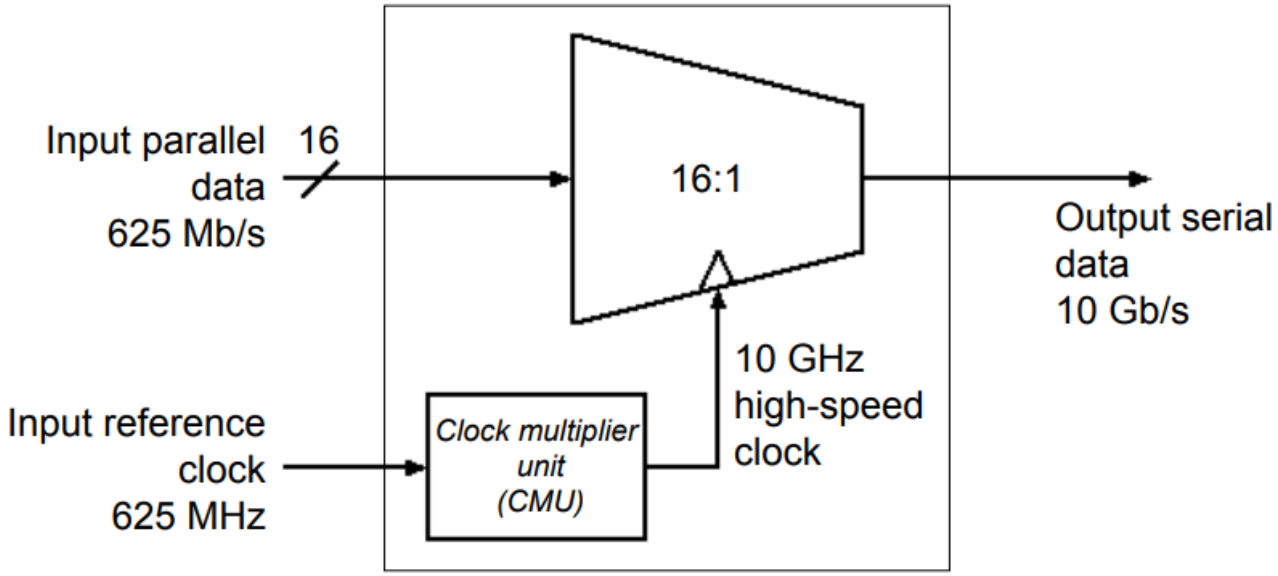
Generates almost any clock (fractional
easy to input slow clock to pass the heavy pads
genarte local clocks at all freq. On chip
filter noise- jitter
LC pll are specially clean, useful for over 1GHz

most SOC chips are designed with a PLL

Example in use for SerDes

Synchronization Using Phase-Locked Loops

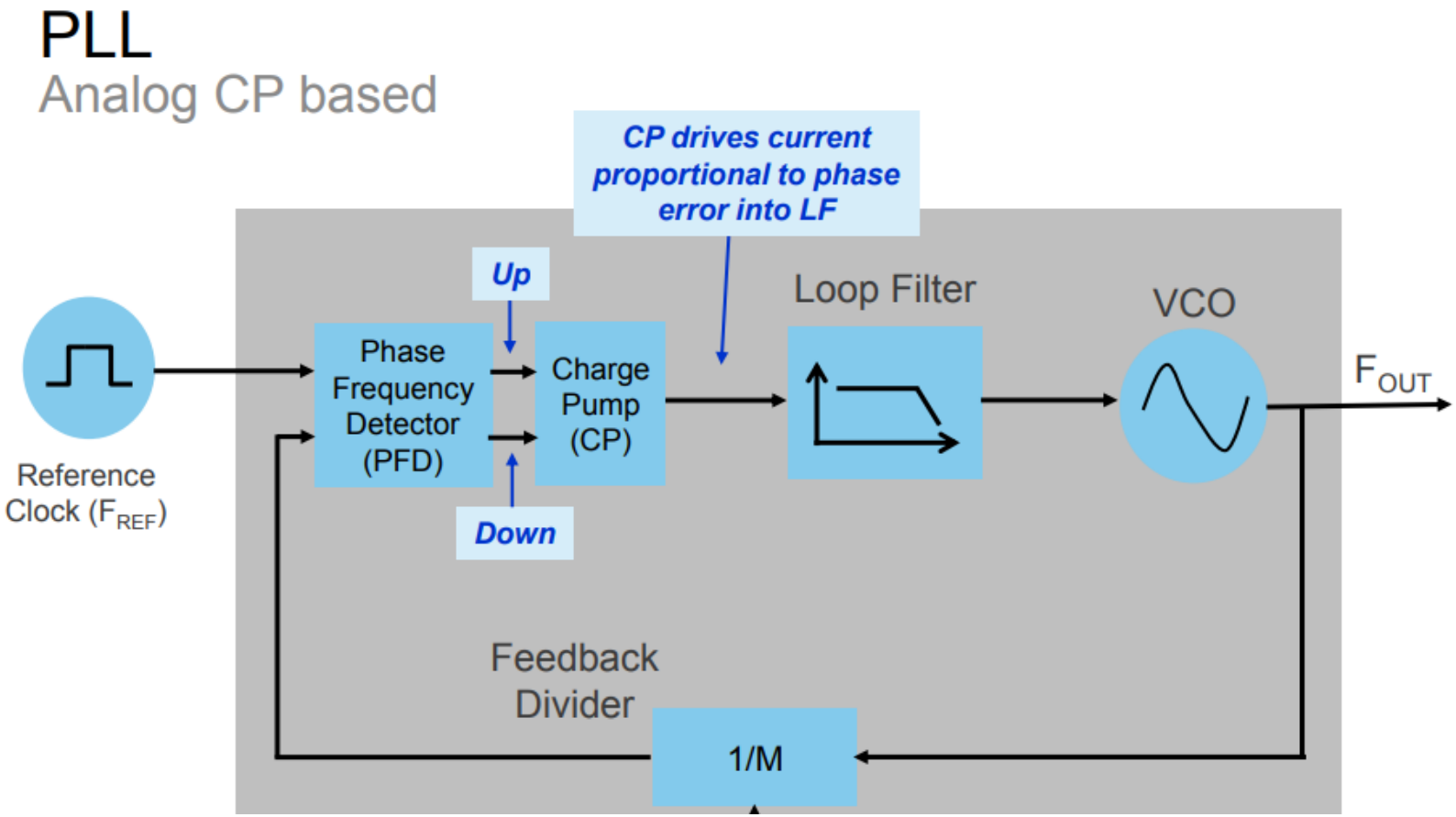
Example: 16:1 Multiplexer



How can we generate the 10 GHz clock to be synchronized with the 625 MHz reference clock?

Prof green

Basic loop

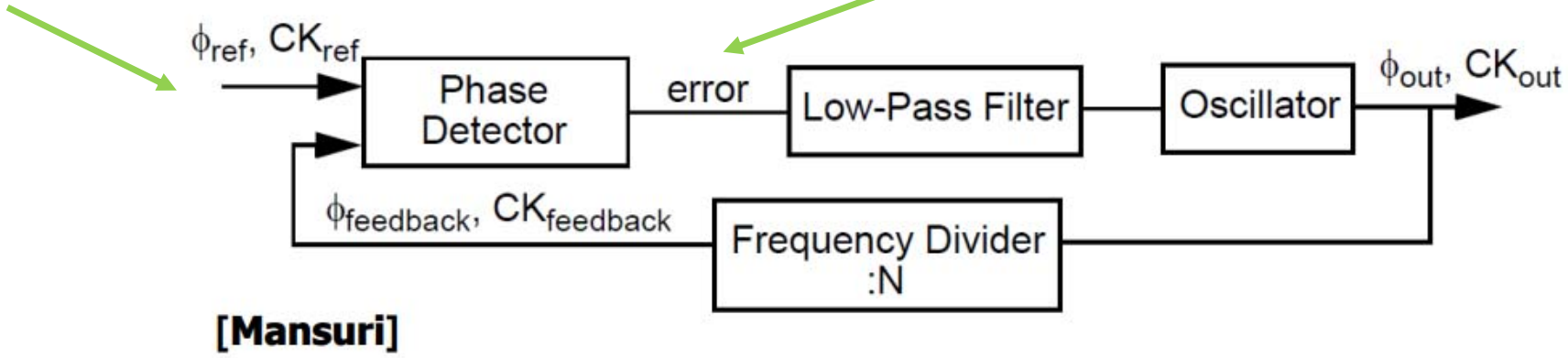


cadence

Basic loop

$$\phi(t) = \underbrace{K_m K_1 A}_{K_D} \sin\left[\theta(t) - \hat{\theta}(t)\right] \overset{\text{small error}}{\approx} K_D\left[\theta(t) - \hat{\theta}(t)\right]$$

$\sqrt{2}A\sin[\omega_0 t + \theta(t)]$



[Mansuri]

What is the loop order ?

PLL loop is about phases.
It must lock on phases and frequency
the integral of the phase relates to freq

Basic types

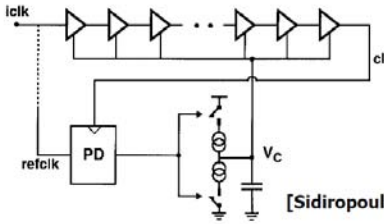
There are basically 2 types
1 APLL after the phase detection we uses analog circuits

2 DPLL after the phase detection we use counters and digital filter and change digitalz the VCO
DPLL are dificult but the advantage is loop filters can be set to low frequency can be adujted fast to other values.

DLL are also sub versions of PLL – whats good in them ?

APLL are the subject of this lecture.

Delay-Locked Loop (DLL)



[Sidiropoulos JSSC 1997]

- DLLs lock delay of a voltage-controlled delay line (VCDL)
- Typically lock the delay to 1 or ½ input clock cycles
  - If locking to ½ clock cycle the DLL is sensitive to clock duty cycle
- DLL does not self-generate the output clock, only delays the input clock

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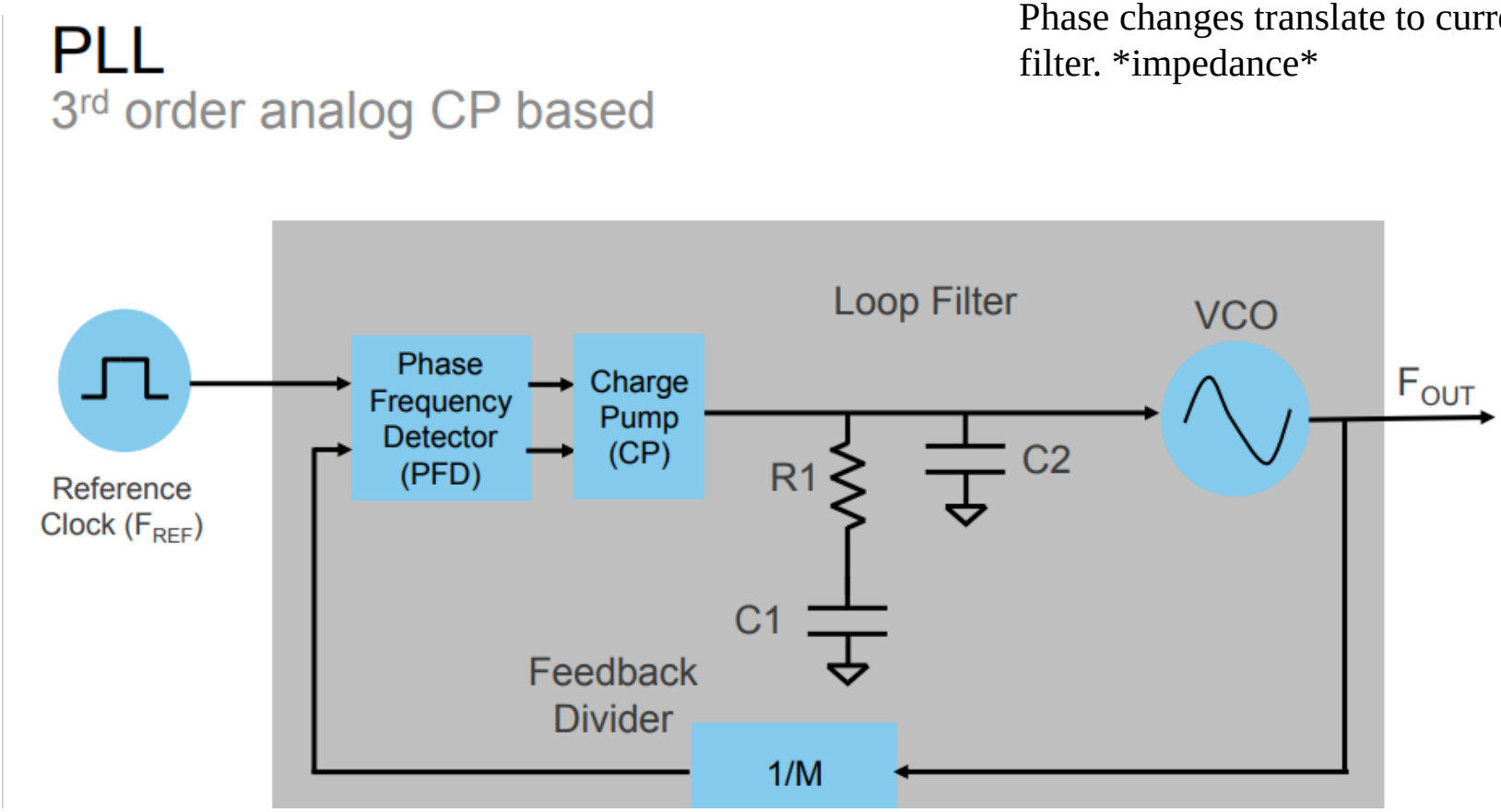
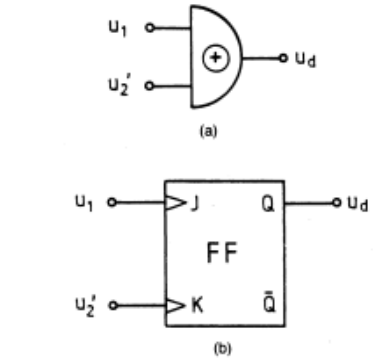
APLL Mixed mode

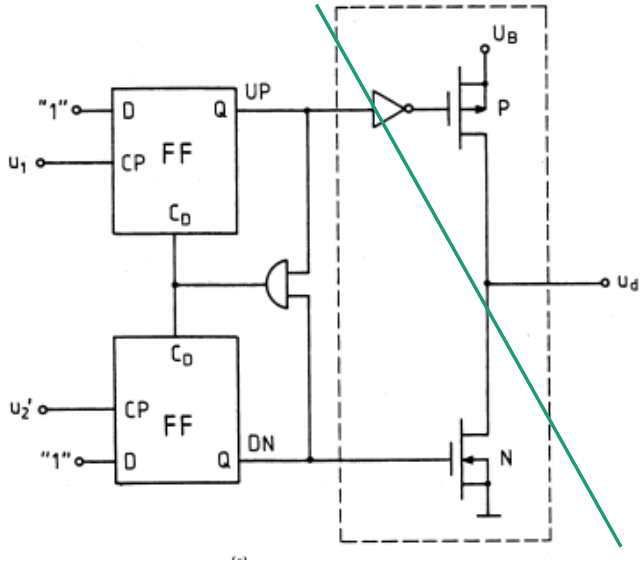
we add a –convertor- called charge pump
Phase changes translate to current dumped onto loop filter. *impedance*



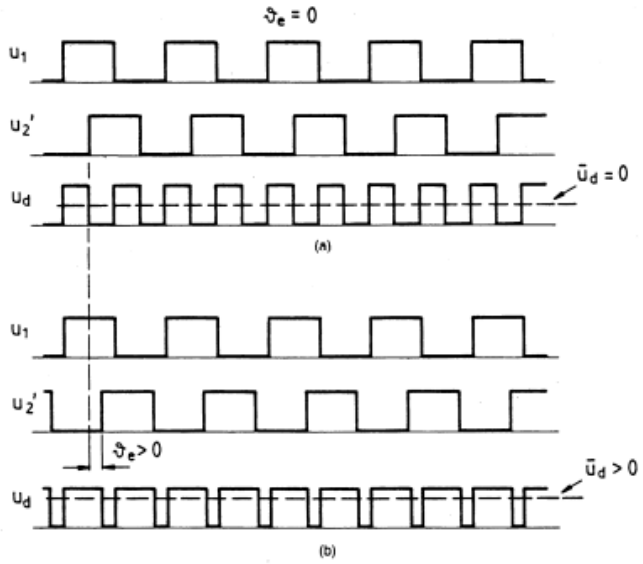
- Popular types of digital phase detectors include:
  - Exclusive or gate (EXOR)
  - Edge-triggered JK-flipflop
  - Phase frequency detector (PFD)



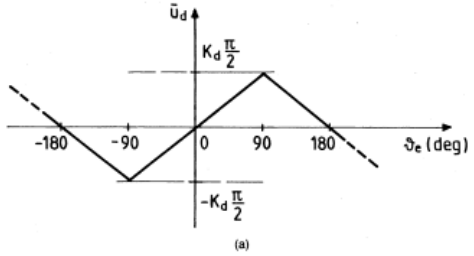
PFD type 4



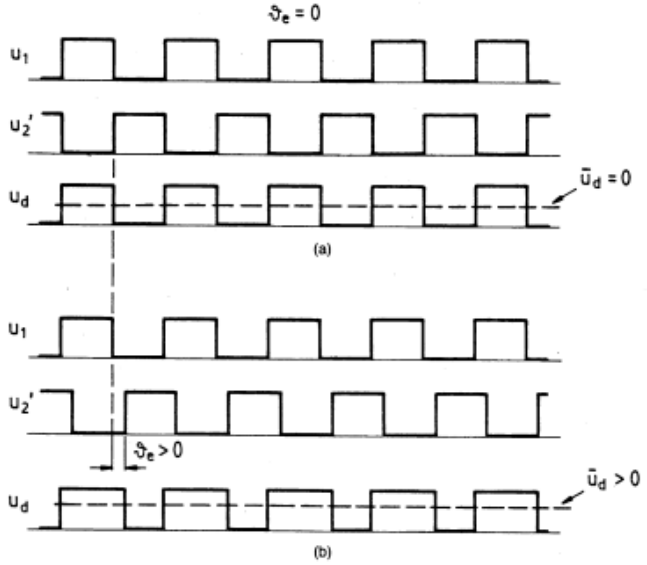
XOR



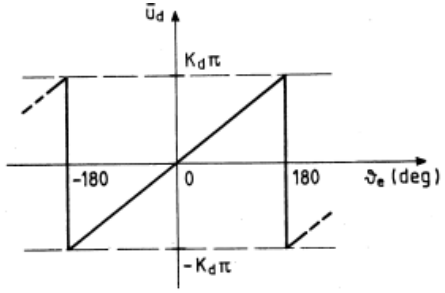
Kd = Vdd by PI



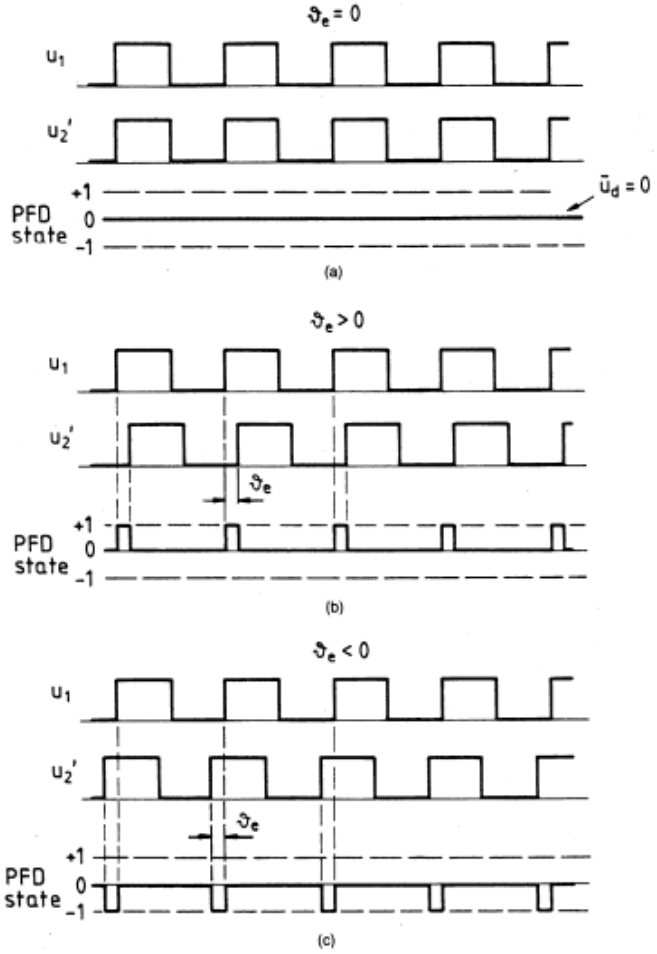
J/K FF



Kd = Vdd by 2PI

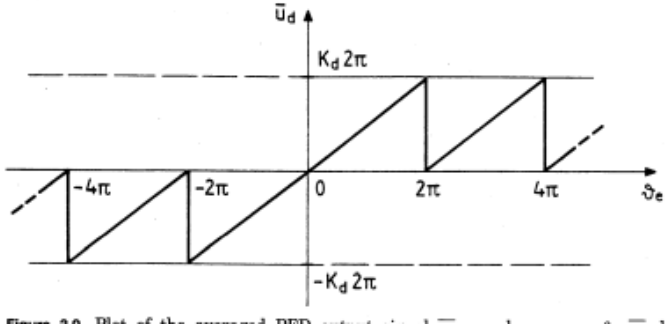


PFD type 4



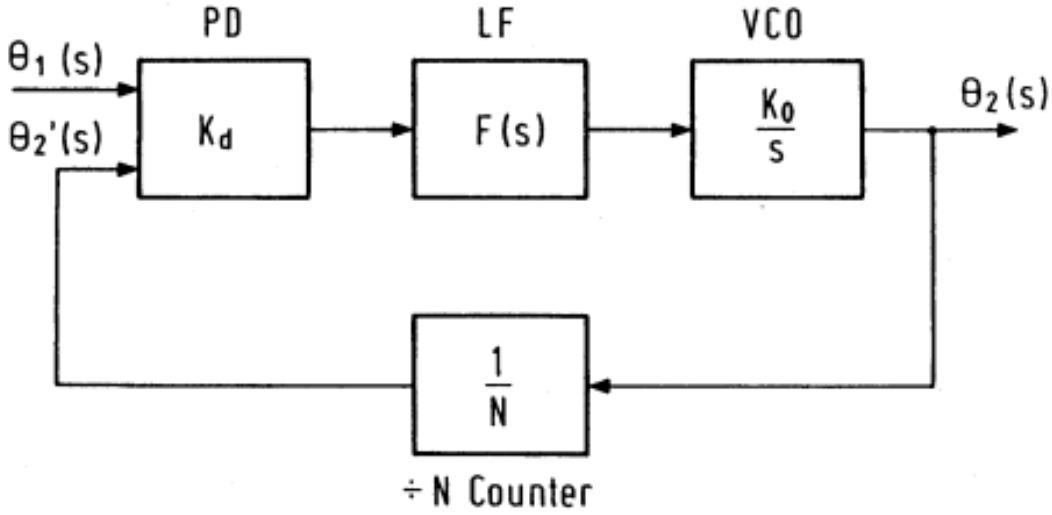
Can pfd4 make mistake miss ? – yes..

Kd =VDD / 2PI



We dont want to dpend on VDD so change to I With CP

Transfer function



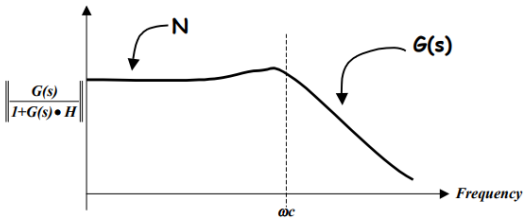
$$\frac{G(s)}{1+G(s)\bullet H}$$

H equal 1/N

Valid only in relation filter pole frequency to input clock frequency

Input frequency ~ 20 time farther than loop filter..or more

Under 20 need transiend or descrete analzsis Some reports say even 8X can pass.



Transfer function

phase detector : $F_{PFD} := I_p$

Stability analysis

feed back counter : $F_N := \frac{1}{Div}$

loop filter :

$$F_{LF}(s) := \frac{\left(R + \frac{1}{s \cdot C_1}\right)\left(\frac{1}{C_2 \cdot s}\right)}{R + \left(\frac{1}{s \cdot C_1}\right) + \left(\frac{1}{C_2 \cdot s}\right)}$$

VCO : $F_{VCO}(s) := \frac{K_o}{s}$

forward transfer function : $A(s) := F_{PFD} \cdot F_{LF}(s) \cdot F_{VCO}(s)$

feed back transfer function : $B(s) := F_N \cdot e^{-s \cdot Per}$

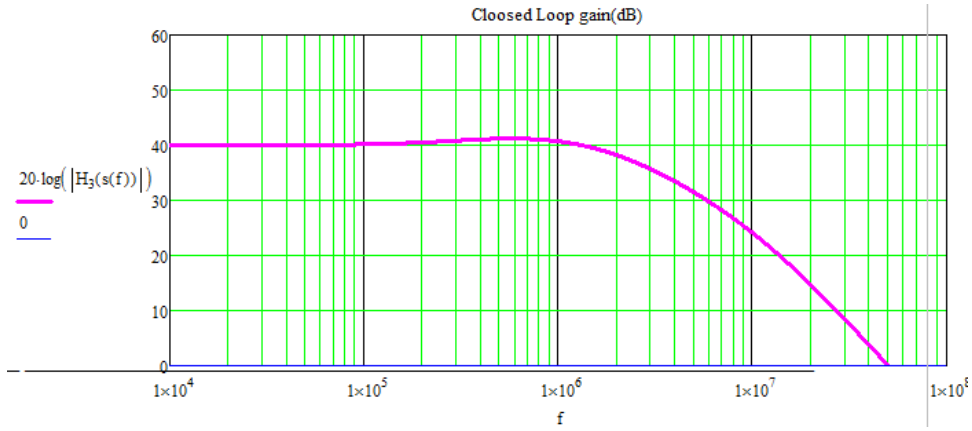
over all transfer function : $H_3(s) := \frac{A(s)}{1 + A(s)\,B(s)}$ (non normalized to 0db)

open loop transfer function : $G(s) := A(s) \cdot B(s)$

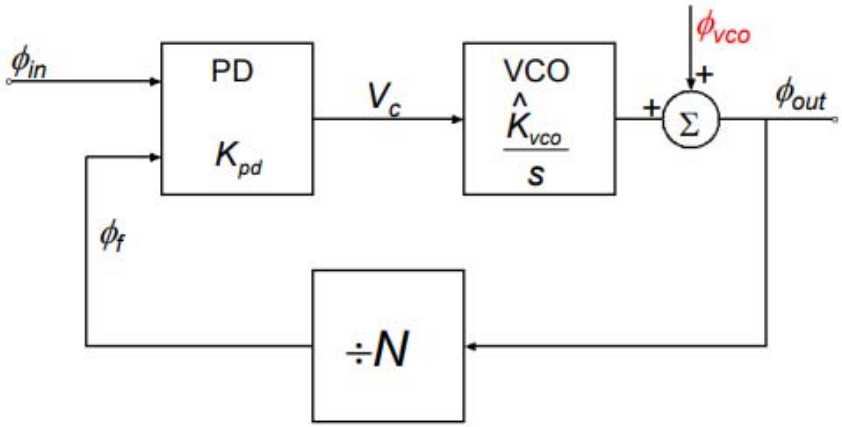
$s(f) := 2 \cdot \pi \cdot f \cdot i$

zero $f_z := \frac{1}{2 \cdot \pi (R \cdot C_1)}$

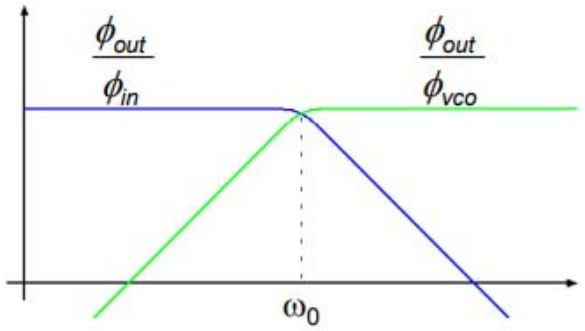
pole $f_p := \frac{(C_2 + C_1)}{2 \cdot \pi R \cdot (C_2 \cdot C_1)}$



Jitter Transfer Functions



$$\phi_{out} = \underbrace{\frac{N}{1+s\frac{N}{K}}}_{\text{lowpass characteristic}} \cdot \phi_{in} + \underbrace{\frac{s\frac{N}{K}}{1+s\frac{N}{K}}}_{\text{highpass characteristic}} \cdot \phi_{vco}$$



13-15 January 2008
הטכניון
Israel Institute of Technology

Prof. Michael Green

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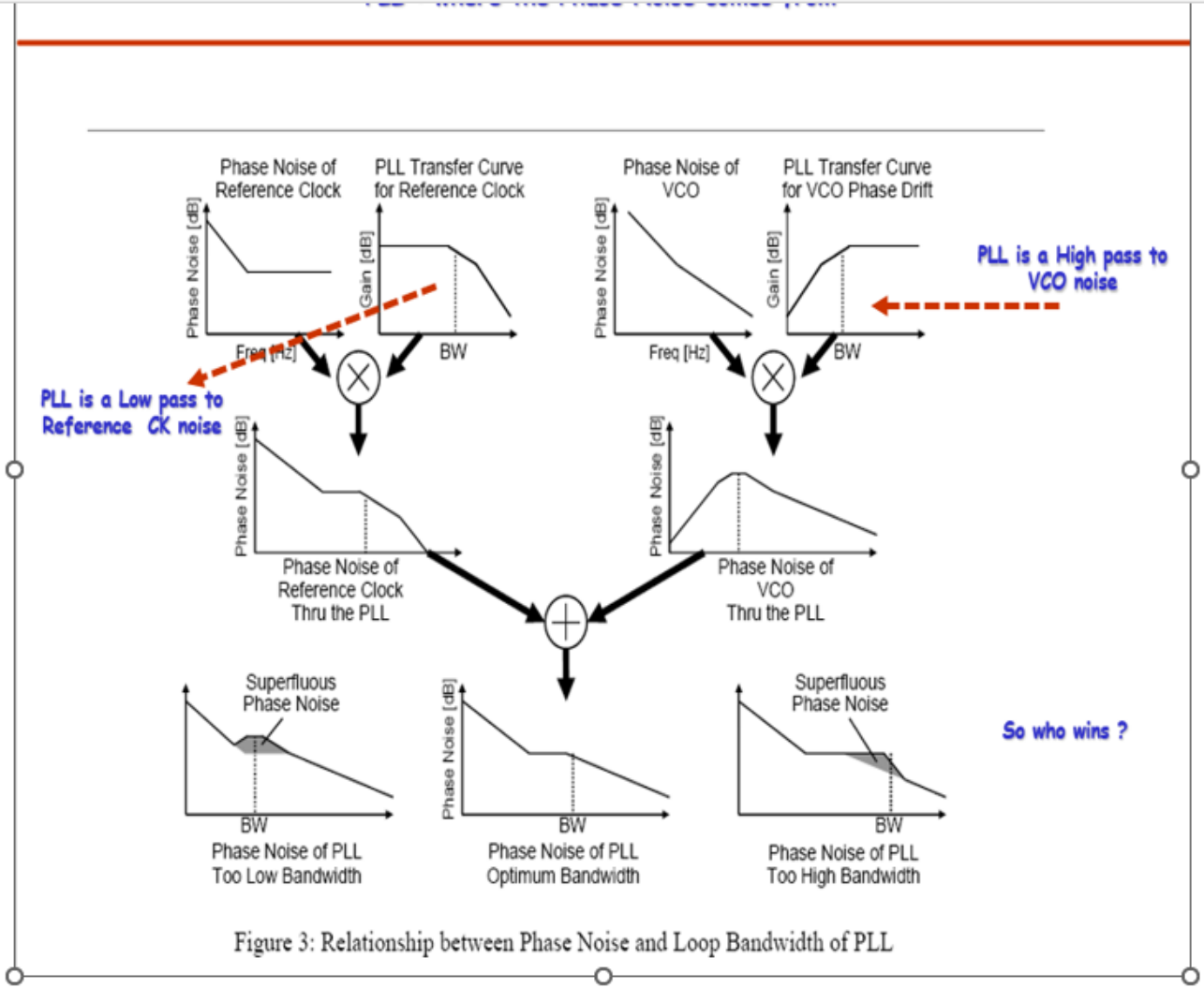
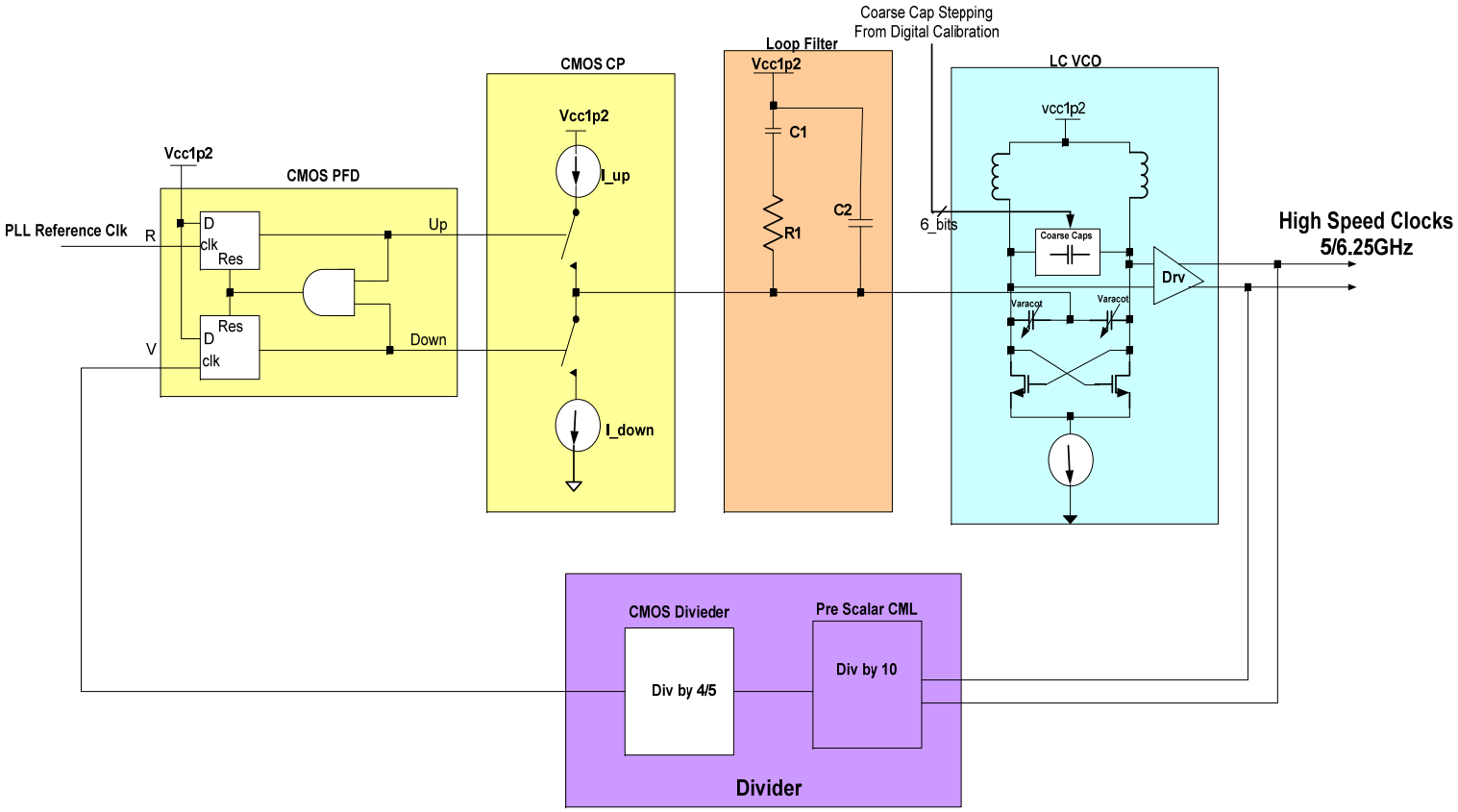


Figure 3: Relationship between Phase Noise and Loop Bandwidth of PLL

Figure 50: View of all noise effects

PLL Simple Block Diagram



PLL Spec For PCI-GEN II

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage	Simulation Condition	1.08	1.2	1.28	[V]
Temperature	Simulation Condition	0	60	120	[Deg C]
Clock Input	External Oscillator		100		[MHz]
Output Frequency			5		[GHz]
Rj			0.6		[ps RMS]
Target Bandwidth		5	7	10	[MHz]
DJ			10		[psec]
PLL Peaking			0.5	1	[dB]
Duty Cycle			49/51		[%]
Output Amplidute	CML	0.32	0.4	0.6	[V ptp]
Total Power Consumption			140		[mW]

SYSTEM CHARACTERISTICS

-3dB closed loop bandwidth with internal filter: **750 kHz**
-3dB closed loop bandwidth with external filter: **100 kHz**

Peaking with internal filter **< 0.8dB**
Peaking with external filter **< 0.01dB**

Locking time: **12µs**
Locking time in clean-up mode: **4.3 ms**

Maximal Capture range: **147MHz-180MHz**

Example of design system 2 block

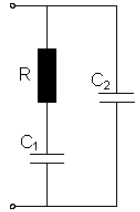
CIRCUIT DESCRIPTION

Internal loop filter	resistor: **15 kΩ** capacitor: **250 pF** glitch capacitor: **7pF**
External loop filter	resistor: **1.8 kΩ** capacitor: **122 nF** glitch capacitor: **10 pF**
VCO	continuous tuning range: **500 MHz** discrete tuning range: **1.5 GHz** gain K_{VCO}: **600 MHz** phase noise @ 500 kHz with LF: **-95 dBc/Hz**
Charge pump	charge pump current: **40 µA**

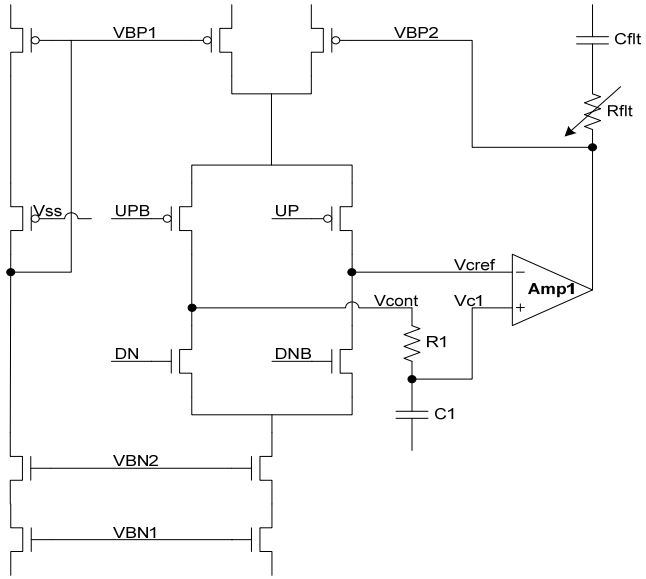
LOOP STABILITY

Position of f_z and f_p?
Choice of R, C_1, C_2?

- Open Loop PM ≥ 0°
- Peaking < 1dB
- Phase Noise
- Loop Capacitor Area



Charge pump block diagram



- **Rout from Amp1 and Cflt contribute a Pole**
- **Rout2 and Cout2 of net Vcref1 contribute a Pole that varies according to CHPMP current and operating point**
- **Cflt & Rflt contribute a Zero**
- **Rflt can be adjusted to match CHPMP current (Rout2 and Cout2)**

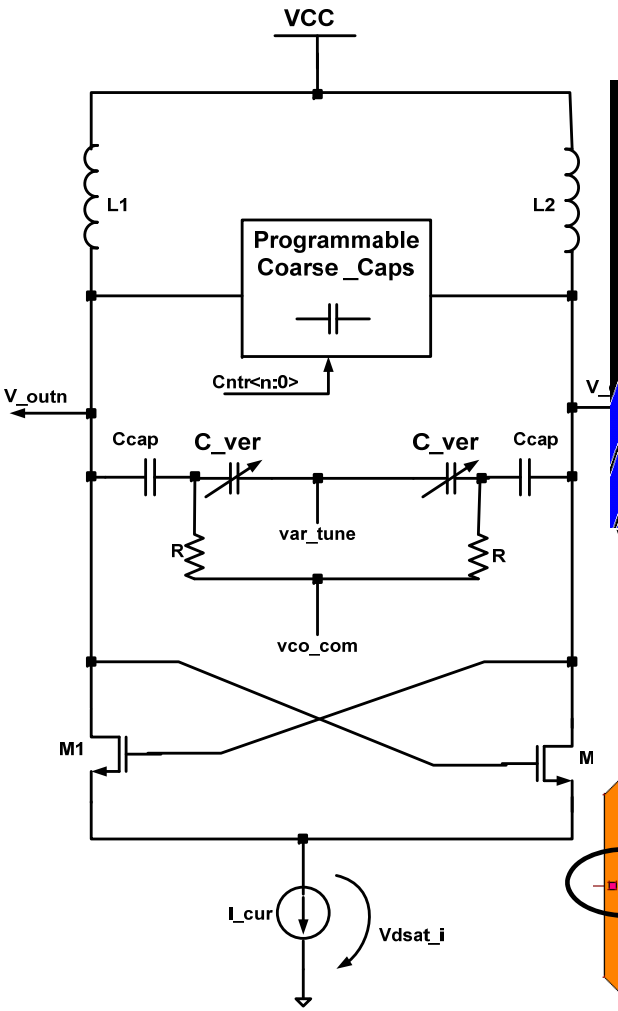
- **Fpole1~6KHz (Rout~3M[ohm], Cflt~10p[F])**
- **Fzero2~6MHz (Rout2 & Cout2)**
- **Fpole2~6MHz (Rflt & Cflt)**

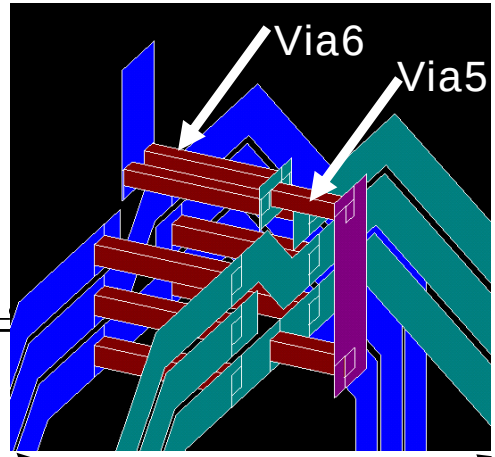
Design SPEC

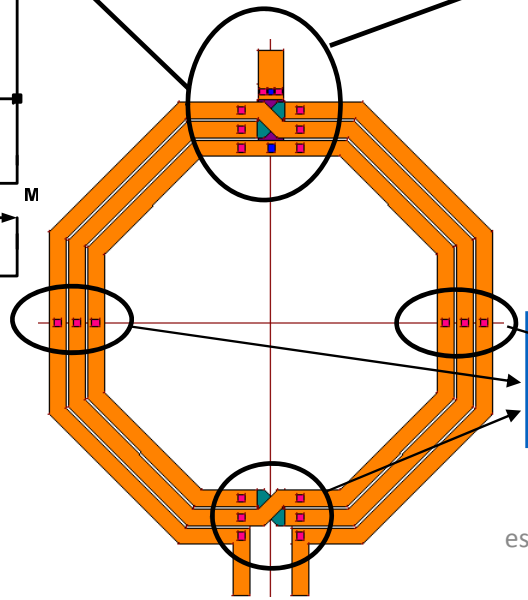
Parameter	Default	Span	Step	Corner
Icp	400uA	25uA→ 800uA	+/- 25uA	+6%, -15%
Cflt	10pF			+/-10%
Rflt	1.7	1.7K→53	+/-1.7K/32	+/-15%
Pole1	6KHz			

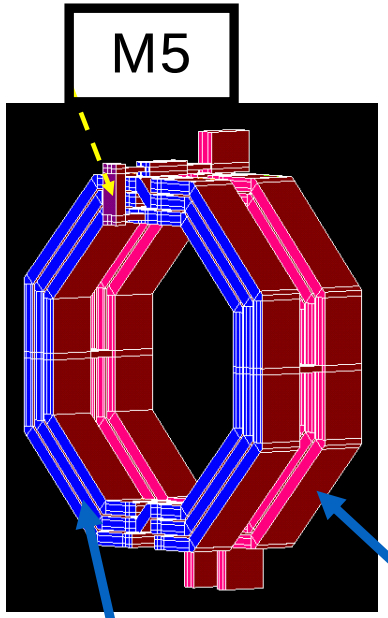
Potential Hazard:
CHPMP Loop Stability (Phase Margin)
VC1 values (in locked condition) will vary according to VCO corner (center frequency and Kvco) thus changing operating point of Nmos and Pmos current sources in the CHPMP (and the effective output resistance, Rout2). Since Pmos output resistance is much smaller it will be the main contributor to the output resistance:

VCO Inductor Model









M6

M7

Each square is a count of 20 via6

W=3.8 um

S=0.6 um

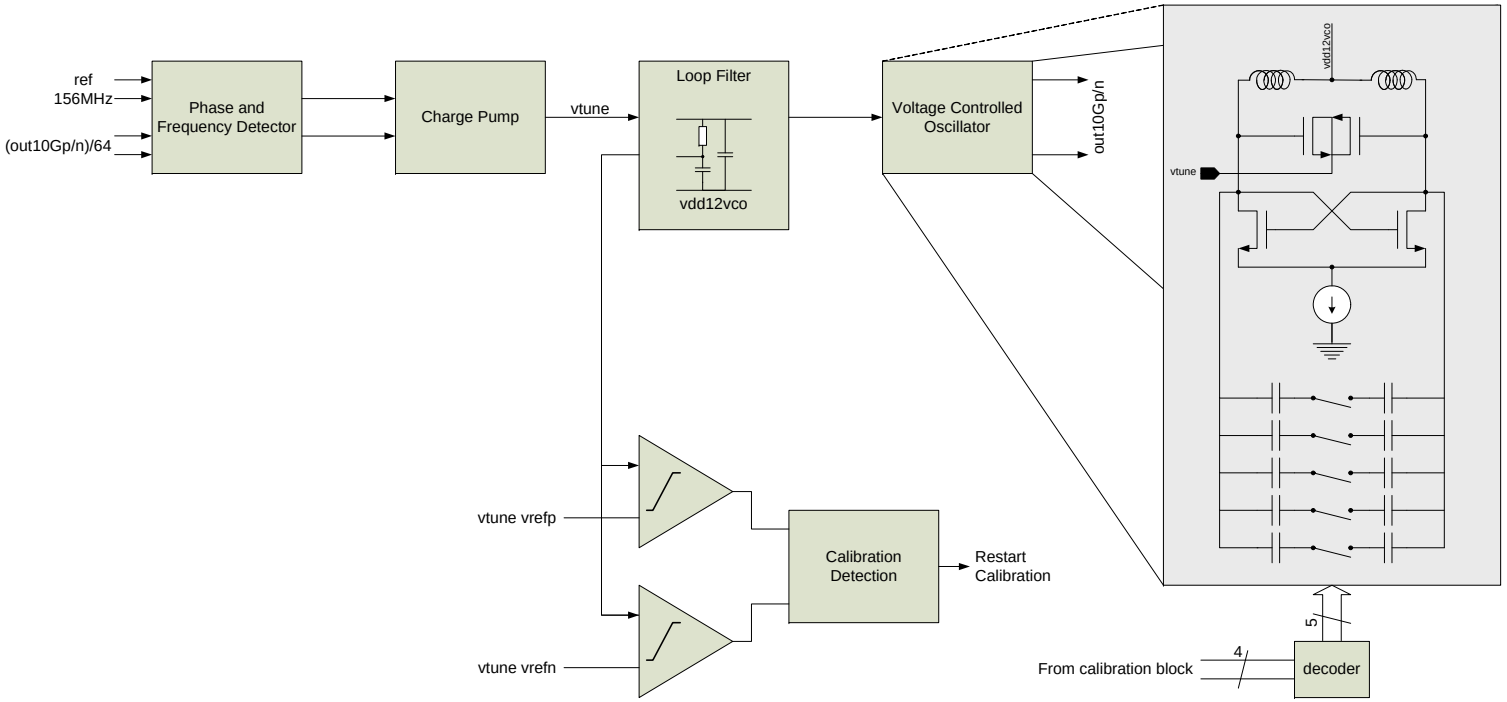
OD=103 um

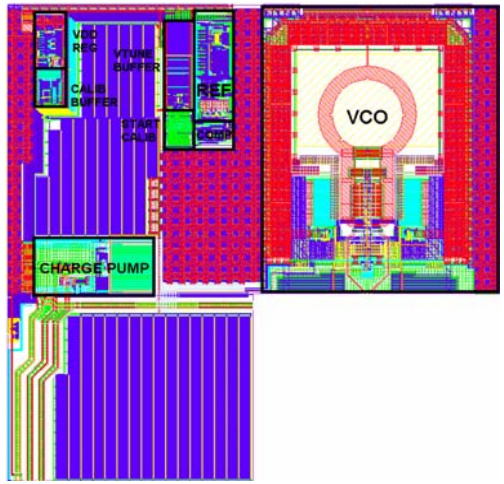
N=3

M7, M6 stacked only

Each square is 20 vias

Smarter way: don't forget to calibrate..





Real design- in lecture-go to attach pdf.

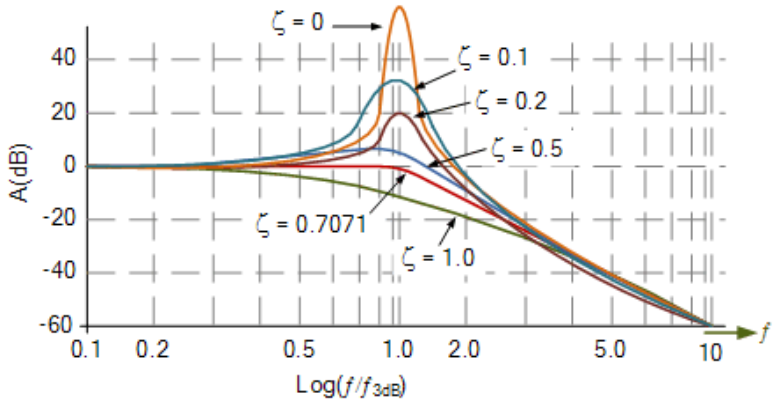
2nd-Order BSF – General-Form Frequency Response

- General form, in terms of ω_0 and Q:

$$H(\omega) = \frac{(j\omega)^2 + \omega_0^2}{(j\omega)^2 + \frac{\omega_0}{Q} j\omega + \omega_0^2}$$

: PLL

Second Order Filter Amplitude Response



Damping Ratio - ζ

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- We've been using ***quality factor*** to describe second-order filter response
  - A measure of the sharpness of the resonance
  - For band pass/stop filters, Q tells us about ***bandwidth***
  - For low/high pass filters, Q tells us about ***peaking***
- Another way to describe the same characteristic: ***damping ratio***, ζ
  - Damping ratio is inversely proportional to Q:

$$\zeta = \frac{1}{2Q}$$

  - A measure of the amount of ***damping*** in a circuit/system
  - Higher ζ implies a less resonant system
    - Less peaking
    - Wider bandwidth for band pass/stop filters

K. Webb ENGR 202

Below, one can observ that the phase does comes up once the loop gain crosses the 0dB line.

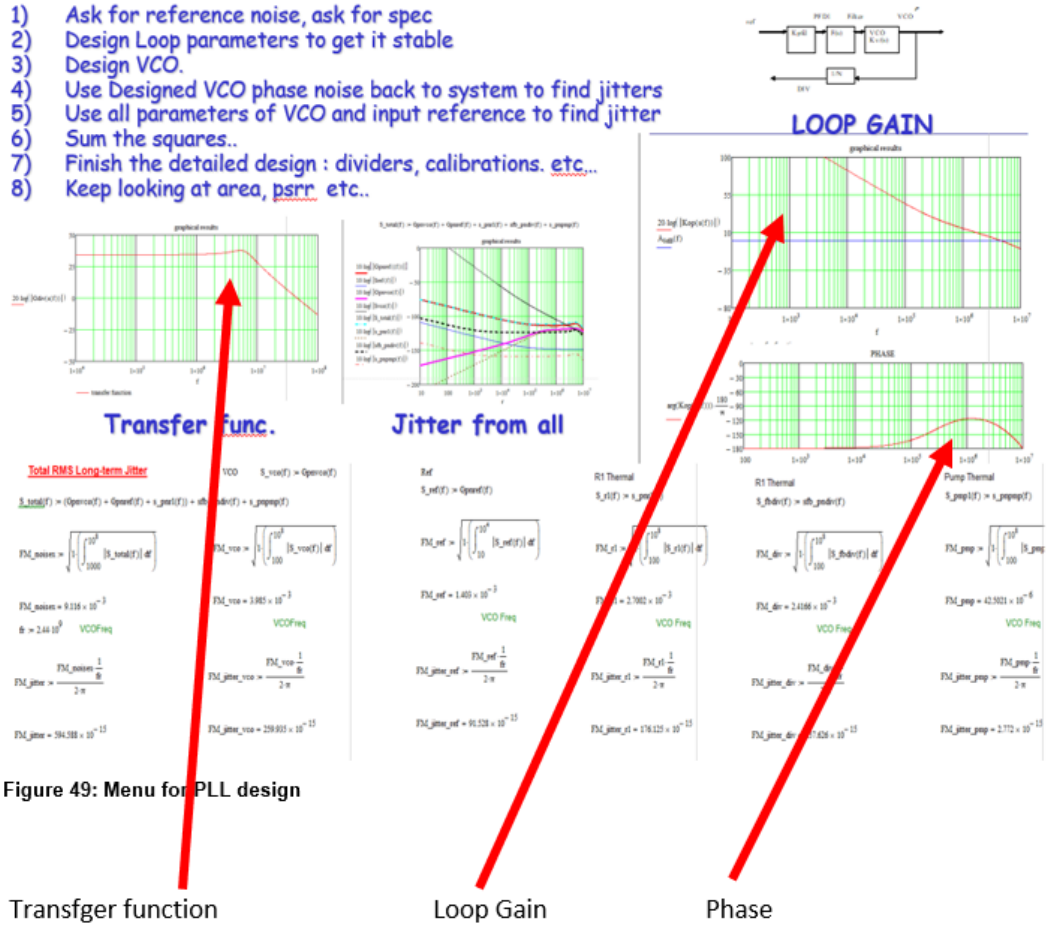
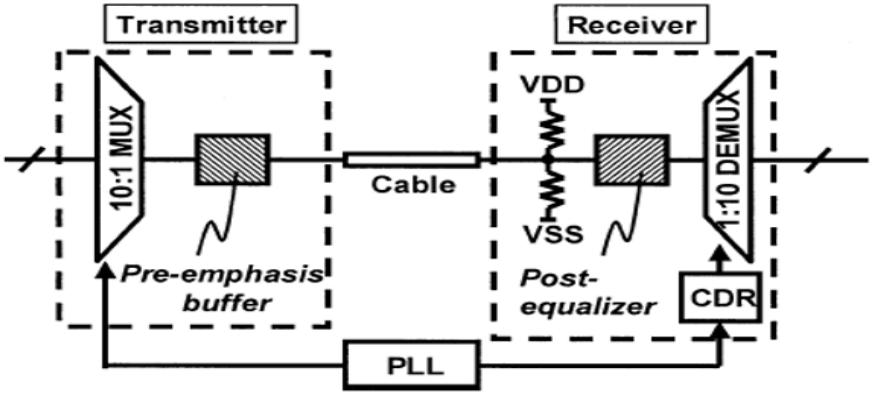


Figure 49: Menu for PLL design

CDR- clock and data recovery.

CDR- used in SerDes Rx.-data center/chip2chip



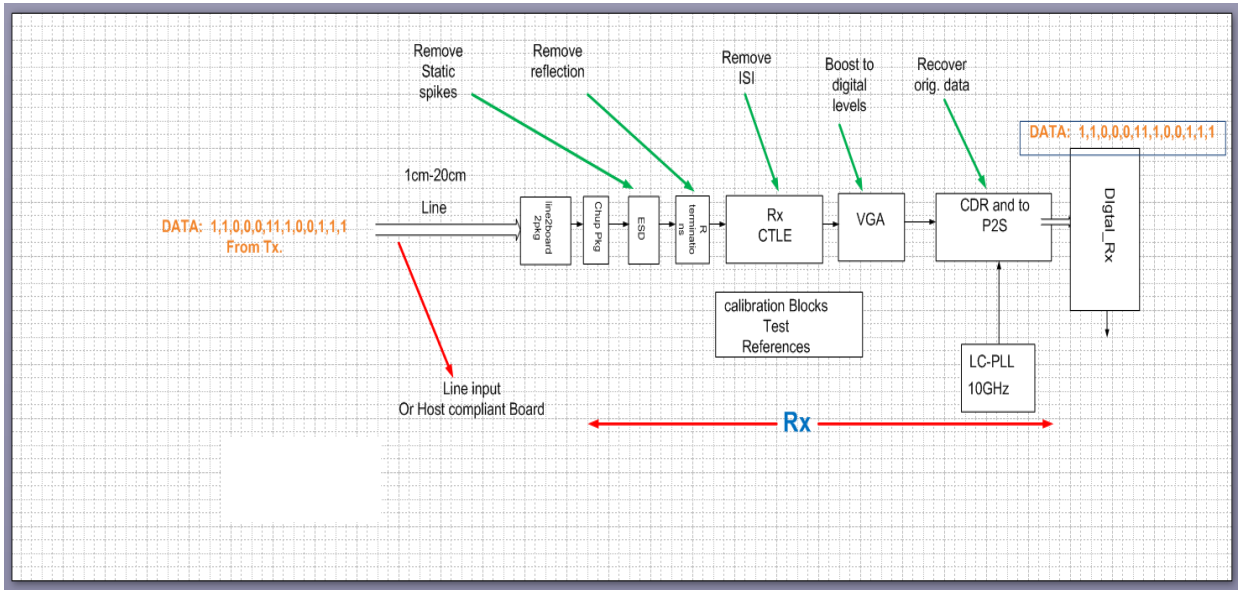
CDR

SPEC

- Jitter Tolerance- one over the jitter transfer…
- Jitter Transfer -- It's a filter, cut off point
- Jitter Generation- How good can you make the FF, VCO, Slicers

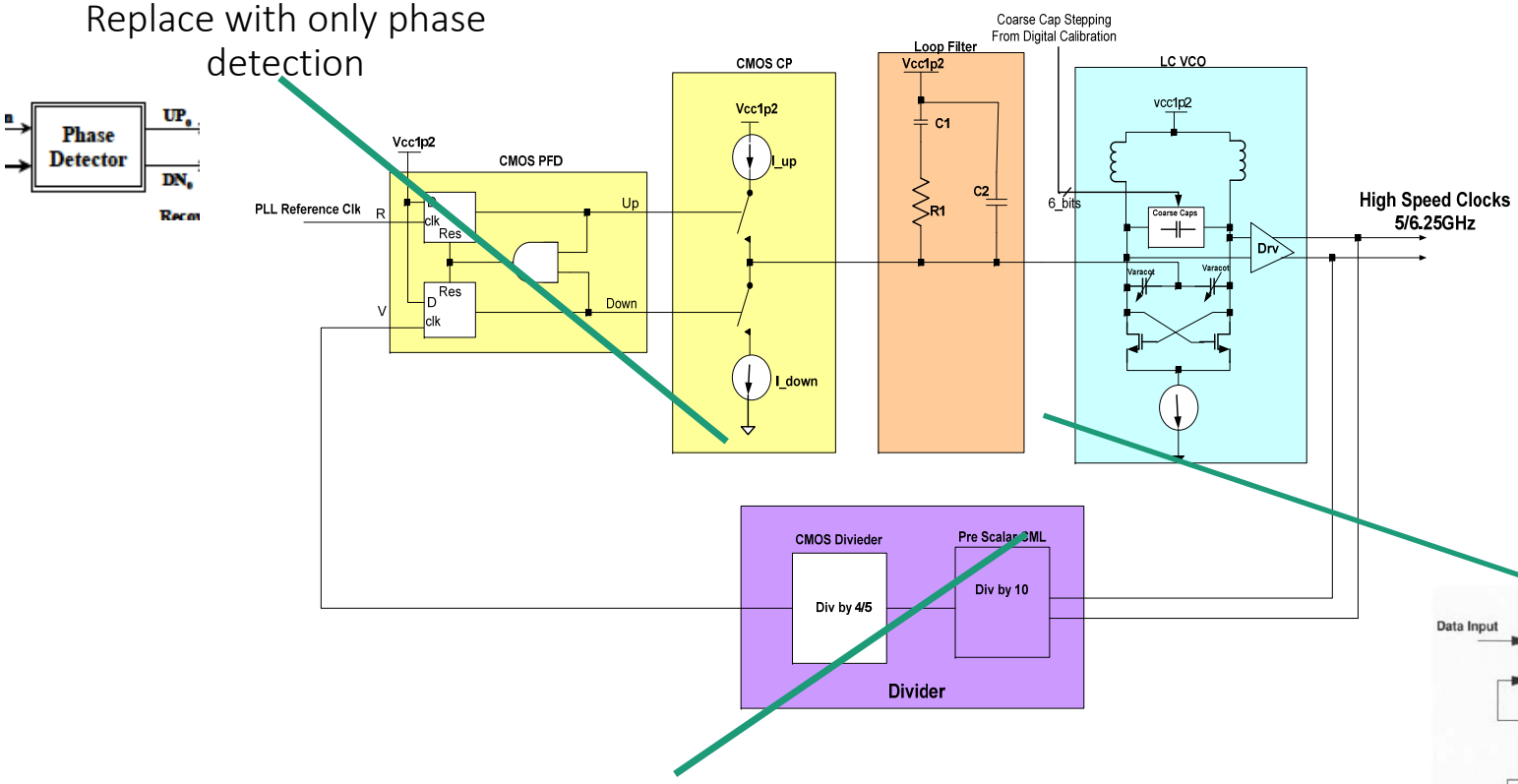
But it won't work without those: Added circuit design specs..

- CDR: lost frequency: ppm differences before it fails
- CDR: calibration if LC OSC is used.
- CDR: sensitivity to VCC ?



CDR- clock and data recovery-similarity to PLL.

Replace with only phase detection



Add FF clock the data
Create synced clock

Make the loop 1

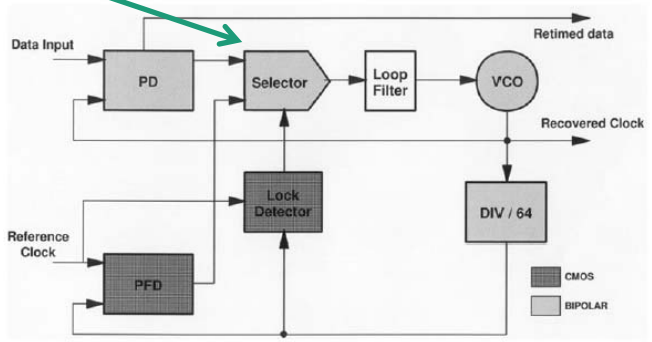


Fig. 1. CDR block diagram.

CDR- key choice PD- **no one** know how to choose…

CDR based on Bang-Bang PD
CDR based on Qureshi PD.

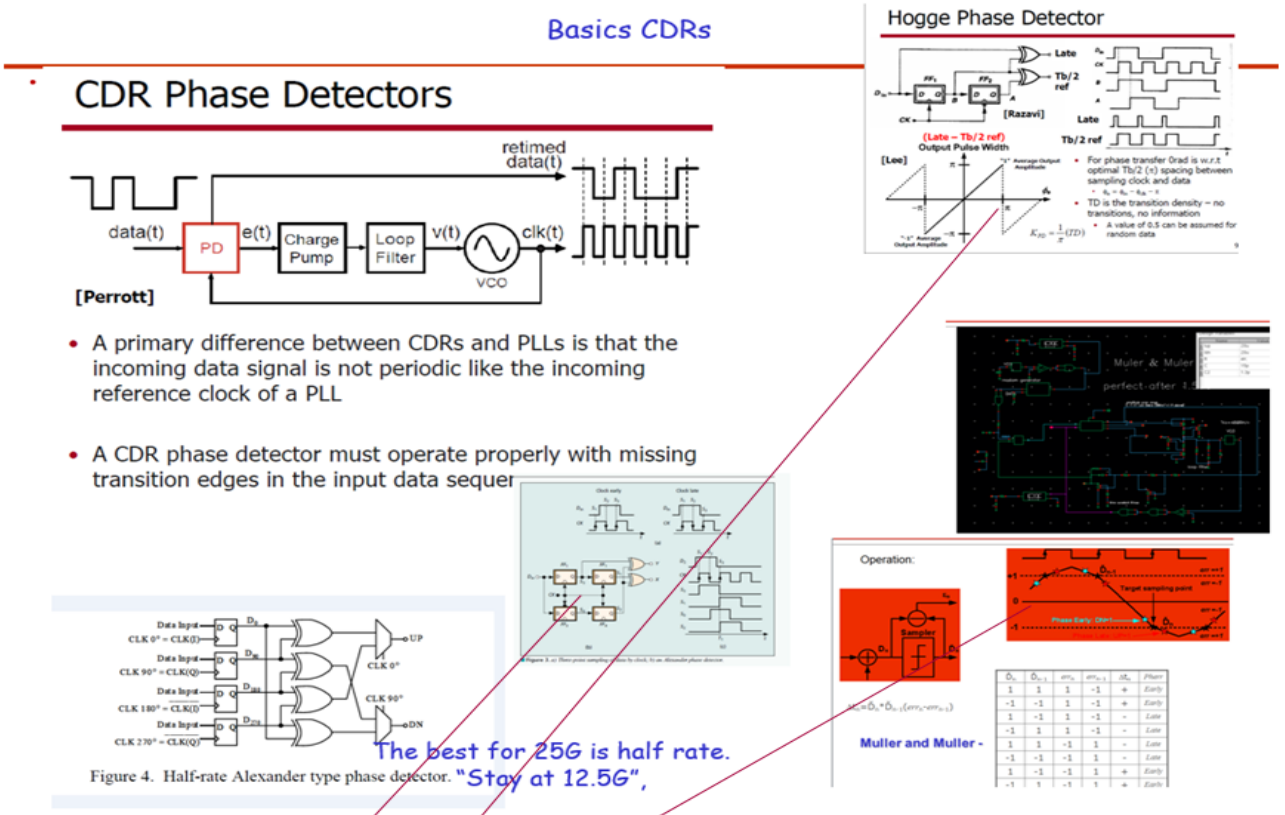


Figure 22: CDR types, Alexander, Hogg, and Qureshi (like: Muller-Muller).

PD-alexander

late information:

- If $S_1 \oplus S_2$ is high and $S_2 \oplus S_3$ is low, the clock is late.
- If $S_1 \oplus S_2$ is low and $S_2 \oplus S_3$ is high, the clock is early.
- If $S_1 \oplus S_2 = S_2 \oplus S_3$, no data transition is present.

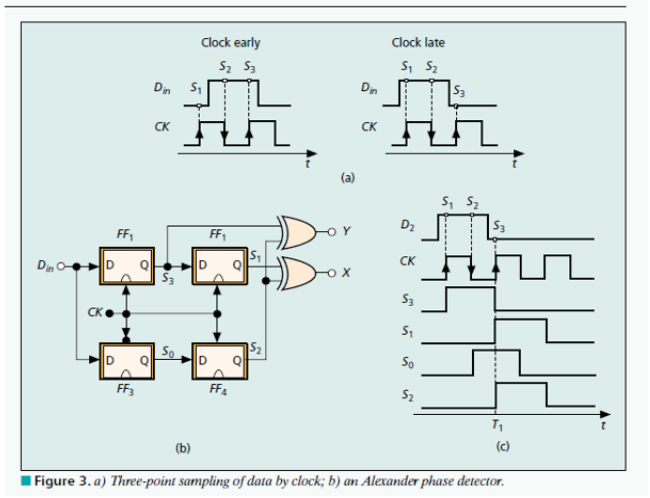
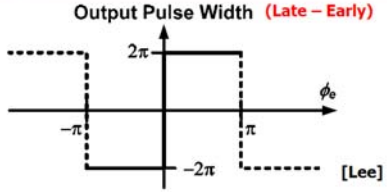


Figure 3. *a) Three-point sampling of data by clock; b) an Alexander phase detector.*

Razavi

Alexander Phase Detector Characteristic (No Noise)



- Phase detector only outputs phase error sign information in the form of a late OR early pulse whose width doesn't vary
- Phase detector gain is ideally infinite at zero phase error
  - Finite gain will be present with noise, clock jitter, sampler metastability, ISI

1

Alexander (2x-Oversampled) Phase Detector

- Most commonly used CDR phase detector
- Non-linear (Binary) "Bang-Bang" PD
  - Only provides sign information of phase error (not magnitude)
- Phase detector uses 2 data samples and one "edge" sample
- Data transition necessary

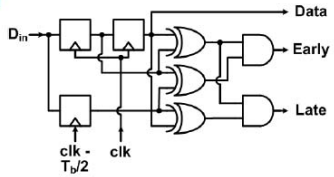
$$D_n \oplus D_{n+1}$$

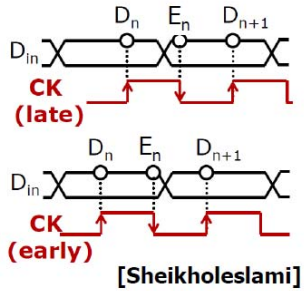
  - If "edge" sample is same as second bit (or different from first), then the clock is sampling "late"

$$E_n \oplus D_n$$

  - If "edge" sample is same as first bit (or different from second), then the clock is sampling "early"

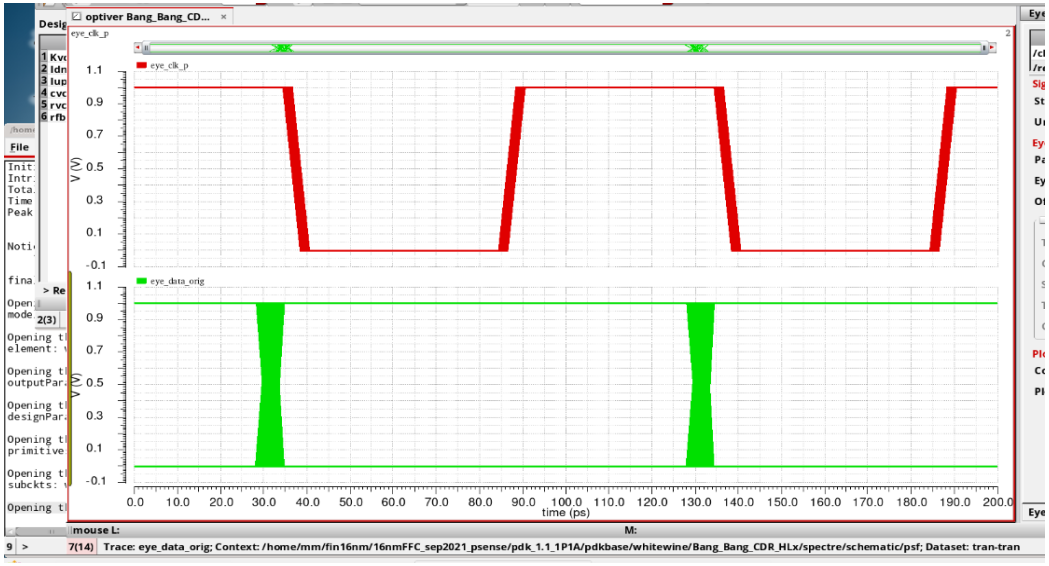
$$E_n \oplus D_{n+1}$$





10

CDR- once it works. The clock sits in the middle of the data



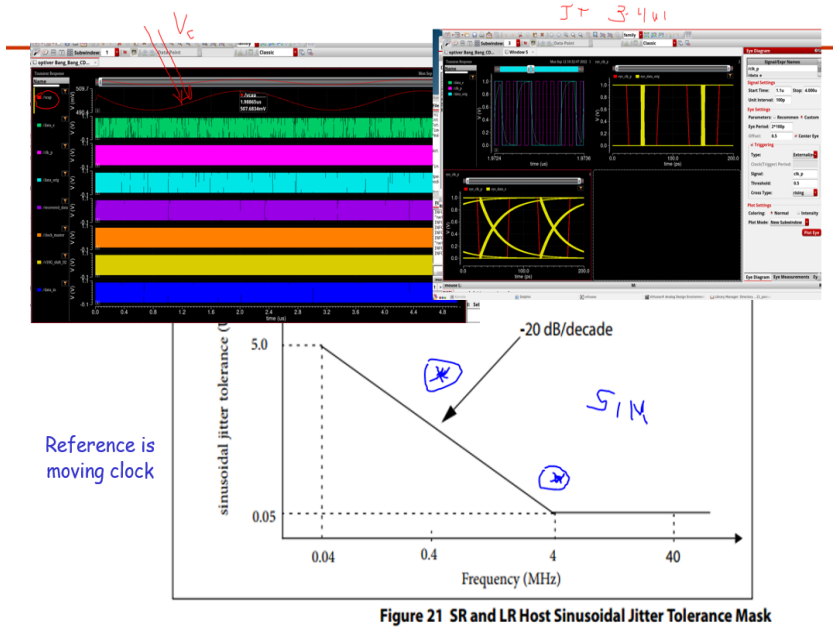


Figure 21 SR and LR Host Sinusoidal Jitter Tolerance Mask

END Lect. 09