Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 8

Sample (Track) and Hold

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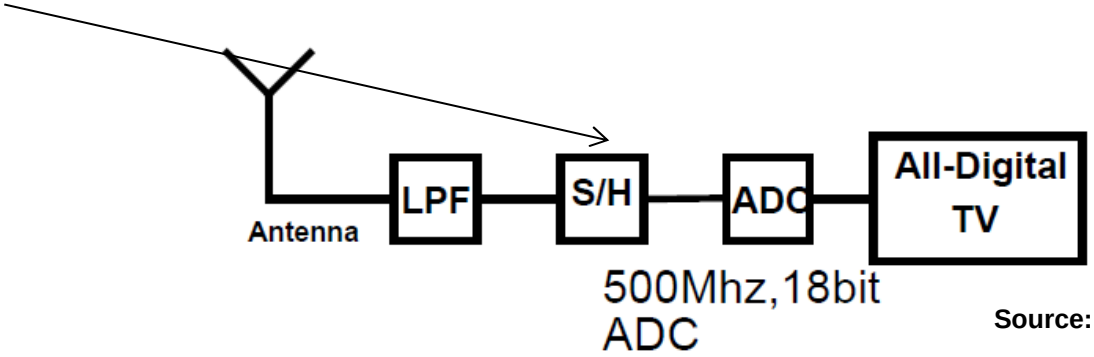
Agenda

Part I : SAMPLE AND HOLD Basics

Part II : Errors & Circuit Technique

Some ADCs can't do without it



Source: P. Grey

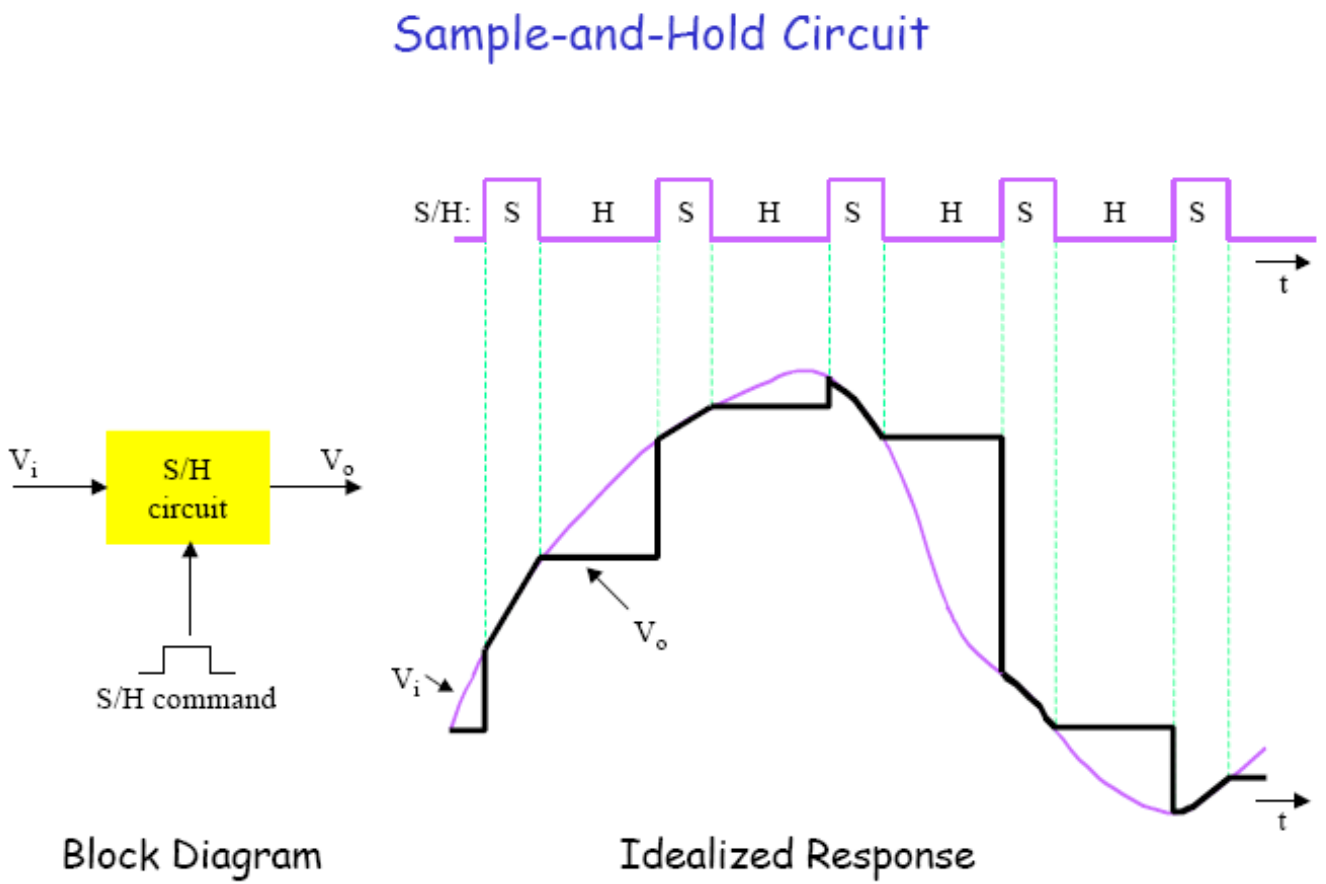
But
In high speed/accuracy it's the limiting elements in ADCs

It's the source of KT/C Noise Offset, Gain and Harmonics

It's one more source effected by clock jitter input

It's the source of Power consumption (maybe the highest)

Ideal

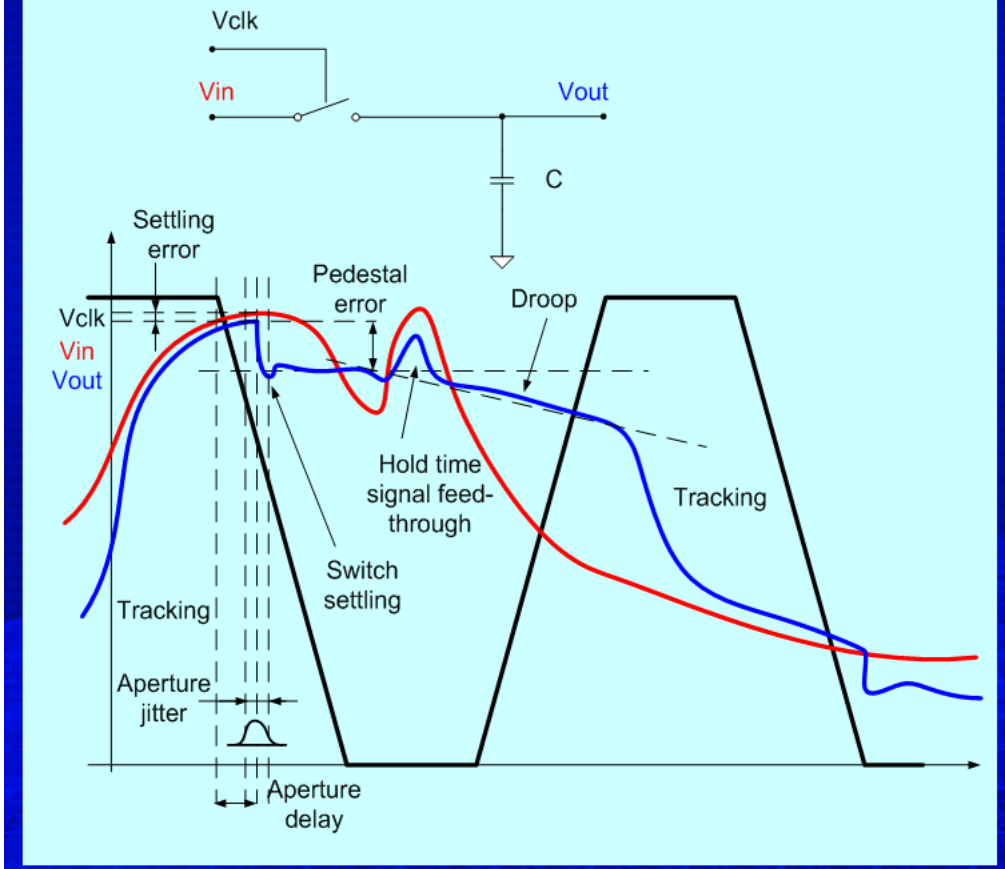


Source: TAMU

SAMPLING:

The Sample and hold keeps the analog value fixed for a clock duration.

S/H – Non Ideal



Practical track and hold circuits come with a plethora of impairments:

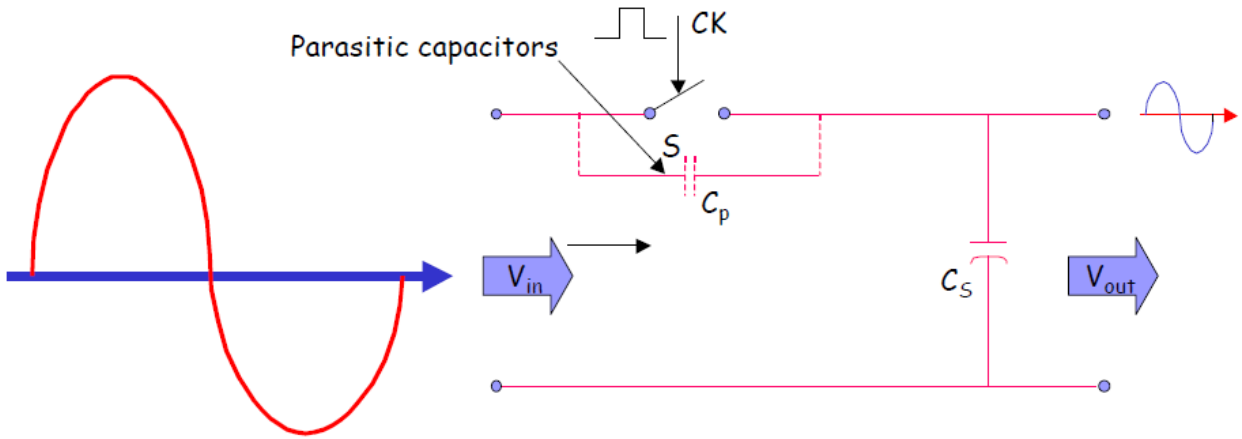
- settling/tracking error:
  - low pass characteristic
- switch settling
- pedestal error:
  - charge injection
  - clock feed-through
- signal feed-through:
  - parasitic capacitances
- droop
  - leakage currents

Lecture on Track and Hold, Edgar Sánchez-Sinencio 2000, http://amesp02.tamu.edu/~sanchez/689-Track-Hold.PDF.

The sampling instance is determined by the device that turns off last.

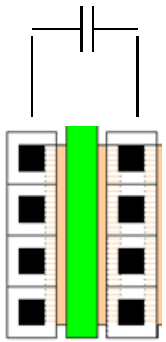
Off-Feed through: = (Cp/Cs+Cp) Vin

- Hold Mode Feedthrough: the percentage of the input signal that appears at the output during the hold mode.

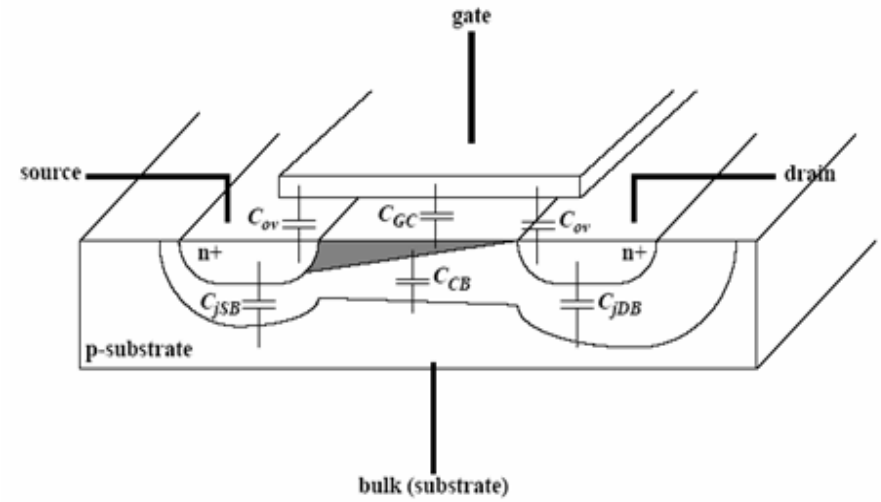


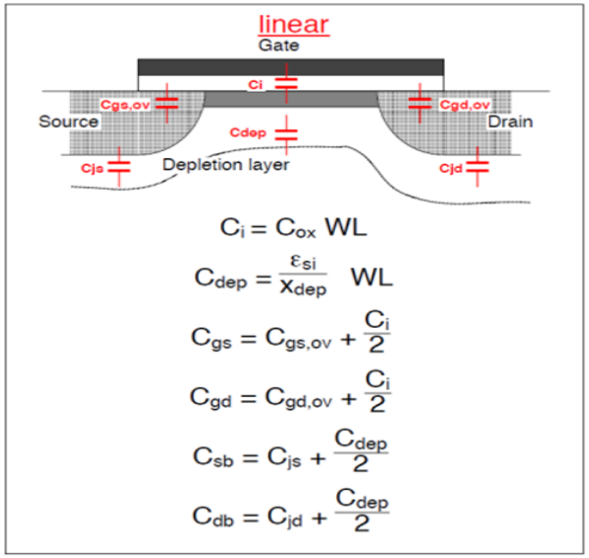
Source: TAMU

Key: Watch for routing metals over the switch transistor
L min and stack metal will add to Cp
Normally not a big issue….Cp is very small ~ 5-25e-15F



Summary lect. 1: The switch make up

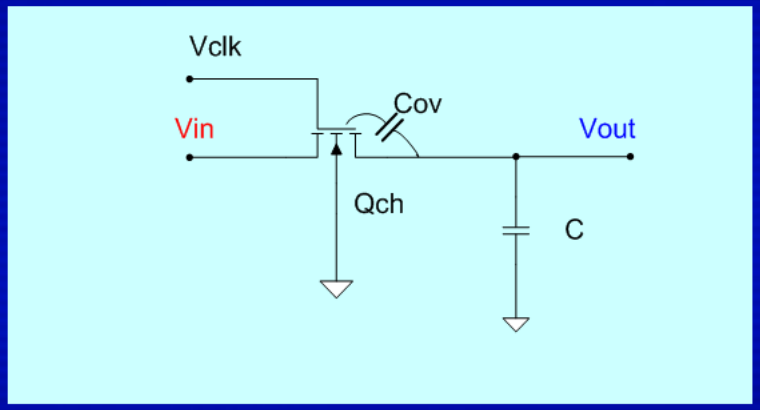




capacitors	Saturation	Linear	Off	
C gate to S	2/3Cox+Cov	1/2Cox+Cov	Cov	
C gate to D	Cov	1/2Cox+Cov	Cov	
C gate to B	0	0	Cox//Ccb+..	
C drain to B C source B	Cj(diode) CJ	Cj Cj	Cj CJ	Voltage dependance

Source: T.H. Lee.

Clock and charge error



Clock feed-through:

$$\Delta V_{feedthrough} \cong \Delta Vclk\frac{Cov}{C} \cong -vdd\frac{Cov}{C}$$

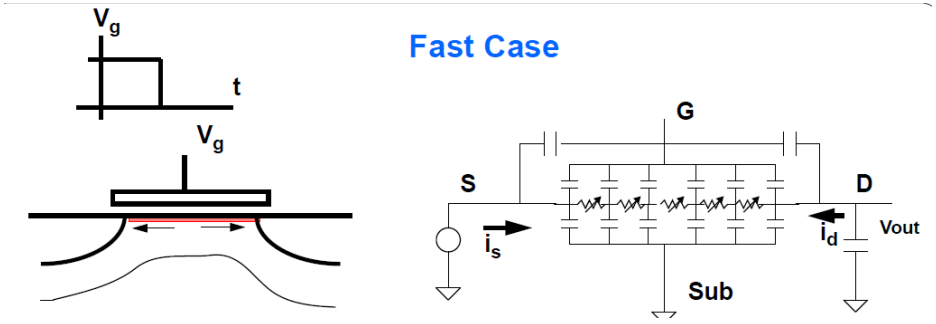
Charge Injection (very simple model)
(Half the channel charge goes to C):

$$\Delta V_{charge} \cong \frac{Qch}{2C} \cong -\frac{Cox \cdot W \cdot L(Vgs-Vth)}{2C} = -\frac{Cox \cdot W \cdot L(vdd-Vin(t)-Vth(Vin(t)))}{2C}$$

Offset-like

Total Error=sum of 2

$$\Delta V = -\frac{C_{ol}}{C_L}(V_H - V_L) - \frac{1}{2}\left(\frac{q_{channel}}{CL}\right)$$

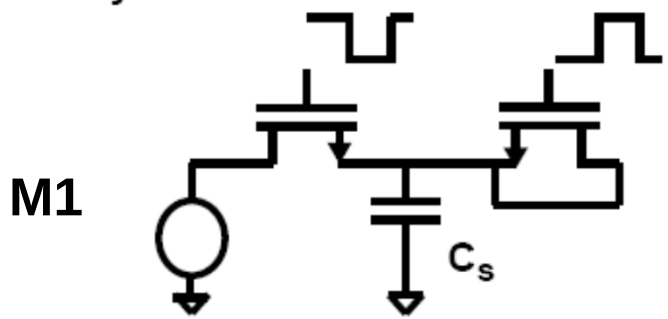


Gain-like

Source: P. Grey

“Circuit solutions” Clock feed through improvement

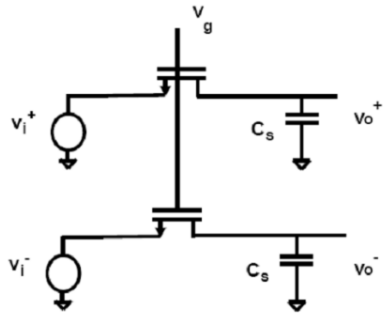
1. Dummy Switch



Problem: No way to balance over Clock fall time variations

if M1= W/L use M1=W/2L

4. Get rid of offset- Go Differential



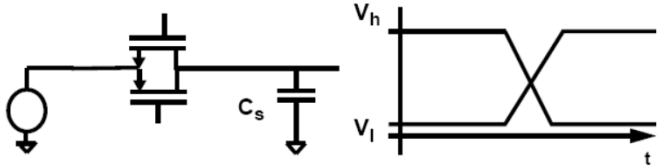
$$v_{o1} = v_{i1}(1+\varepsilon) + V_{os1}$$

$$v_{o2} = v_{i2}(1+\varepsilon) + V_{os2}$$

$$\Delta v_o = \Delta v_i(1+\varepsilon)$$

Source: P. Grey

3. Complementary NMOS, PMOS



Assume fast case

$$\frac{1}{2}q_{CN} = \frac{1}{2}(V_H - |V_{TN}| - V_i)W_N L_N C_{oxN}$$

$$\frac{1}{2}q_{CP} = \frac{1}{2}(V_i - |V_{TP}| - V_L)W_P L_P C_{oxP}$$

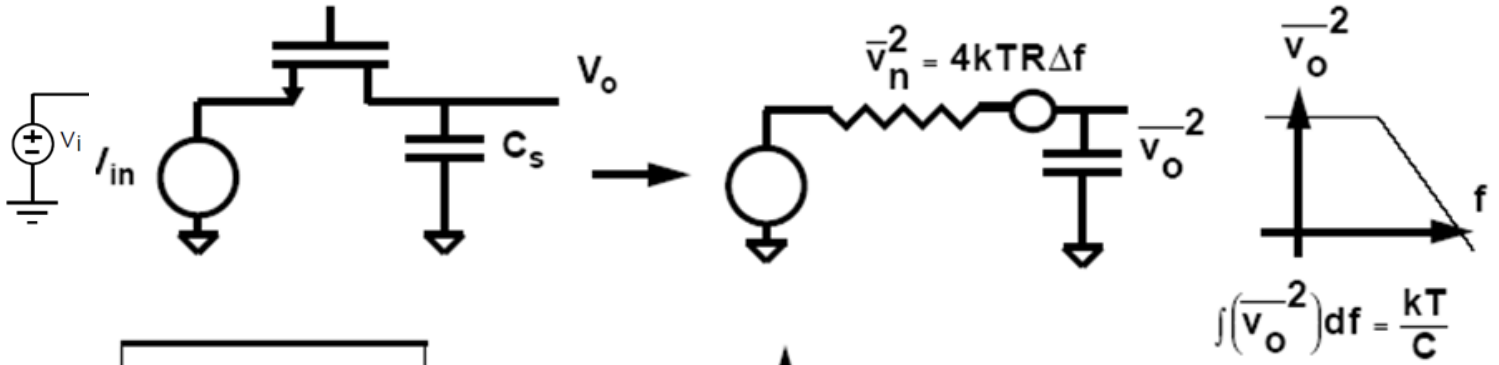
$$\Delta V = -Vin(1+\varepsilon) + V_{os} \text{ where:}$$

$$\varepsilon = \left(\frac{W_P L_P C_{oxP} + W_N L_N C_{oxN}}{C_L}\right) \qquad V_{os} = (V_{OSN} - V_{OSP})\frac{C_{ol}}{C_L}$$

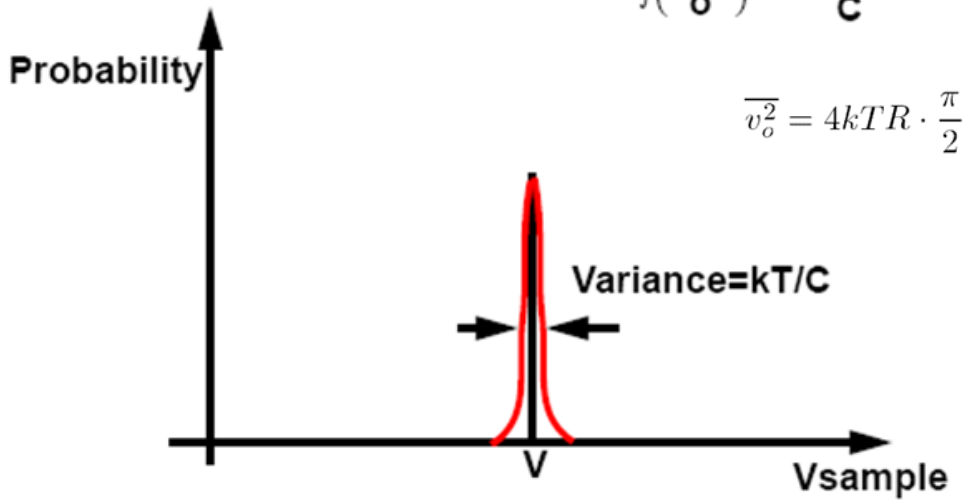
Key Point:
1. Offsets Partially Cancel
2. Gain errors ADD!!

Noise: Model

kT/C Noise Limitation



C	$\sqrt{\frac{kT}{C}}$
100pF	6.4uV
10pF	21uV
1pF	64uV
100fF	210uV
10fF	0.64mV

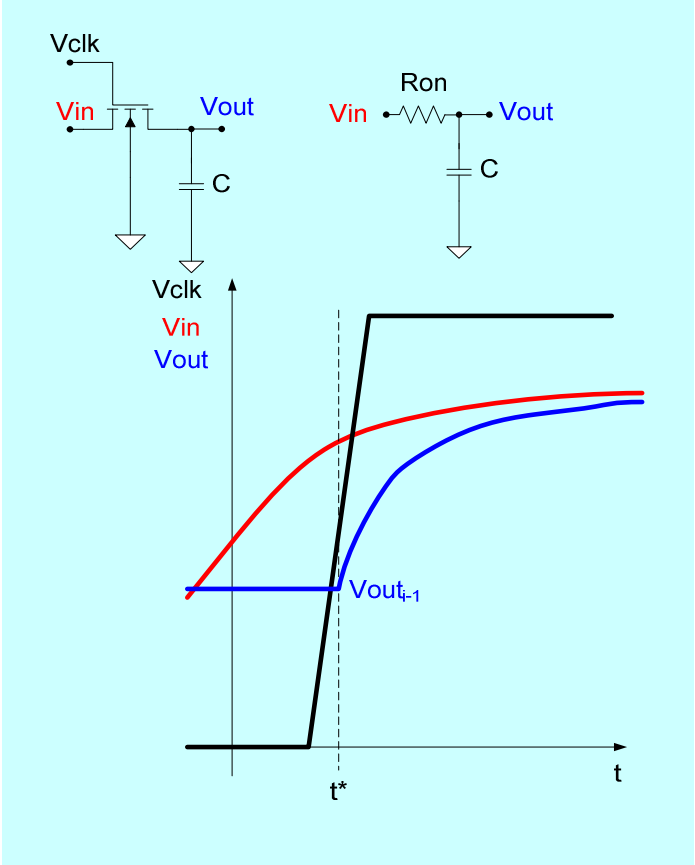


$$\overline{v_o^2} = 4kTR \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{kT}{C}$$

ADC-In class derivation: KT/C<LSB*LSB/12

$$C > 2^{2b}\left(\frac{kT}{\hat{V}^2}\right)$$

Settling



Aquisition

Acquisition: for a step input response is

Vout = (Vold-Vnew) (1-exp(-1/RsCh))

I max is at t=0 ant it is Vmax=Vin-V Ch

Imax = Vmax/Rs

Time needed

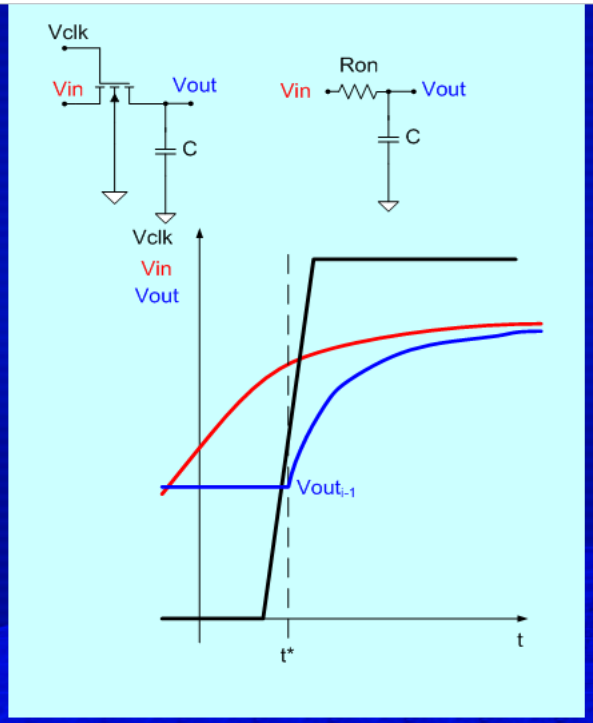
1% = 4.6 RsCh
0.1% = 6.9 RsCh = 10bit
0.01% = 9.2 RsCh

If the input is **current limited** them the output is slweing at a rate of

dVout / dt = Iin/Ch

in reality the input is moving, BW limited, and it is not a step input- see next slide

Settling time error input is changing



Tracking/settling error calculation:

$$Vin(t) = Vcm + A\sin(2\pi f_{in} t)$$

$$Vin(t) = Vout(t) + Ron \cdot C\frac{\partial Vout}{\partial t}$$

$$t = t^* \Rightarrow Vout = Vout_{i-1} \cong Vin\left(t^* - \frac{1}{2\,fsmp}\right)$$

Forced solution:

$$Vout^f(t) = Vcm + \frac{A\sin\left[2\pi f_{in} t - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}}$$

Homogenous solution:

$$Vout^h(t) = B \cdot e^{-\frac{t-t^*}{R_{on}C}}$$

Solution:

$$Vout(t) = Vout^h(t) + Vout^f(t)$$

Set initial condition (determine B):

$$B = Vout_{i-1} - Vcm - \frac{A\sin\left[2\pi f_{in} t^* - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}} \cong$$

$$\cong \frac{A\sin\left[2\pi f_{in}\left(t^* - \frac{1}{2f_{smp}}\right) - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}} - \frac{A\sin\left[2\pi f_{in} t^* - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}}$$

$$= \frac{-2A}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}} \cos\left[2\pi f_{in}\left(t^* - \frac{1}{4f_{smp}}\right) - \arctan(2\pi f_{in} R_{on} C)\right] \sin\left(\frac{\pi f_{in}}{2f_{smp}}\right)$$

$$R_{on} = \frac{L}{W \cdot K(Vgs - Vth)} = \frac{L}{W \cdot K(Vdd - Vin - Vth(Vin))}$$

(no body effect)

Basic fast S/H (Open loop)

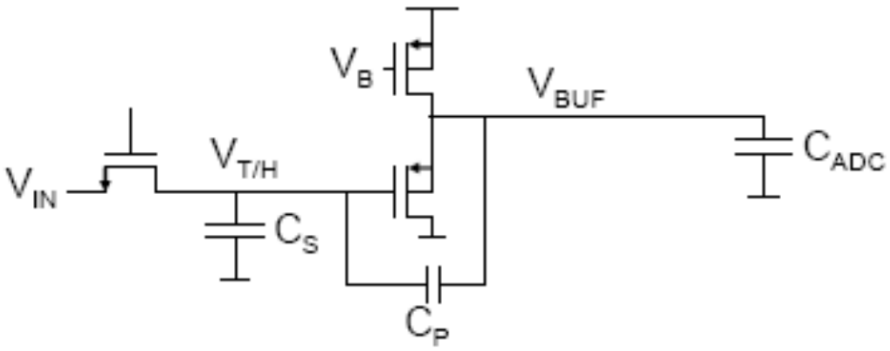


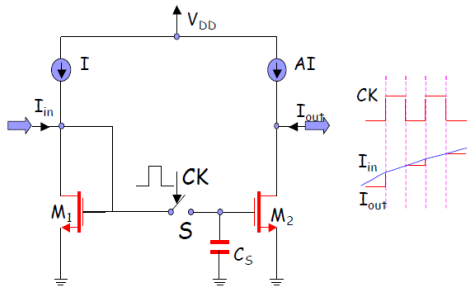
Figure 6: Buffer directly connected to ADC, omitting the resistor.

Use differential structure..

T&H Circuit: Current-Mode

Current-Mode Architecture:

Advantages: high-speed (over 100MHz) and low voltage (<1.2).
The speed depends on the time constant given by:



$$\tau = \frac{C_S}{g_{m1}}$$

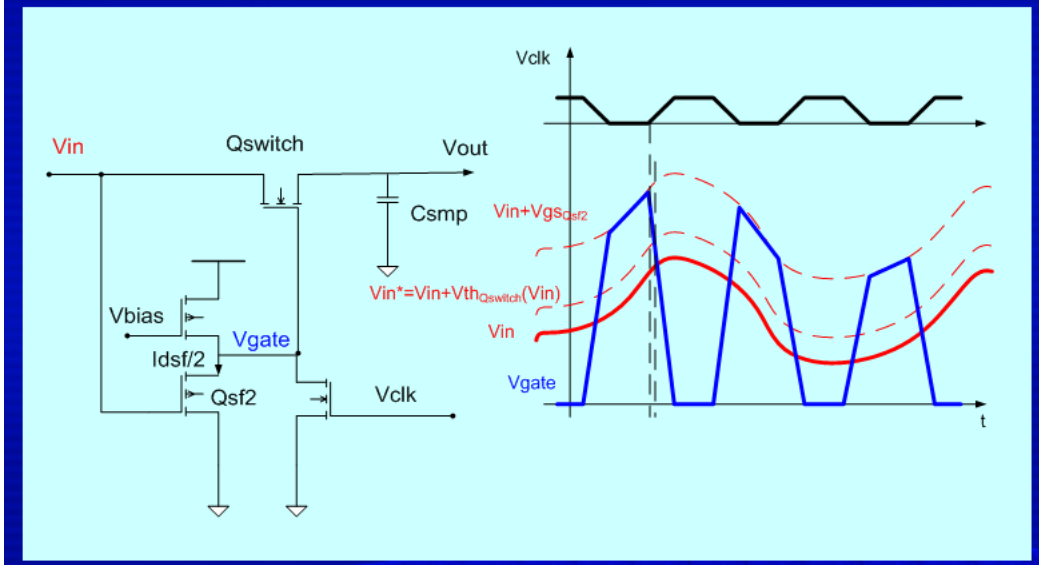
$$C_S = \frac{2}{3} C_{ox}(1+A) W_1 \bullet L_1$$

$$g_{m1} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{Tn})$$

Source: TAMU

Boost the gate: Linearization design

Linearized MOS Track and Hold

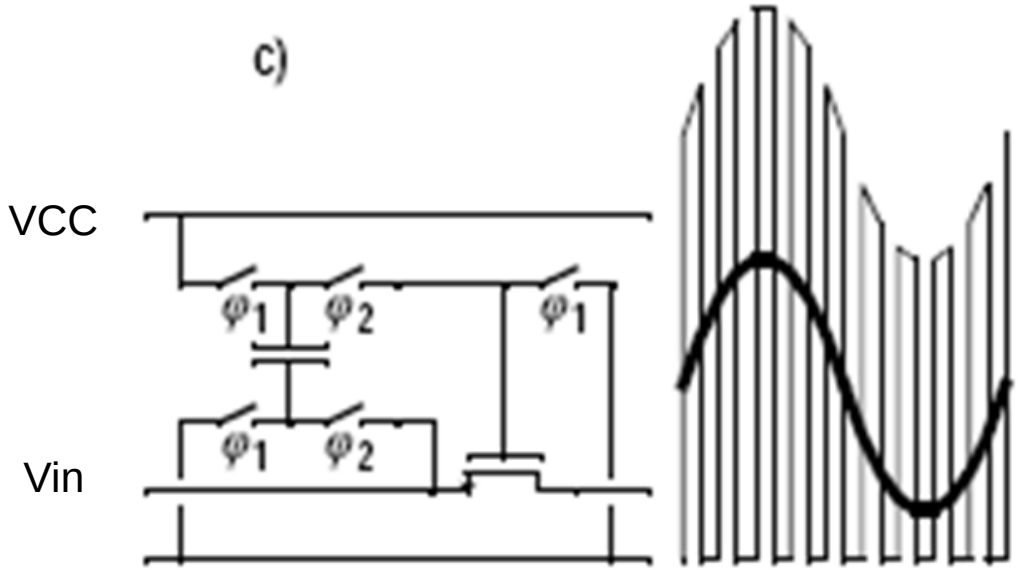


Compared to simple Track and Hold:

- less signal dependent sampling
- less non-linear charge injection
- signal dependent clock feed-through

For the pseudo-differential structure, performance can be somewhat worse than for the simple track and hold if there is not enough headroom.

Key: Qsf2 is P ch follower - on board operation..
Vcc of follower need higher voltage, speed of follower high, more Idd..



gnd=0v

(Abo and grey)

1) Short with 1 to vss and
2) Load Vcc and ground on C
3) Close 2 Load Vin were gnd was and
4) inject VCC+Vin on the gate

In class analysis

END Lect. 8

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