Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 7 part b. + 8

Comparator: Operation and Design

www.gigalogchip.com

Agenda

Comparator Basics

Architectures

Error Sources

Comparator Examples

Comparator Basics-Design Methods

Comparator: Non Sampled, Sampled

Error in Comparators

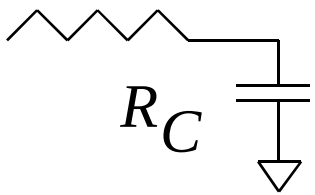
Basic Analysis

Architectures

Special topics – Calibrated and differential

Basic Feed back to boost BW

"SLOW"

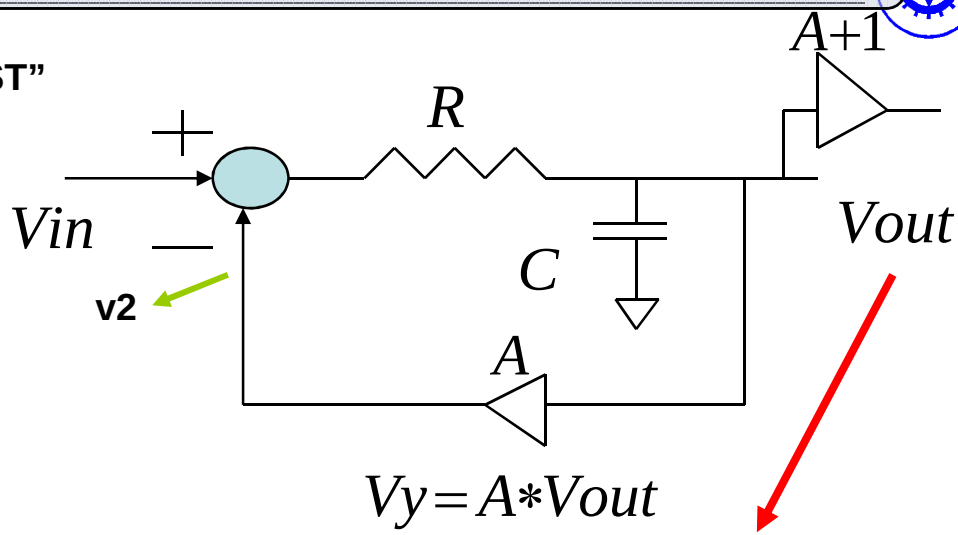


$$Vout(t) = Vin[1 - e^{-t/RC}]$$

$$\tau = R * C$$

DC gain=1

"FAST"



$$Vout(t) = Vin\ [1 - e^{-t(A+1)/RC}]$$

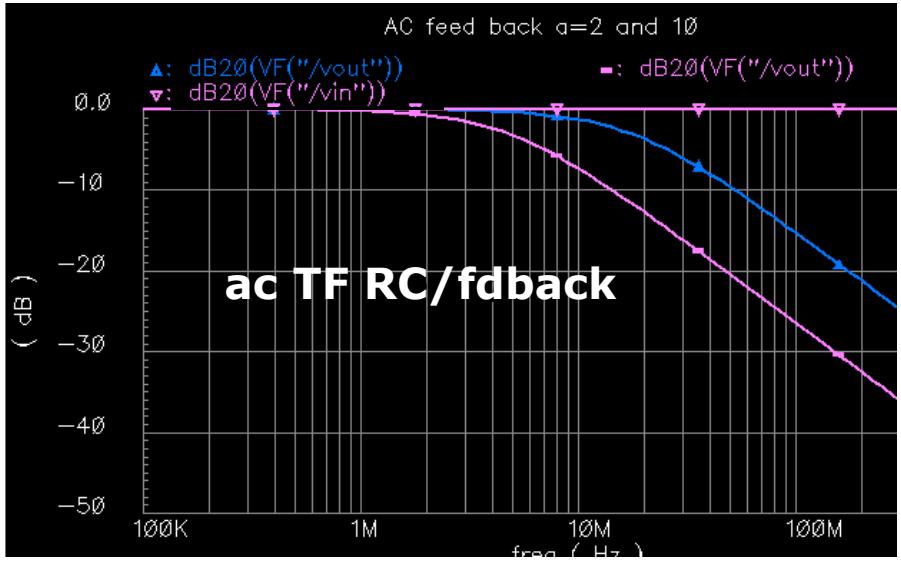
$$\tau(new) = R * C/(A+1)$$

DC gain=1/1+A

But at v2 DC

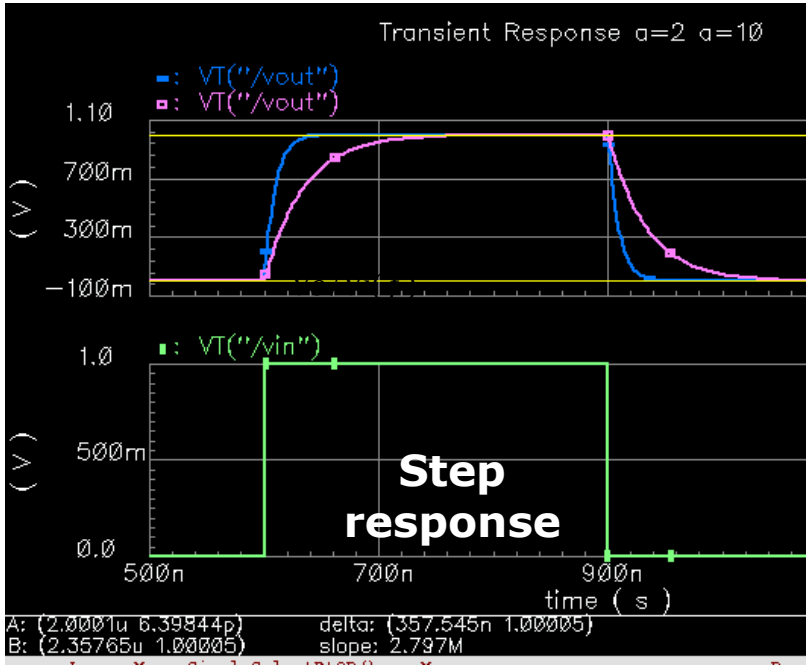
gain=A/1+A~1

Simulation: a=2 and a=10



Frequency

$$Vo/Vi(f)$$

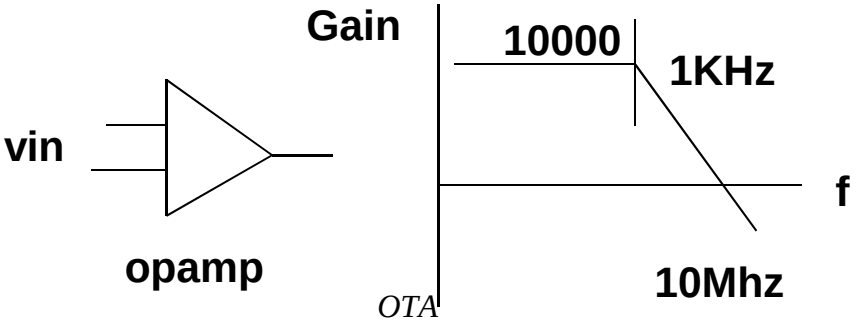


Time

Ac response

Time domain

Speed and feed back basics

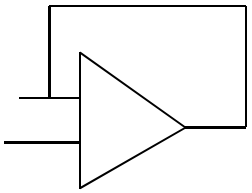


Speed

$\tau = 1ms$

Gain(dc)

80dB



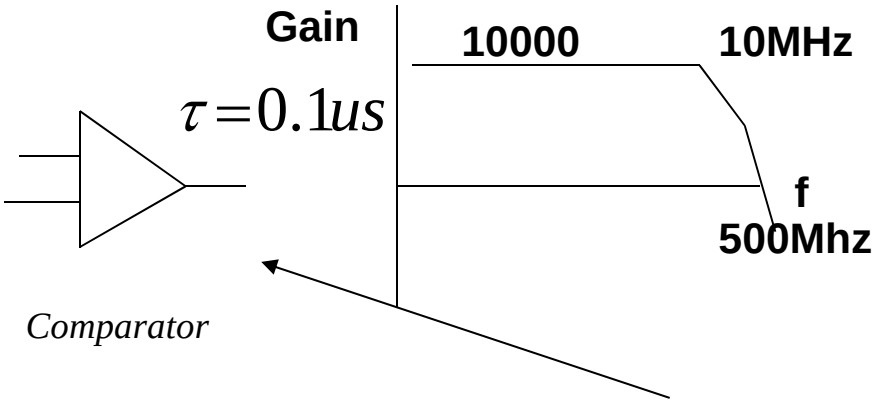
Gain=1

And accurate

$\tau = 0.1us$

0dB

Feed _back



$\tau \sim 0.1us$

80dB

Removed all compensation

Comparator Basics

A Comparator:

LINK FROM ANALOG TO DIGITAL – QUANTIZER

Definition: Compare 2 or more input and produce
a digital value high or low**-** **“**Its a 1 bit ADC !”

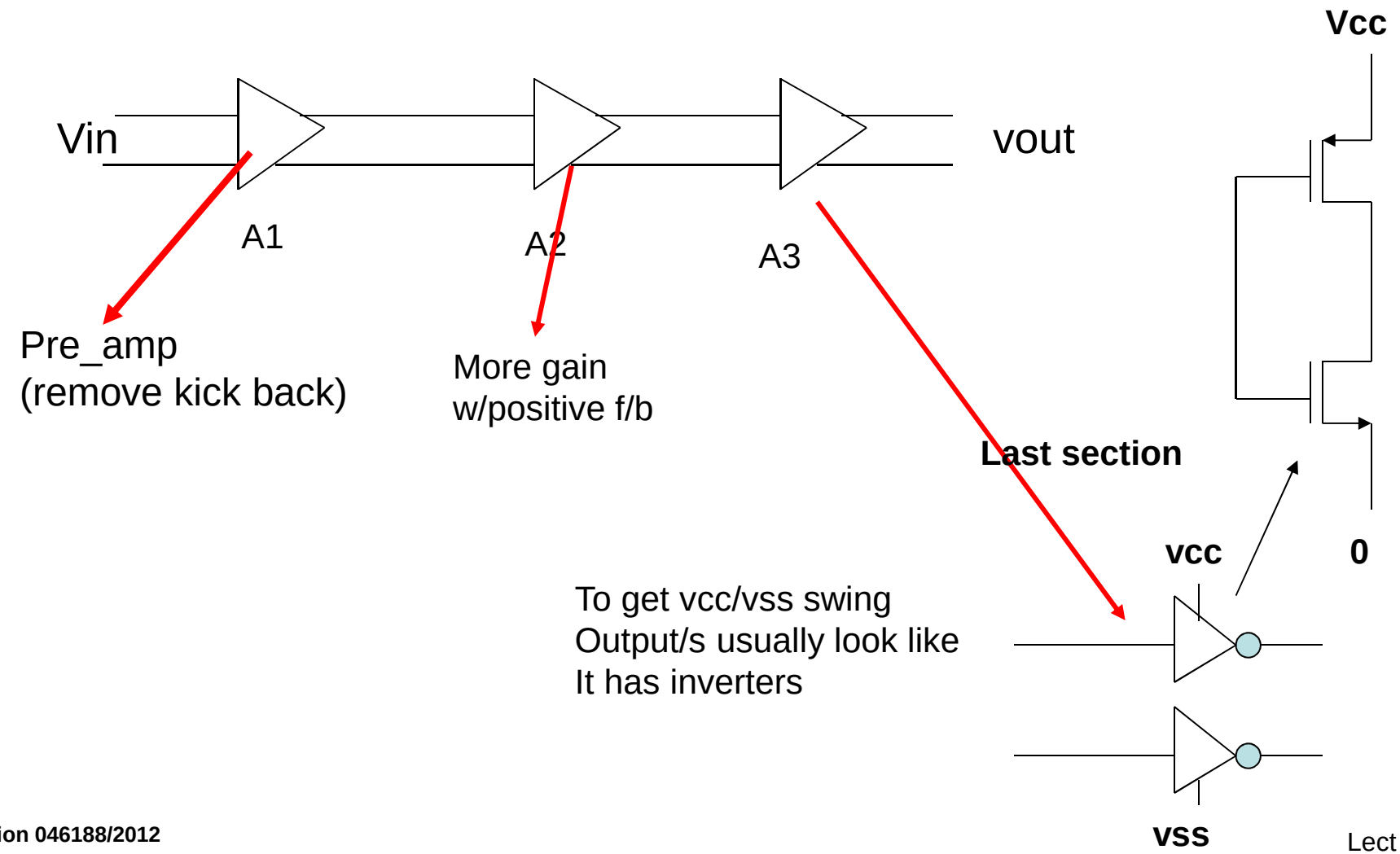
Structure:
A chain of gain stages (no feed back-unlike amplifier)

It is used in an “open Loop” configuration
to achieve fast digital response (opamps are slow and big)

Basic Architecture1 of comparators

Non Sampled: Continuous Time (CT)

Output is gain time input differences:
slow because internal nodes need to be recovered

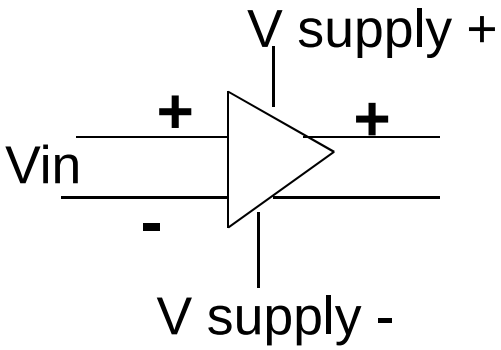


Mathematical Descriptions (low frequency)

For small Vin1-Vin2

Vout=A(vin1-Vin2)

A is the gain of the combine structure



For all Vin1-Vin2 Vout=clamp at either supply

Ideal

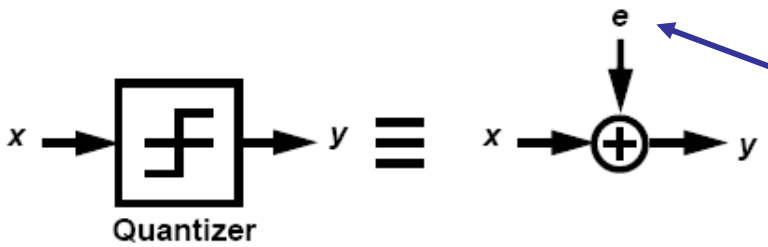
Vout=A(vin1-Vin2) results fall between supplies

(realistically its exponential)

Vout=Vdd if A(Vin1-Vin2) > Vdd-Vss

Vout = Vss is A(Vin1-Vin2) < Vdd-Vss

Mathematical Descriptions with noise.



Important model in
Sigma delta ADCs

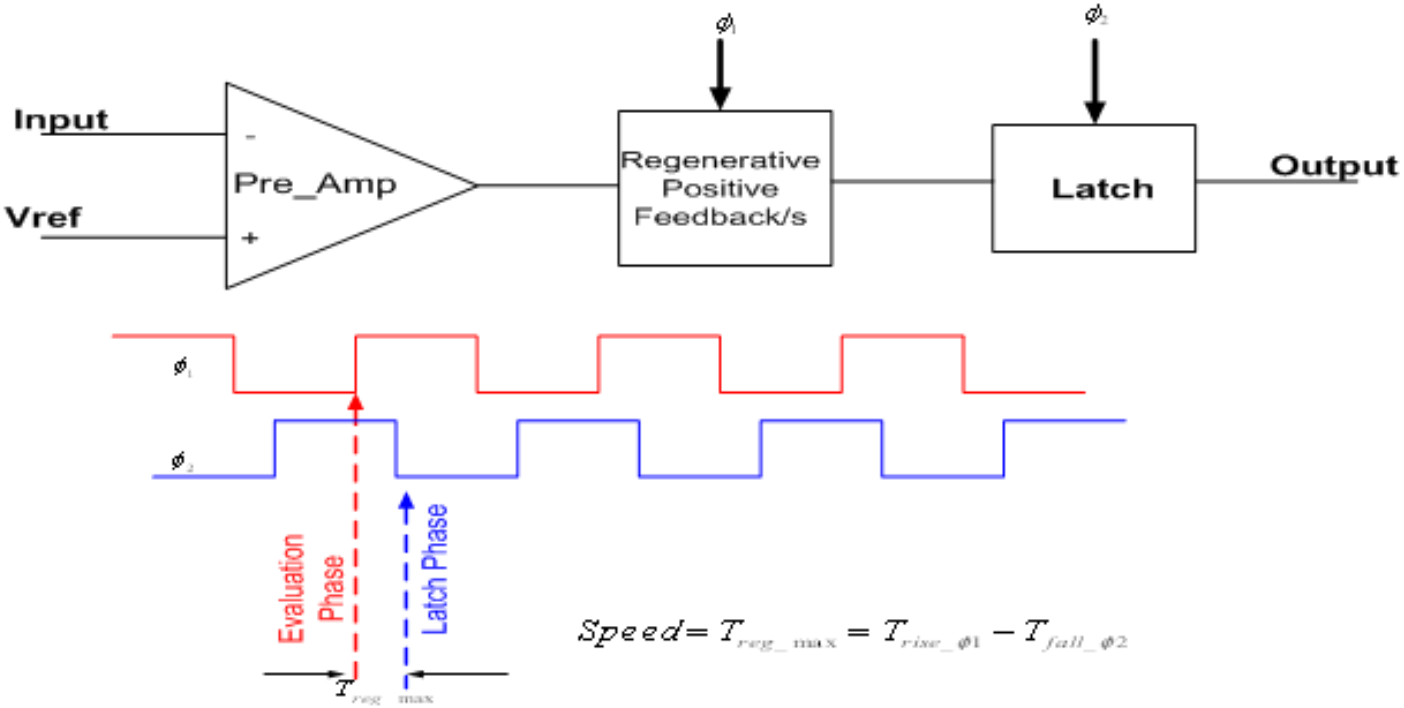
exact model if *e* is defined properly
ex. *y=sgn(x)*, then *e=y-x=sgn(x)-x*

becomes an approximation when we claim noise is independent

Basic Architecture 2 type-Latched

Sampled Comparator:
Much faster
clamp high gain stages
Need clock or digital signal

Concept:



Error in Comparators:

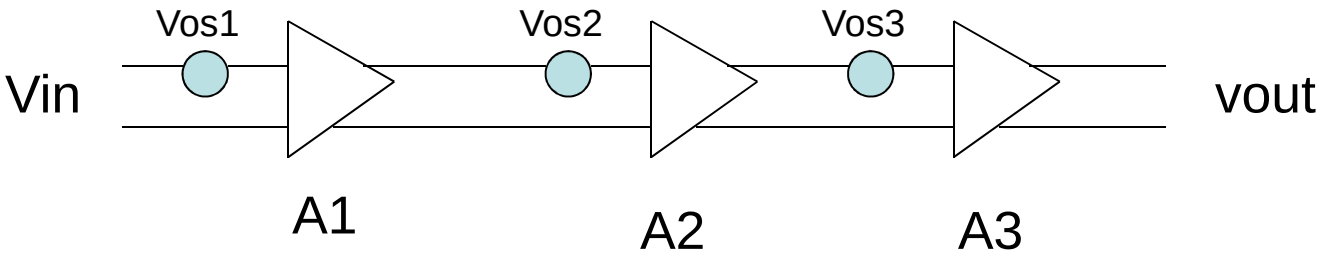
Gain
Offset
Meta State
Speed
Kick Back
Noises and supply noise

Main Parameters Definitions

- **Input Offset** – It is the voltage that must be applied to the input to obtain the crossing point between low and high logic level
- Vout = A x Vindiff , vss<Vout<Vdd A=1000 , time is also a factor
- **Sensitivity**- It is the minimum voltage or current that produces a consistent output signal within the expected comparison time- Meta state
- **Comparator response time** – It is minimum time interval required to achieve the proper logic output as a response to the minimum input step
- **Overdrive recovery time** – When the input signal is pretty large the gain stage saturates to the positive or negative rails quickly. If the input stage become small, the gain stage takes some time to react and generates the voltage required to produce the output voltage
- **Kick back input noise** – Caused in evaluation state due to transition response: Switching noise

Offset and gain basics in comparator

Vos(total)



$$Vos(total)^2 = \sqrt{\boldsymbol{Vos1^2} + \boldsymbol{Vos2^2}/A1^2 + \boldsymbol{Vos3^2}/A1^2 A2^2}$$

Key: Vos is a statistic parameter
Further stages (A2 and A3) have larger offset
Using minimum sizes..

Example: 8 bit ADC 1GS/s (through put=2ns)
for 8 bit with Vfs=0.5v , Vdd=1v at 1/10LSB =
A1 x A2 X A3 required ~ 5000 ➔ (1v/(0.5/255 x 10) in under 1ns

If
Vos1=2mv , vos2=10mv vos3=20mv
If we take : A1=10 A2=25 A3=20

$$Vos(total) = \sqrt{\boldsymbol{2^2} + \boldsymbol{10^2}/\boldsymbol{10^2} + \boldsymbol{20^2}/10^2 25^2 +}$$

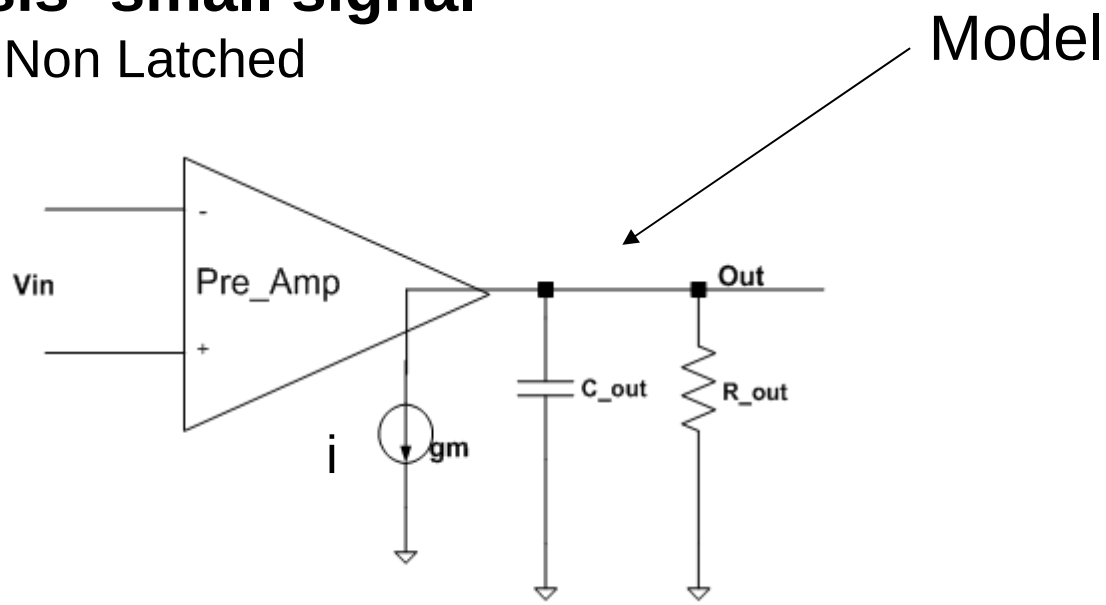
Vos(total)=2.23mV

Transistor as linear gain blocks

Gm Rout … diff stage..

Basic Analysis- small signal

Non Sampled – Non Latched

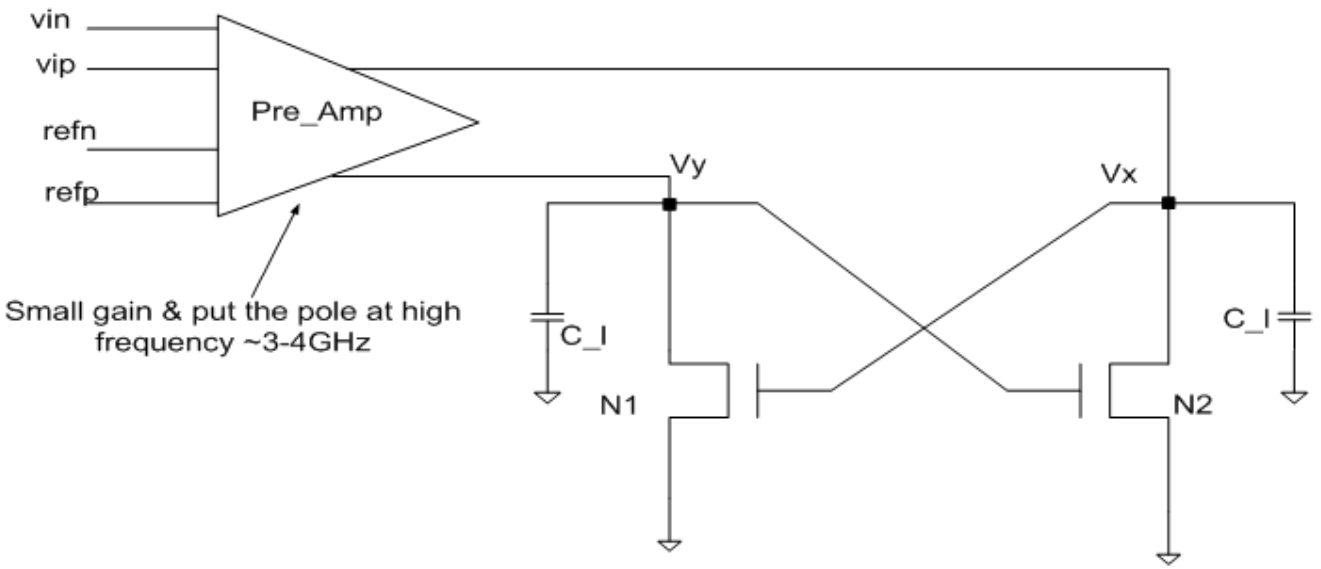


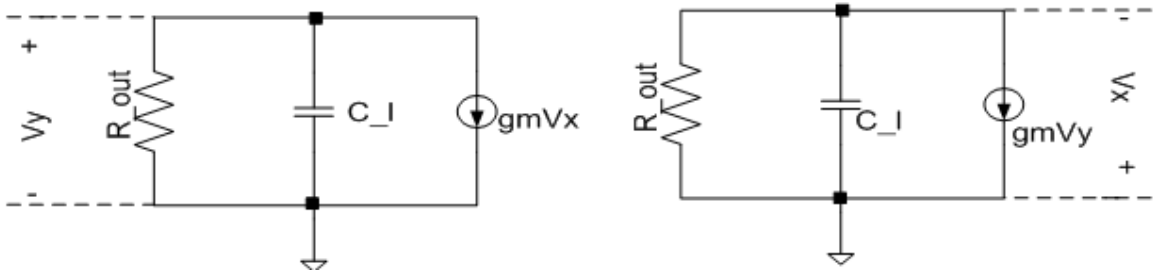
$$V_{out}(t) = V_{in} \cdot g_m \cdot R_{\_out} \cdot (1 - e^{-t_{reg}/\tau})$$

$$Where: \tau = R_{out} \cdot C_{out}$$

gm=i/vin

With Positive feedback- sampled





Small signal representation

Math- Positive feed back comparator latch

$$g_m \cdot V_y = -C_L \cdot \frac{dV_x}{dt} - \frac{V_x}{R_{out}} \qquad g_m \cdot V_x = -C_L \cdot \frac{dV_y}{dt} - \frac{V_y}{R_{out}}$$

$$\begin{cases} \tau \cdot \dfrac{dV_x}{dt} + V_x = -A \cdot V_y \\ \tau \cdot \dfrac{dV_y}{dt} + V_y = -A \cdot V_x \end{cases} \rightarrow \text{where} \quad \tau = R_{out} \cdot C_L, \quad A = g_m \cdot R_{out}$$

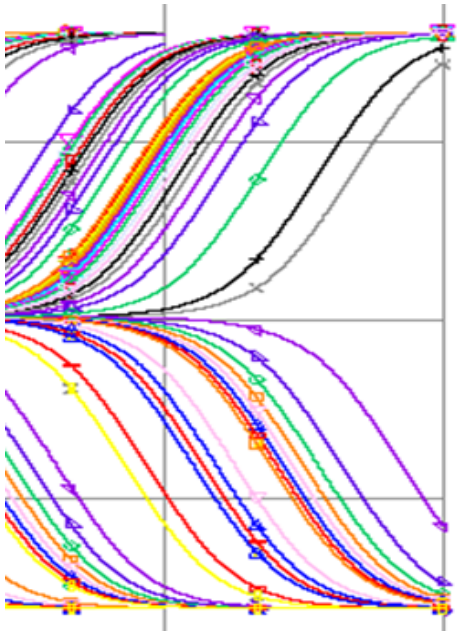
$$\tau \cdot \frac{d(\Delta V)}{dt} = \Delta V(A-1)$$

$$\frac{\tau}{A-1} \cdot \frac{d(\Delta V)}{dt} = \Delta V$$

Solution →

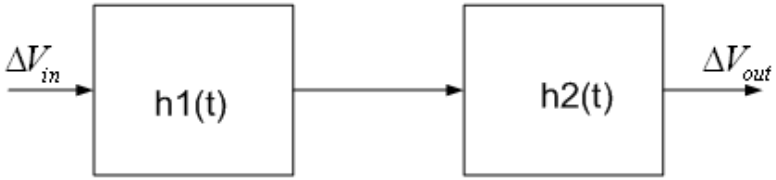
$$\Delta V = \Delta V_0 \cdot e^{\frac{A-1}{\tau} \cdot t} \approx \Delta V_0 \cdot e^{\frac{g_m}{C_L} \cdot t}$$

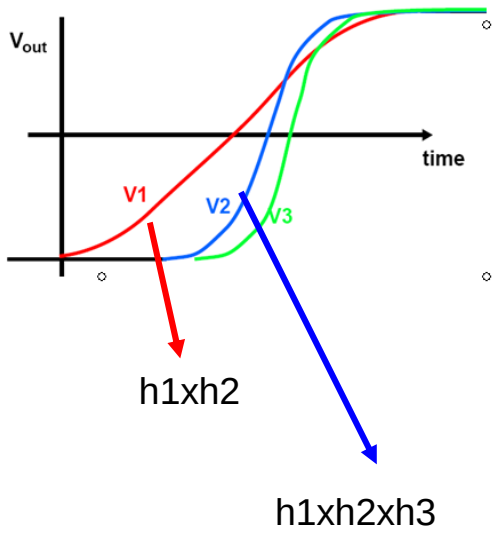
$$\frac{A-1}{\tau} = \frac{g_m \cdot R_{out} - 1}{R_{out} \cdot C_L} \approx \frac{g_m}{C_L}$$



Cascade stages:

Band width reduction





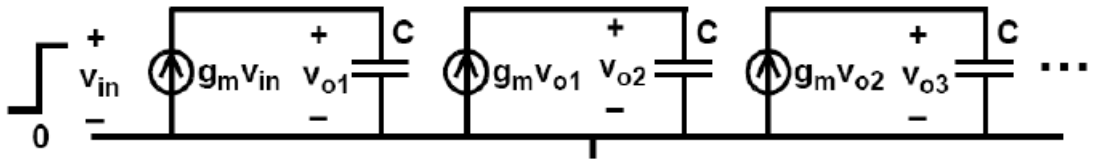
$$h(t) = h_1(t) * h_2(t) = \left(e^{\frac{g_m}{C_L} \cdot t} * e^{\frac{g_m}{C_L} \cdot t} \right) = t \cdot e^{\frac{g_m}{C_L} \cdot t}$$

$$\Delta V_{out}(t) \approx \Delta V_{in} \cdot K \cdot t \cdot e^{\frac{g_m}{C_L} \cdot t}$$

Note: if we have n-stages of the regenerative feedbacks then

$$h_n(t) = h_1(t) * h_2(t) \cdots * h_{n-1} * h_n = \left(e^{\frac{g_m}{C_L} \cdot t} * e^{\frac{g_m}{C_L} \cdot t} \ldots * e^{\frac{g_m}{C_L} \cdot t} * e^{\frac{g_m}{C_L} \cdot t} \right) = \frac{t^{n-1} \cdot e^{\frac{g_m}{C_L} \cdot t}}{(n-1)!}$$

$$v_{oN} = \frac{\omega_u^N}{s^N} v_{in}$$

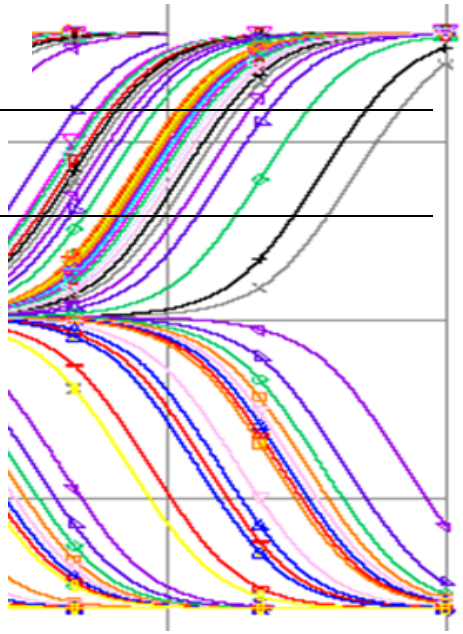


Meta-Stability In Comparator

- Meta-stability is a potentially catastrophic event that can occur when asynchronous inputs and regenerative/flip-flops are used
- Meta-stable outputs are not logic high or logic low and cause delays and system failures
- Meta-Stability is a probabilistic event, because the difference between the input signal and the reference voltage is a random variable
- The smaller the difference between the input signal and reference voltage, the longer the decision time required. On the limit the decision time can approach infinity

Not defined place

Example in class



Analytical Derivation of Meta-Stability & Mean Time To Failure (MTF)

- The probability event given following: where t is the actual comparison time, T is the allowed time

$$\Pr(t > T) = e^{\left(-\frac{A}{\tau}\cdot T\right)} = e^{-\frac{g_m}{C_{out}}\cdot T}$$

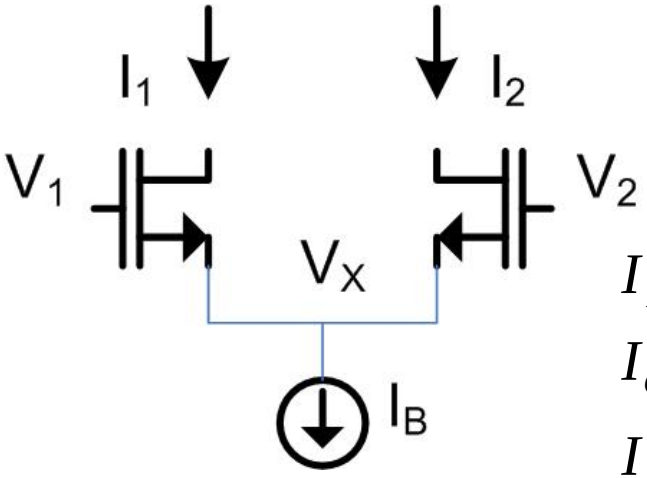
- If one can have a collection of N such comparators all clocking at a frequency fs, then one can found MTF following

$$MTF \approx \frac{e^{\frac{A}{\tau}\cdot T}}{N \cdot f_s} = \frac{e^{\frac{g_m}{C_{out}}\cdot T}}{N \cdot f_s}$$

~ Set it for > month

example in class

The 'CML'



$$I_B = I_1 + I_2$$

$$I_O = I_1 - I_2$$

$$I_B^2 - I_O^2 = 4I_1I_2$$

large signal transfer: assuming square law devices in saturation region.

Express Iout as a function of differential Vi.

$$I_1 = k(V_1 - V_X - V_T)^2$$

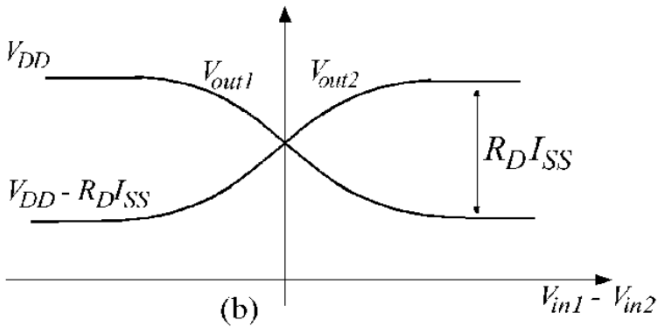
$$I_2 = k(V_2 - V_X - V_T)^2$$

$$V_i = V_1 - V_2 = \sqrt{\frac{I_1}{k}} - \sqrt{\frac{I_2}{k}}$$

$$kV_i^2 = I_1 + I_2 - 2\sqrt{I_1I_2} = I_B - 2\sqrt{I_1I_2} = I_B - \sqrt{I_B^2 - I_O^2}$$

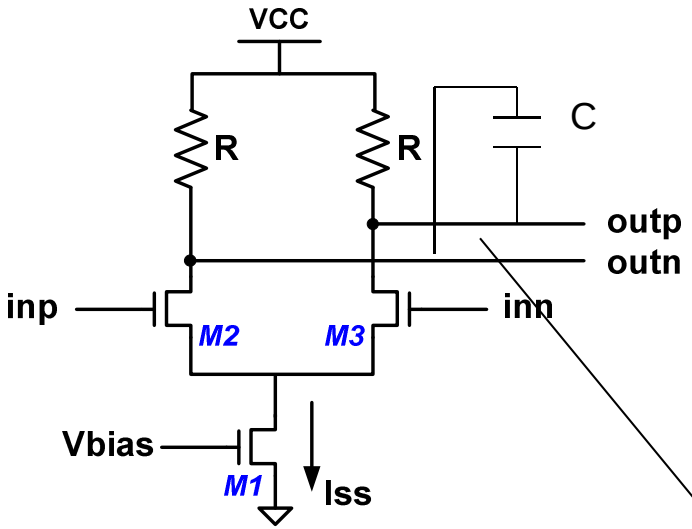
$$I_O = \sqrt{2I_Bk}\cdot V_i\sqrt{1-\frac{k}{2I_B}V_i^2}$$

(I1-I2)R



Resulting expression is a linear term multiplied by a non-linear square root function.

The 'CML'



- **CML (current mode logic) is a differential structure**
  - **Basic block in Ananlog/Mixed signal**
  - **Less sensitive to supply noises and noise from aggressors**
    - **Less noise (AC current) injected to supply -> less supply noises in analog portion**
  - **Good for high speed operation**
    - **No PMOS devices (slower)**
    - **Differential switching is faster than single ended rail-to-rail**
    - **Noninverting cells are just as fast as inverting cells (unlike CMOS: inverter vs. buffer)**
  - **Drawback: Static current consumption**

- **The output load (CL) and the operation speed (BW) determine the value of R***
- **CL must include the capacitance of the next stages and all parasitic capacitances of wires and Cgd of switching transistors in differential pair**
- **f must be taken higher than target frequency for margin (10% higher)**

- **When used in large signal inputs !**
- **The typical CML swing for 1.2V process is 400mV -> this determines Iss, Iss = 400mV/R**

1. **P. Heydari & R. Mohanavelu, "Design of Ultrahigh-speed Low-V CMOS CML Buffers..", 2004**

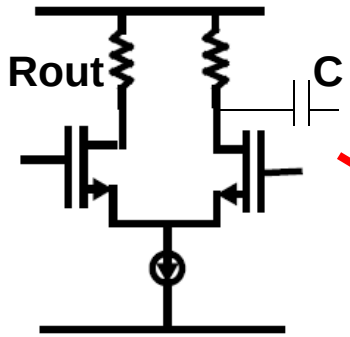
$$f_{3dB} = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi C f_{3dB}}$$

$$G_{m\_avg} = \frac{g_{m\_ss}}{\sqrt{2}}$$

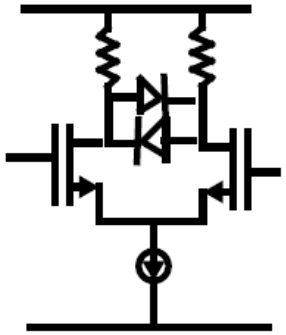
Front stage Architectures- with resistors

1. Use small values of R_l
   - Minimizes swing
   - Shortens time constant



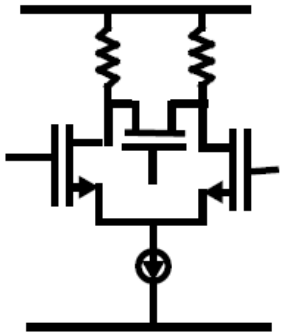
$$V_{out}(t) = V_{in} \cdot g_m \cdot R_{\_out} \cdot (1 - e^{-t_{reg}/\tau})$$
$$Where: \tau = R_{out} \cdot C_{out}$$

2. Use Passive Clamps
   - Limits Swing
   - Adds parasitics



BW = 1 / 2pi(RoutC)

3. Use active nulling clamps
   - Good in principle
   - Tough clock generation problem

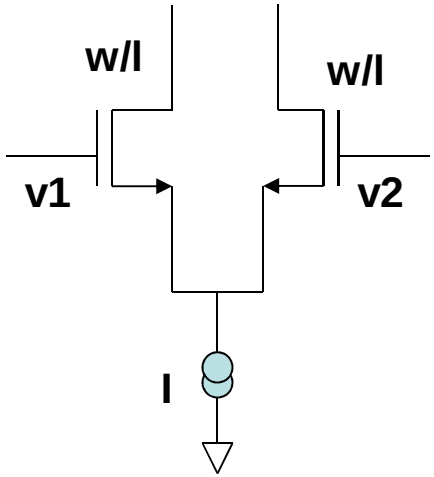


Source: P Gray

Summary:
Number of stages and gain needed
is process and project dependent no fixed analytical solution.

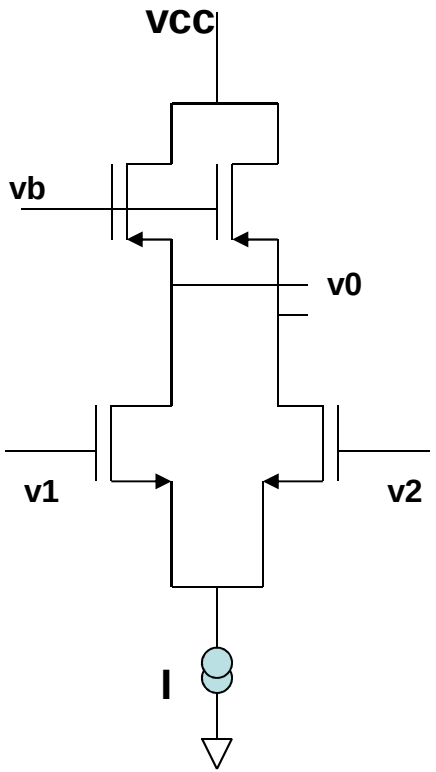
Best empirical gmR=4-8 number of stages ~ 2-4

Input stage: Architectures options- using P cmos



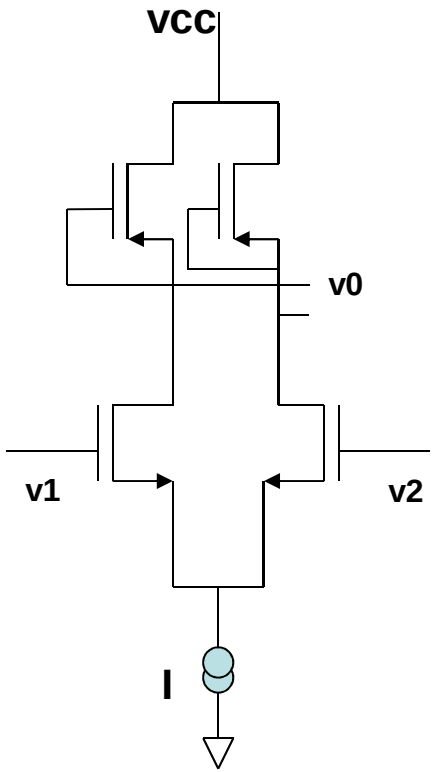
gm x what

A



Gm x Rop/Ron
Kickback
Large gain

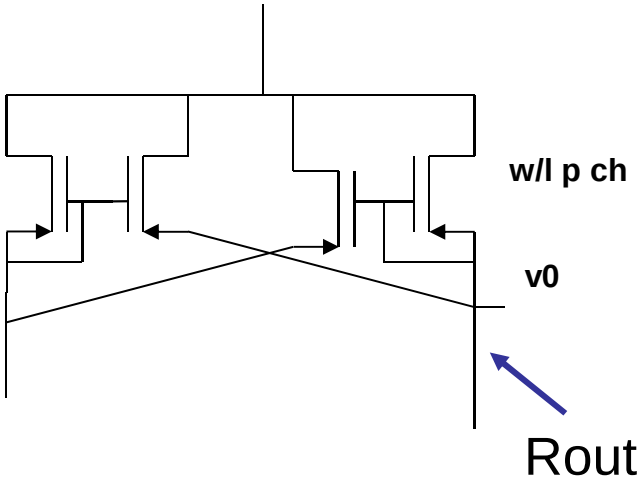
B

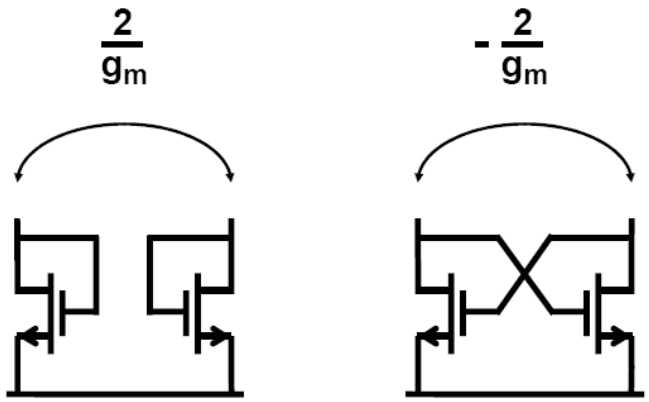


Gm x 1/gmp
Low gain

C

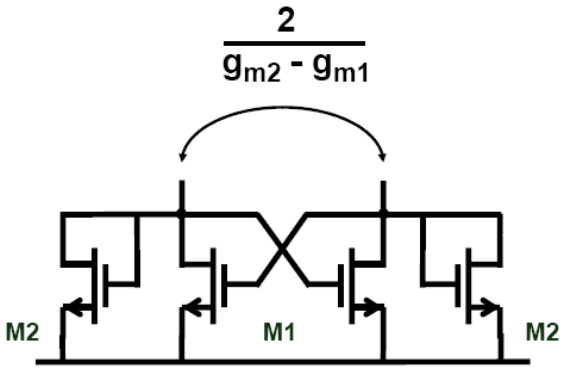
Added feed back to load





positive feedback to raise Rout

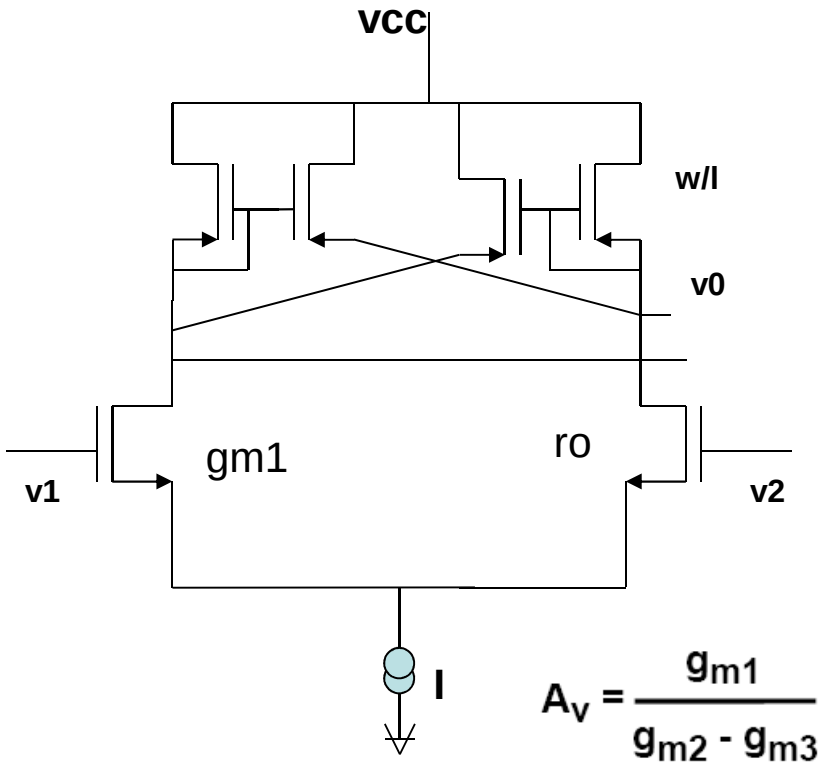
Effective rout =infinite



Values close to ∞ !

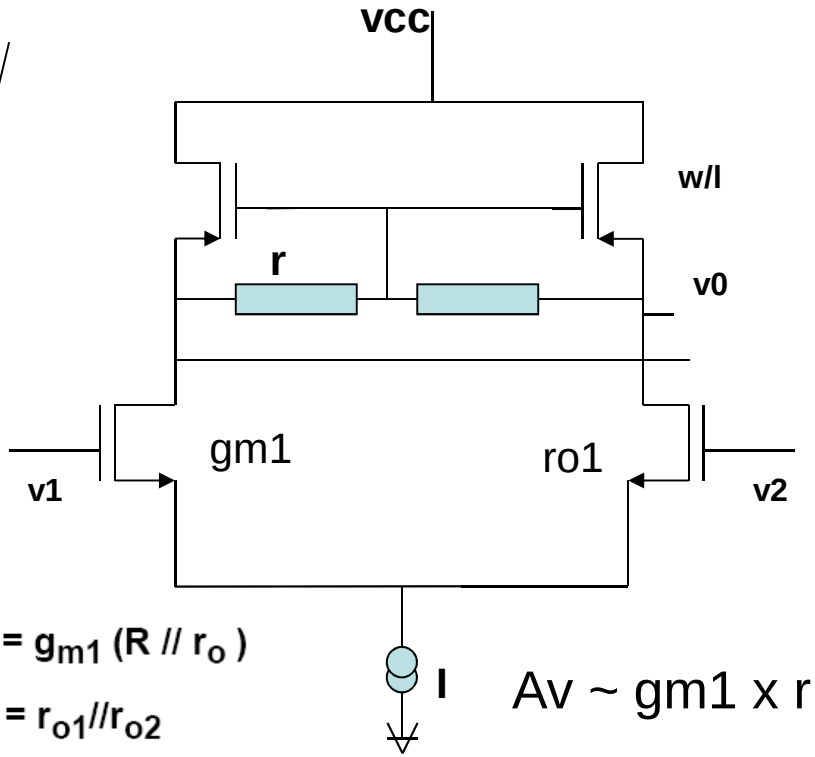
Source: Willy Snasen 2005

Input stage: Architectures options



$$A_V = \frac{g_{m1}}{g_{m2} - g_{m3}}$$

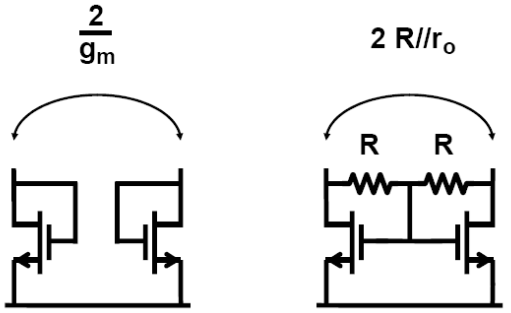
AV ~ gm1 x ro



$A_V = g_{m1} (R // r_o)$

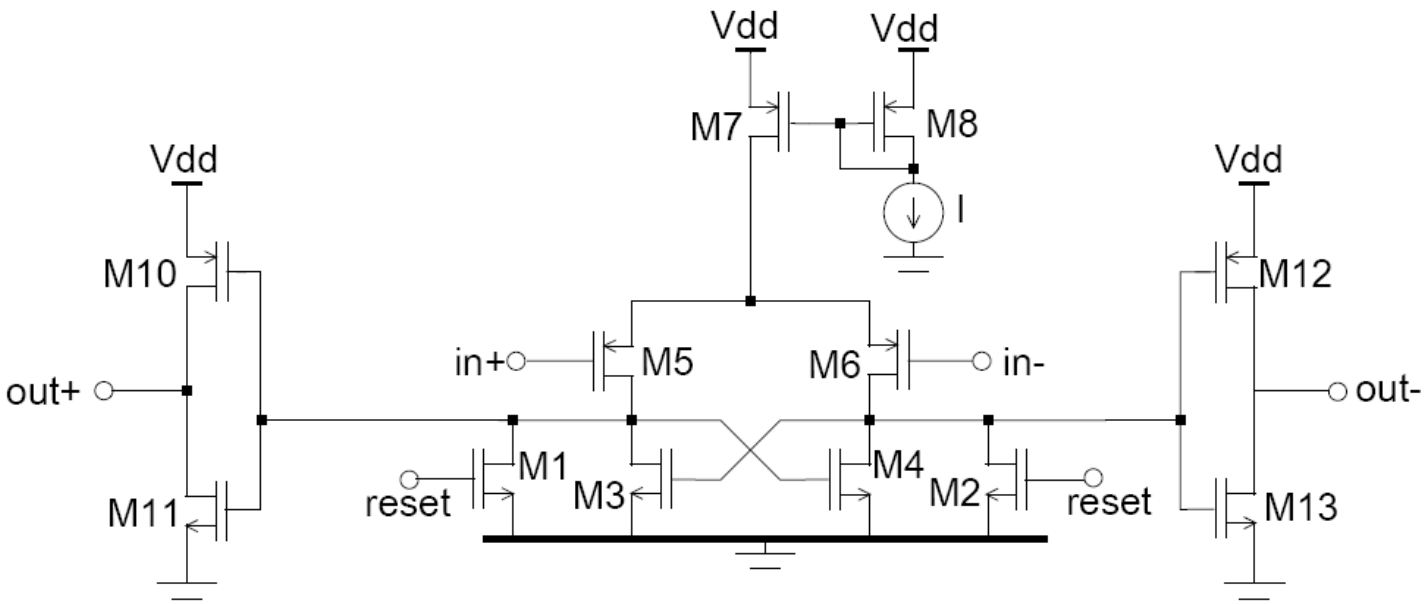
$r_o = r_{o1} // r_{o2}$

Av ~ gm1 x r



Source: Willy Snasen 2005

Comparator Examples

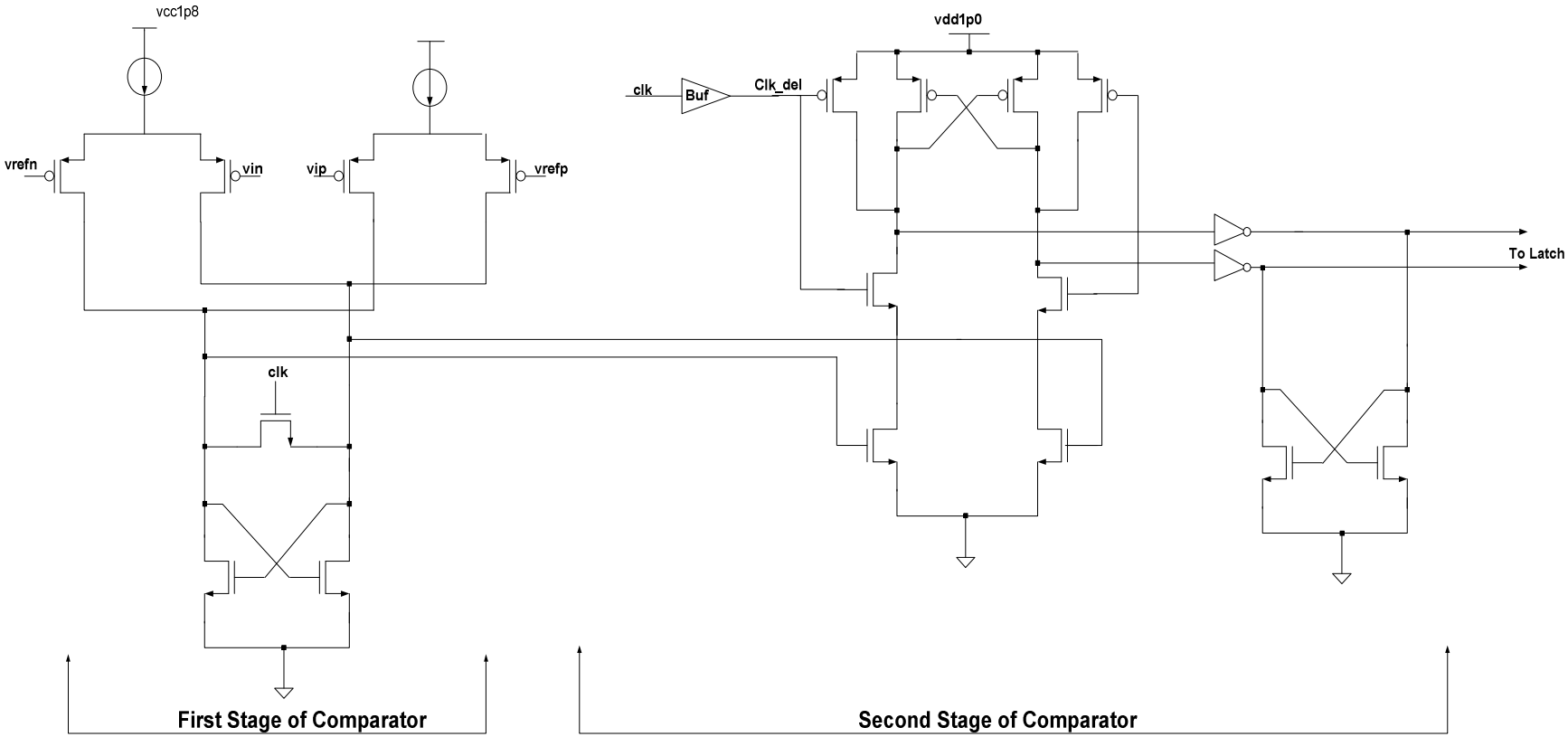


Simple

Good for low supply
Reset switch to ground
Kick back

Question can the outputs (inverter) swing to Vss ?

Differential input Two Stage Comparator Option (no pre_amp)



More Example of comparators

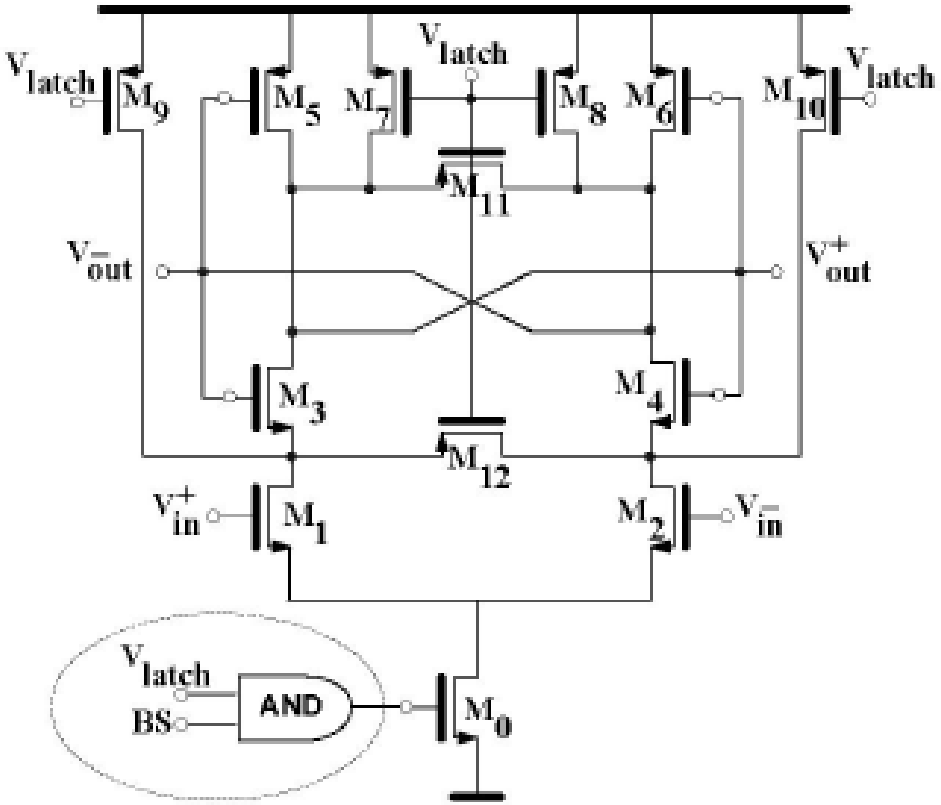


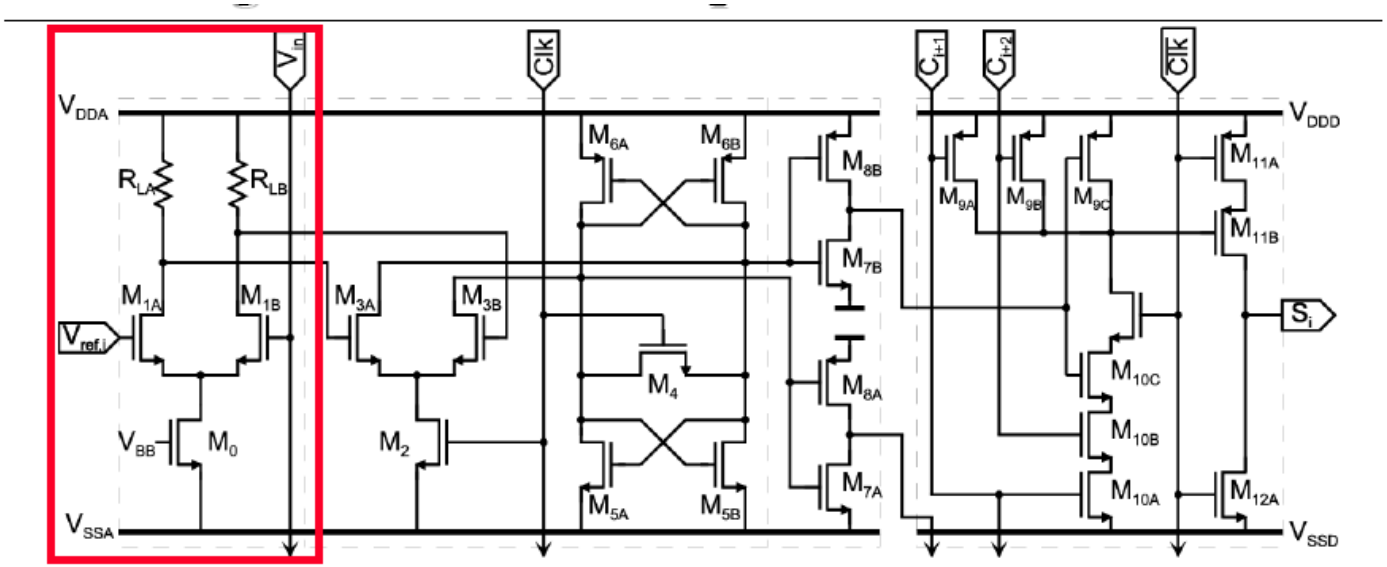
Fig. 5: High speed comparator and its switching circuit

A Power-Efficient 1.056 GS/s Resolution-Switchable
5-bit/6-bit Flash ADC for UWB Applications

Jun-Xia Ma, Sai-Weng Sin, Seng-Pan U [1], R.P.Martins [2]

Special Topics – Calibrated and differential

Architectures examples



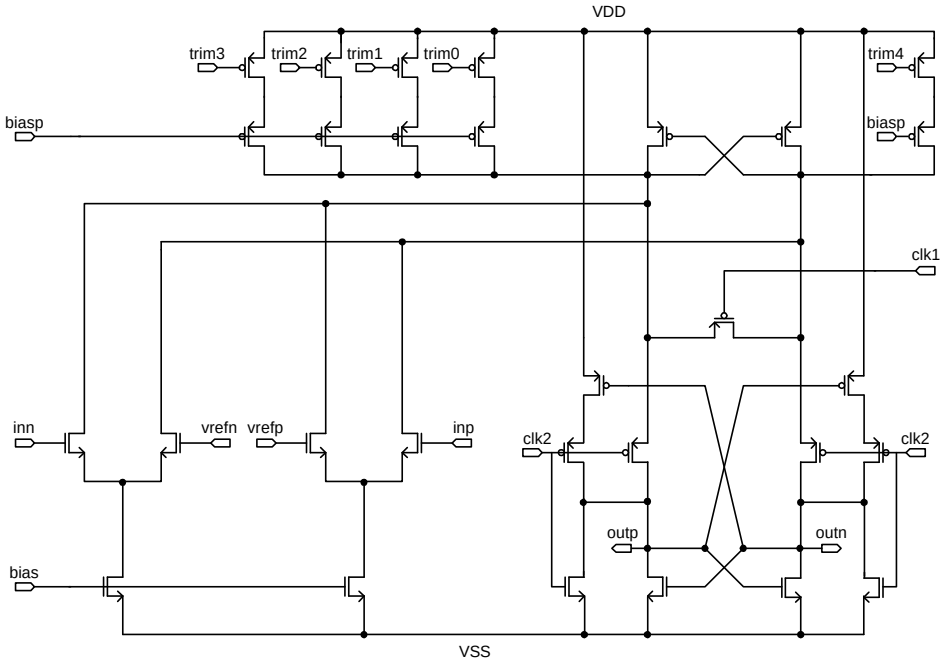
- ***Pre-amplifier [M1a,M1b]***
  - **Differential Pair with resistive load**
  - **Reduce Kick-back noise**
  - **Reduce Input Referred Offset Comparator**

Source: Esat-Micas esscirc00

Offset calibration of Comparators:

Why : Main reason lower input capacitance

DIFFERNTIAL: LATCHED With CALIBRATION AND DIFFERNETIAL !



A 10.3GS/s 6bit (5.1 ENOB at Nyquist) Time-Interleaved/Pipelined ADC Using Open-Loop Amplifiers and Digital Calibration in 90nm CMOS

Ali Nazemi[1], Carl Grace[1], Lanny Lewyn[1], Bilal Kobeissy[1], Oscar Agazzi[1,2], Paul Voois[1], Cindra Abidin[1], George Eaton[1], Mahyar Kargar[1], Cesar Marquez[1], Sumant Ramprasad[1], Federico Bollo[2], Vladimir A. Posse[1], Stephen Wang[1], Georgios Asmanis[1]
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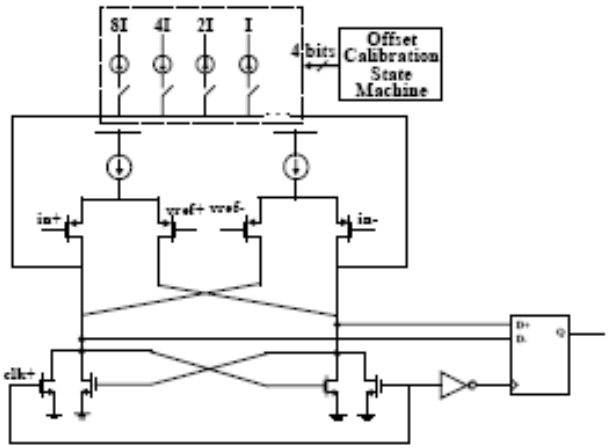
[2]ClariPhy Argentina S.A., Cordoba, Argentina



Comparator schematic with digital offset calibration.

End Lecture 7b + 8