Welcome to

046188 Winter semester 2012

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 7 (part a)

FLASH ADC ARCHITECTURE ALTERNATIVES

www.gigalogchip.com

ALTERNATIVE DESIGNS OF FLASH ADC

SUB-RANGING ADC

Charge Flash architecture

Differential Architecture

FLASH ADC- SUMMARY

Bad-Good

Monotonic

Very fast, No amplifiers, Resistors can match well to 10b

Design Issues:

Big input capacitance

Comparator offset is an issue

Clocking routing sampling time

Meta stability

Decoding to avoid bubbles

If S/H is used – Distortion added

Hardware:

Exponential in complexity

High in power for 7 bits or more (127 comparators)

Could lead to large die size

References may need to be filtered from kick back

Medium: to scale down in technology → power supply!

Power ~ 2 to N

Area ~ 2 to N

Cin ~ 2 to N

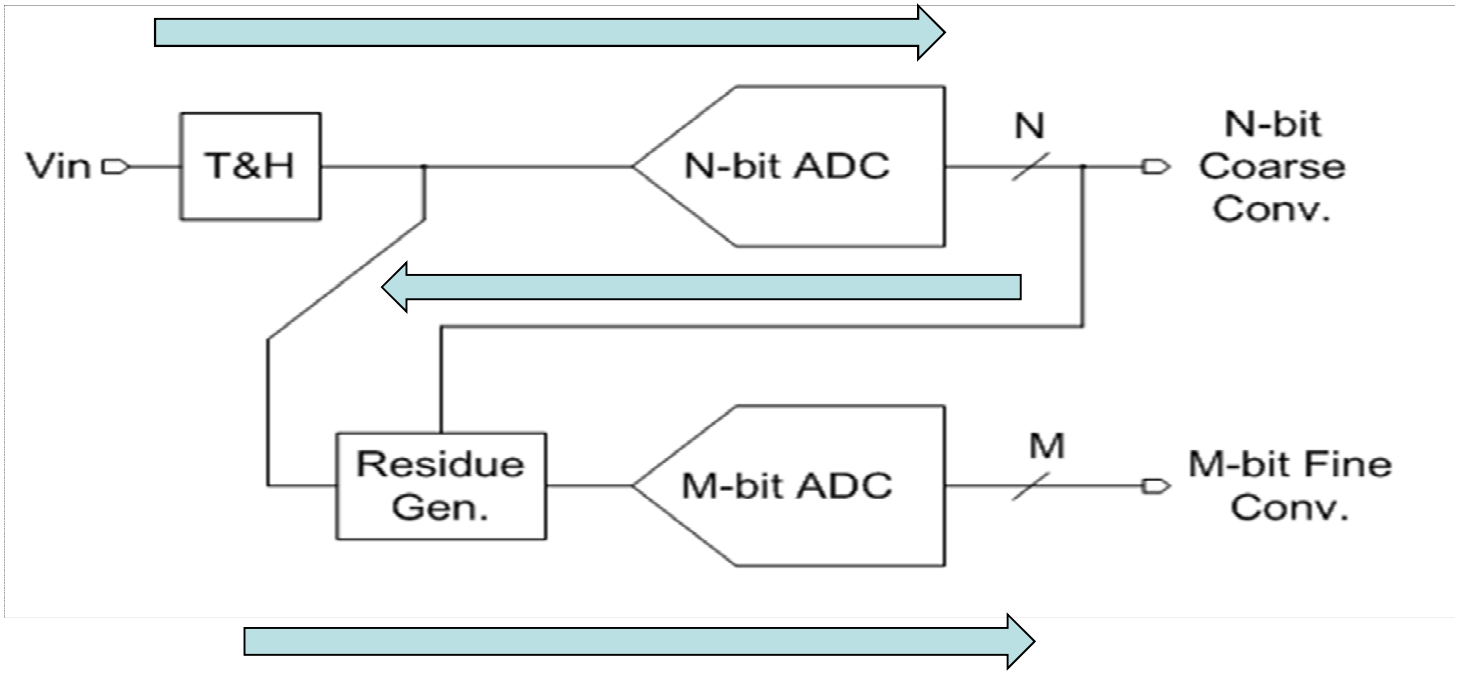
R ladder ~ 2 to N

Here N is an increase of effective resolution

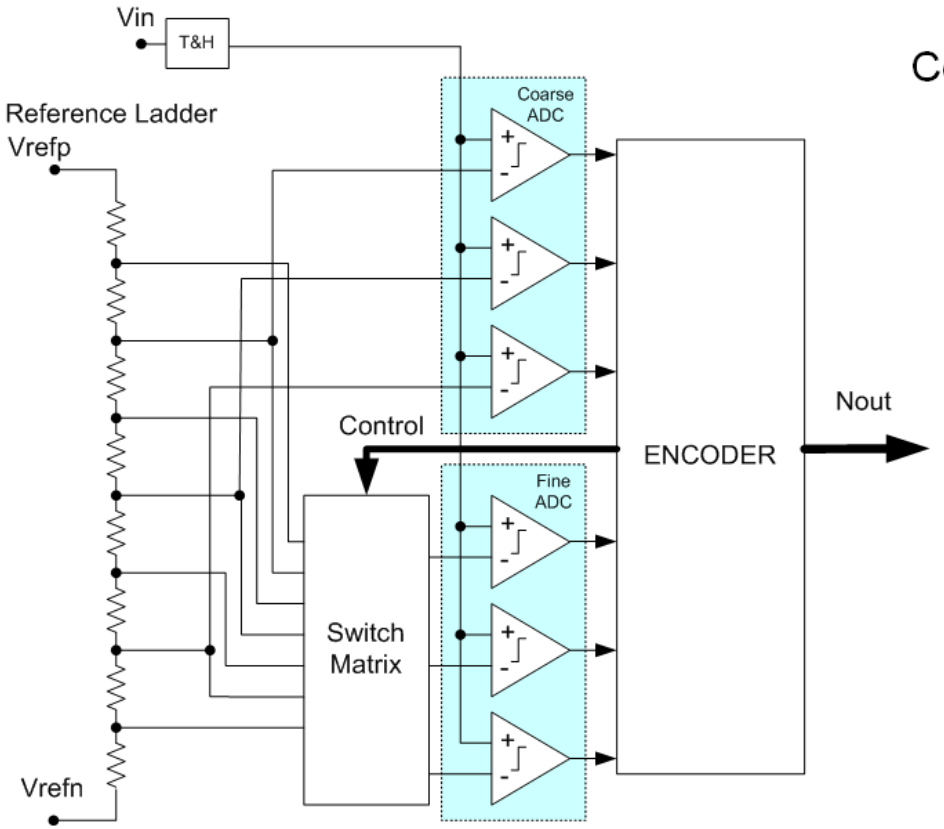
Since Flash ADC in silicon Area and Power grows exponentially . How about different architecture

Sub-ranging ADCs

Concept


Vin
T&H
N-bit ADC
N
N-bit
Coarse
Conv.
Residue
Gen.
M-bit ADC
M
M-bit Fine
Conv.

Sub-Ranging ADC Basics



Conversion is done in two steps

- coarse ADC determines the region of the ladder the fine ADC will use
- regions can overlap to produce the redundancy that relaxes the offset requirement for the coarse ADC
- for the fine ADC – strict offset requirements

Fine is waiting for the Coarse (MSBs) – need S/H
How to partition ? 10 bit can use 31 comparators for Coarse and 32 for fine = 63 instead of 1024
Or 63 for coarse (6 bit) and 15 for fine ?

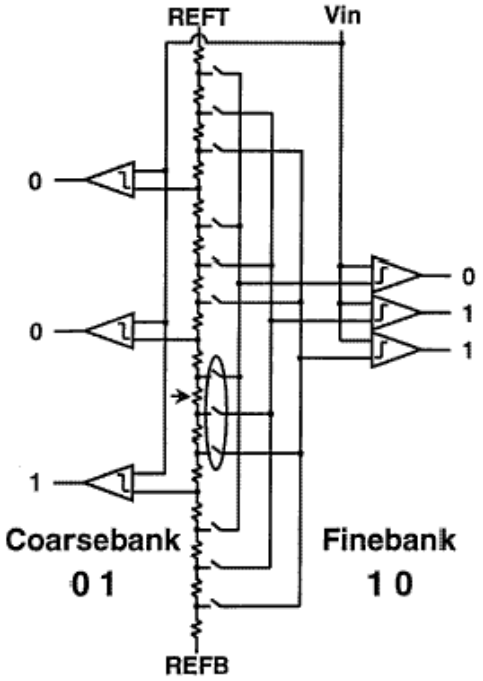
Two-step: subranging ADC

+ $2(2^{N/2}-1)$ comparators

  Coarse bank selects which part of reference ladder to connect to fine bank

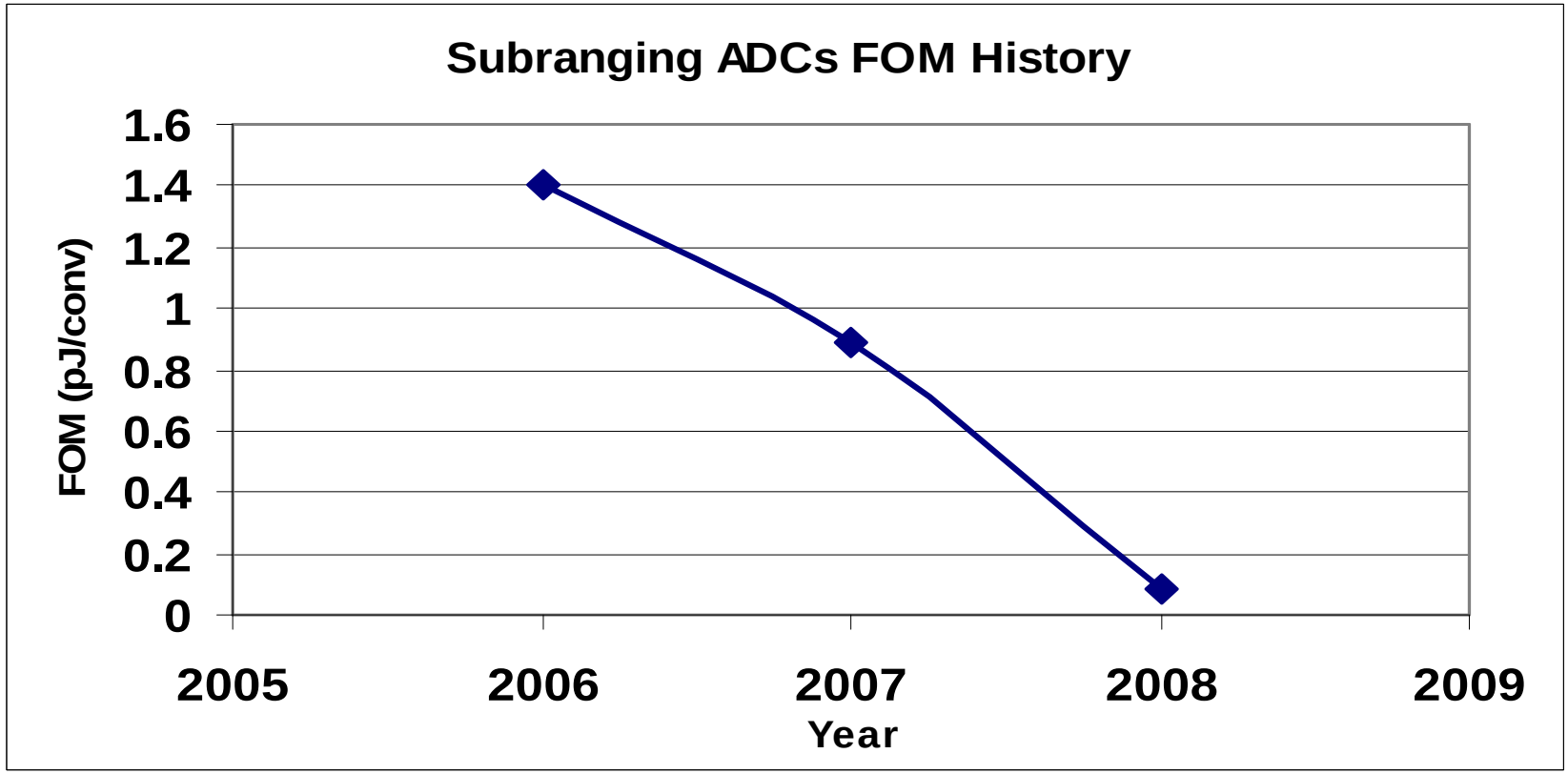
- Speed limited by settling of fine references

  parasitic capacitance from > 2^N switches + large kickback



Source: BRCM

Lost time- Need twice the time and S/H.
Resistor get glitches now impedance is important
New many switches (2 to the N – M Coarse connection **)**



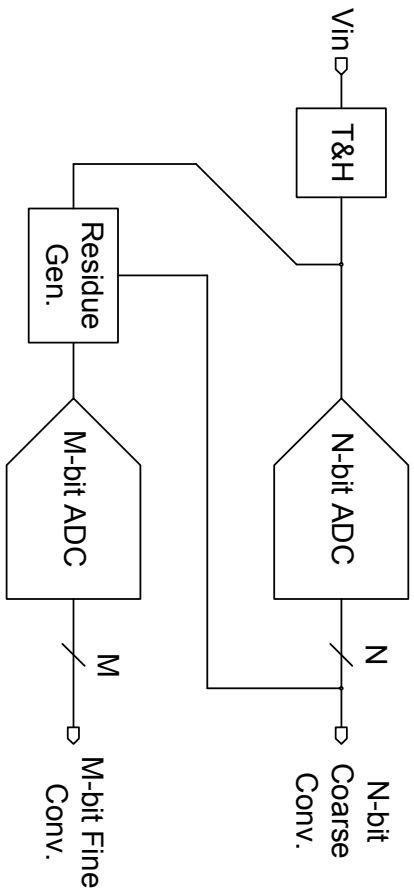
2006 ➔ 6b & 1Gs/s (90nm CMOS)

2007 ➔ 10b & 160Ms/s (90nm CMOS)

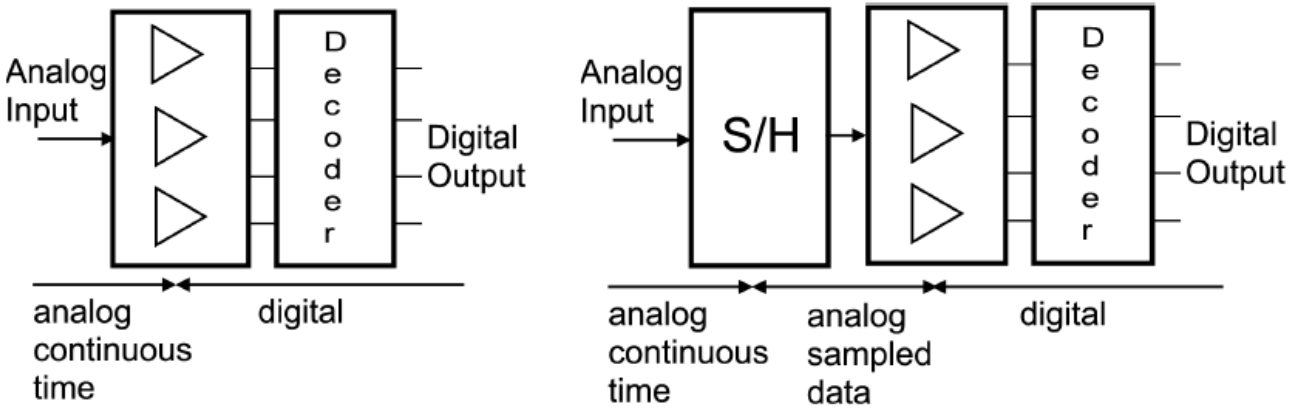
2008 ➔ 5b & 1.75Gs/s (90nm CMOS)

Summary: : Sub-ranging ADCs

- Power efficient
  - Two low resolution ADCs operating in a pipeline manner
- Reduced speed
  - Throughput can be still very high
- T&H is inevitable
  - The most critical component in the architecture
  - Loading is relaxed
- Residue generation
  - Needs M+N bit accuracy
- Interleaving is possible
- State of FOM is around 0.5pJ/conv



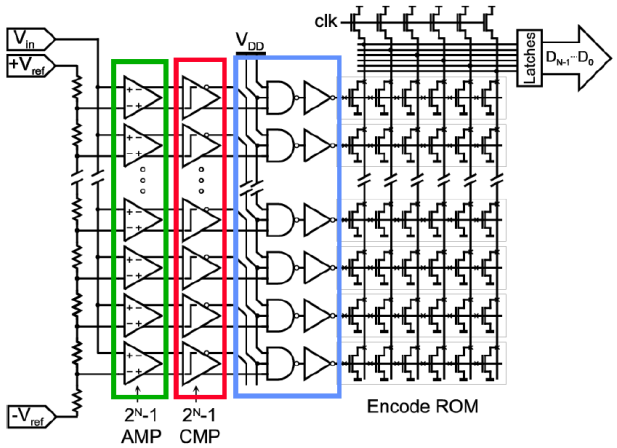
SH Versus clocked flash (“mandatory” in Sub-Ranging



Source: KU Leuven

SH will draw 20-40% more power

Flash architecture with digital corrections 1GHz/6 bits



Avantages :
Remove sample and hold – make clocking harder
Use comparators as sample and hold
Use pre gain comparator – Option
Error correction logic
ROM Grey encoder
Now task is on the clock to be accurate to all comparators

Capacitive Charge FLASH

Architecture Alternative: Capacitive Charge ADC

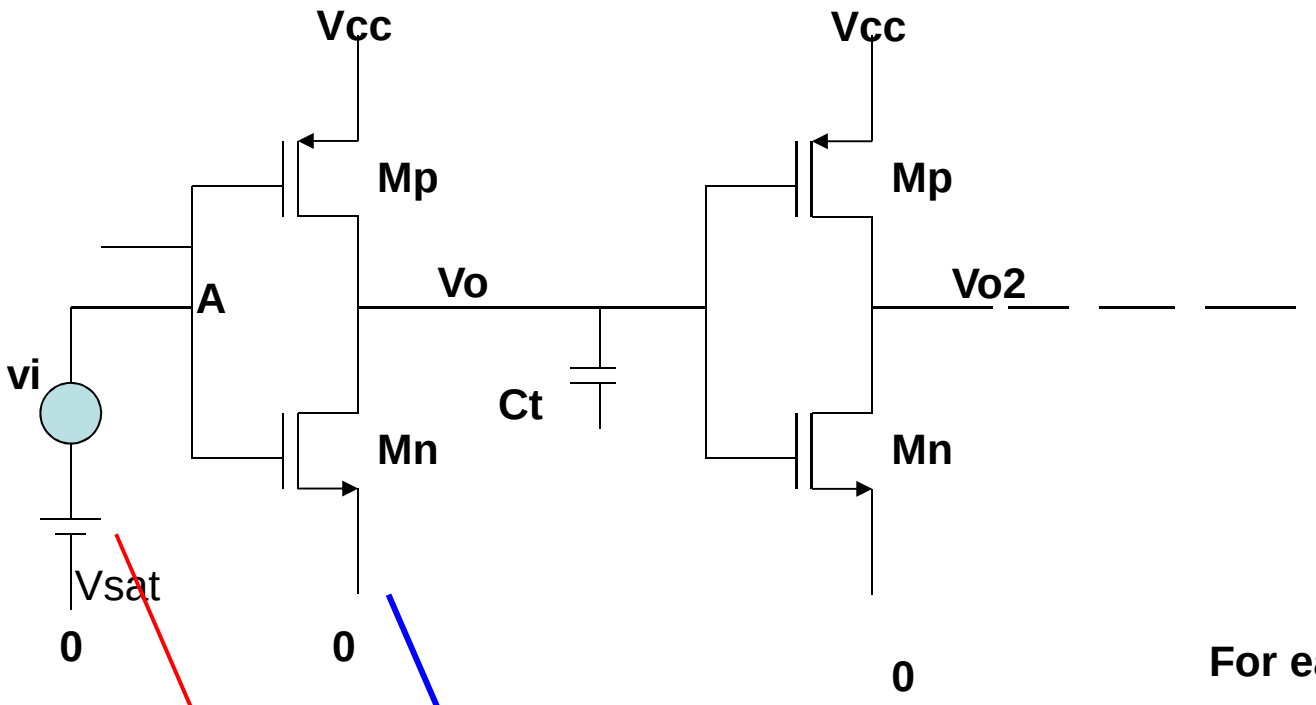
Save power- simplified the complex comparator design
Can we use an inverter as simple gain stage
Use capacitors to transfer (Vin- Vref) x gain.

Why ?

Inverter is a digital cell no special process needs
It draw 0 DC current (power)
very fast and simple, power is lower..
(Offset cancellation is build in) !

With 2 capacitors..we can build a simpler comparator

Operation- Inverter chain- as gain stage



For each stage

Av(dc) = (gMn+gMp) x rop//ron

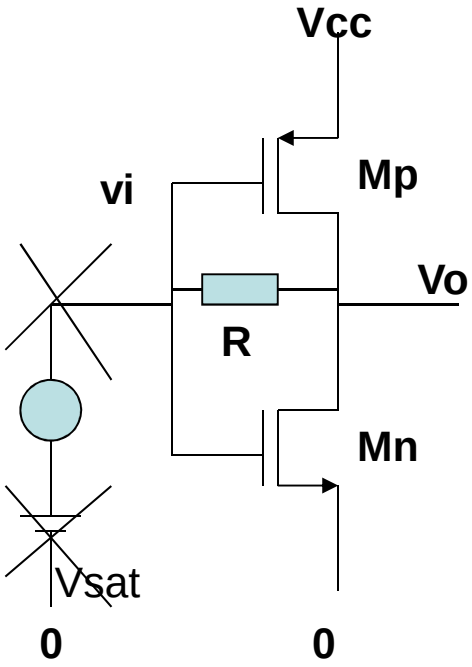
Pole = 1/ 2pi Ct (rop//ron)

Amplification is done but

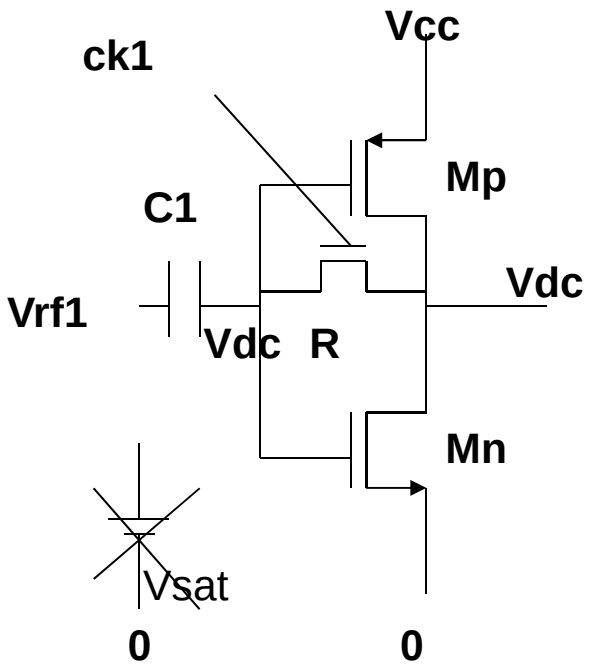
Next how to fix the DC, mid point ? (in saturation)

Next: Can we create differences with one input- at A

Fix the DC point and insert the first input level across a capacitor



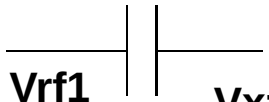
Step 1



Step 2

Ck1=H

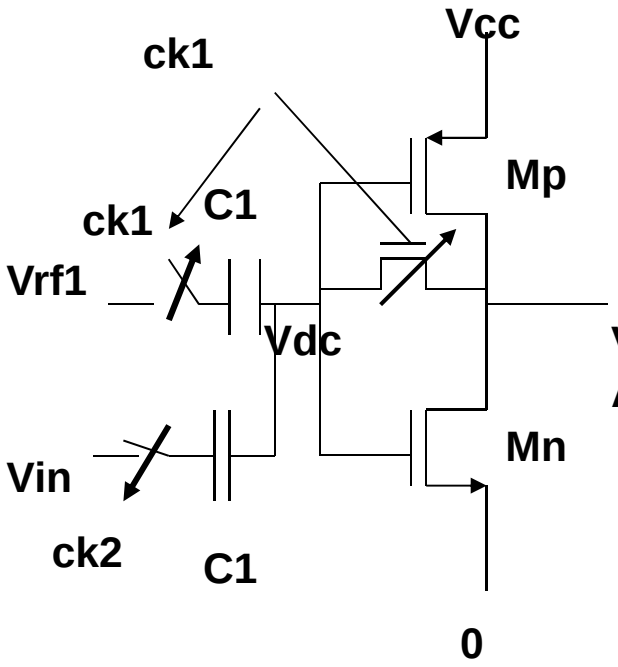
Model at ck1=1



Q1=C(Vrf1-Vx)

v0=vi the inv. is for sure in
Saturation and in low gain/impedance

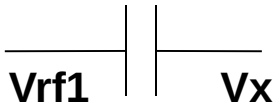
Insert the second level - Subtraction and gain



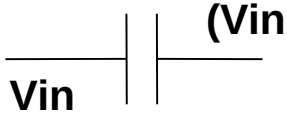
V0=(Vrf1 - Vin)Ao(f)
And No offset.

Q1=C(Vrf1-Vx)

Model at ck1=1

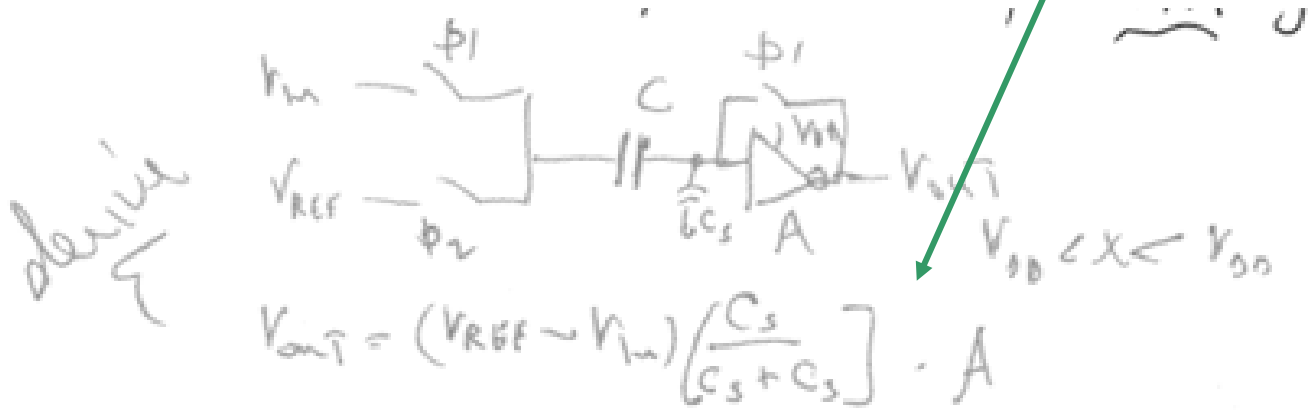


Model at ck1=0

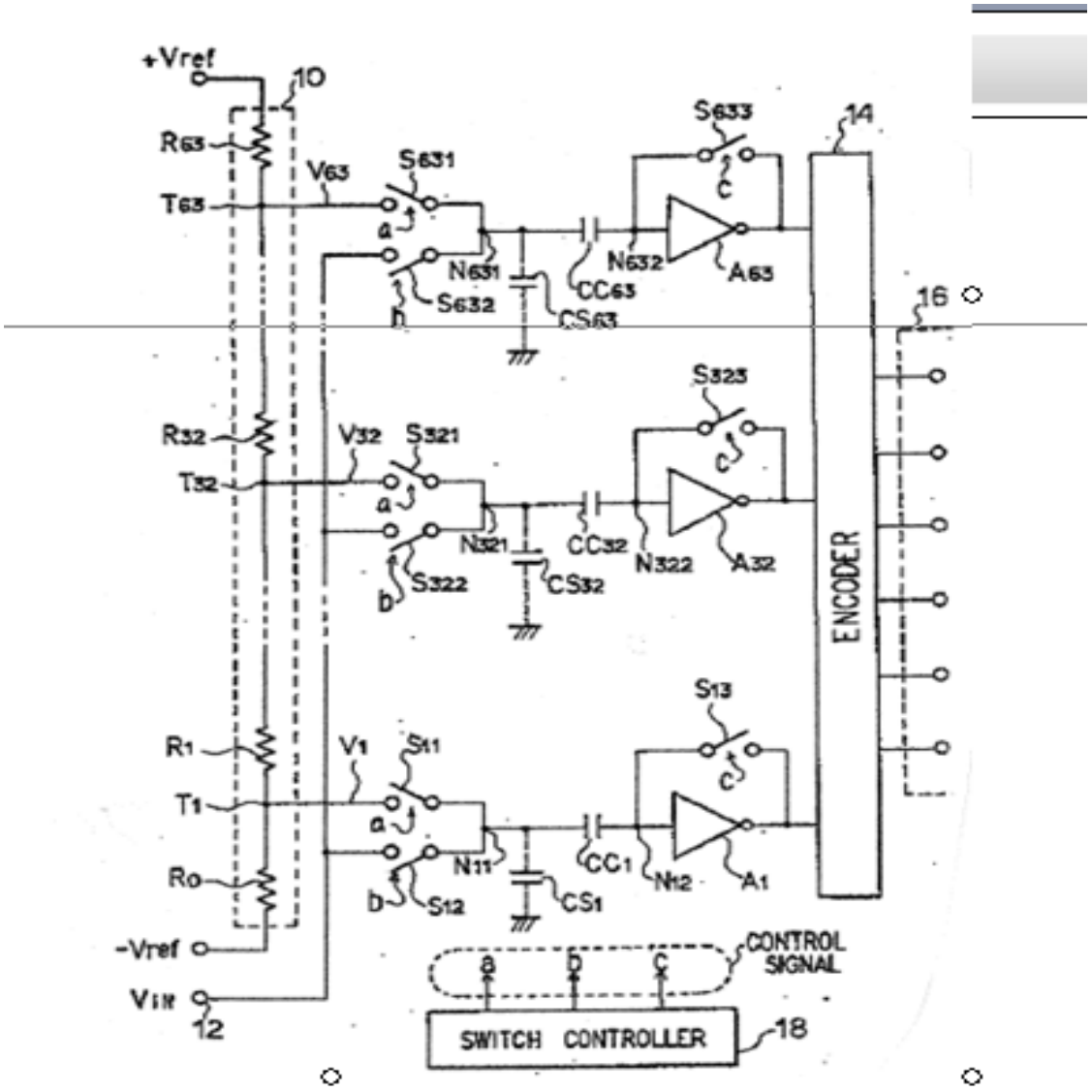


(Vin-Vrf1)+Vx

Step 3
Ck1=0
Ck2=H



Example: Create the ladder codes.



Source: Fairchild Data sheet

Speed example in class..

Speed Estimation:

6 bit ADC, no S/H
At L min130 nm (Cox ~ 13ff/uu) can get to 1-2 GHz – Flash “only”

Example:
Input Delay= 150ps (5.5/2piRCin + RladderCgs/2 to drive 63 comp/calibrate)
+ 250ps comparator + 100ps logic (25ps/gate) = 500 ps max
Possibly latch after comp and save some of the 100ps. (50ps)

Sample at 2.0GHz max through put (Input frequency)
twice the min delay ~ 1 GHz

Differential /improved implementation In FLASH architecture

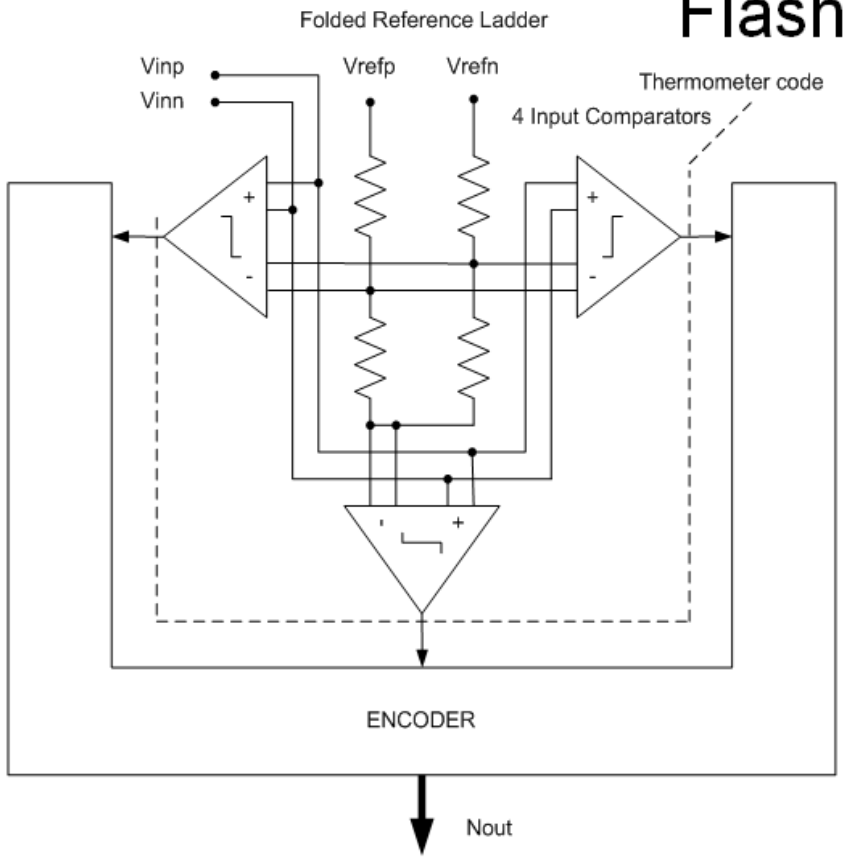
Differential Design

DIFFERENTIAL

INL GOES TO 0 In the middle
Signal is doubled routing is harder

Simple to make differential comparator

Flash ADC Basics (2)



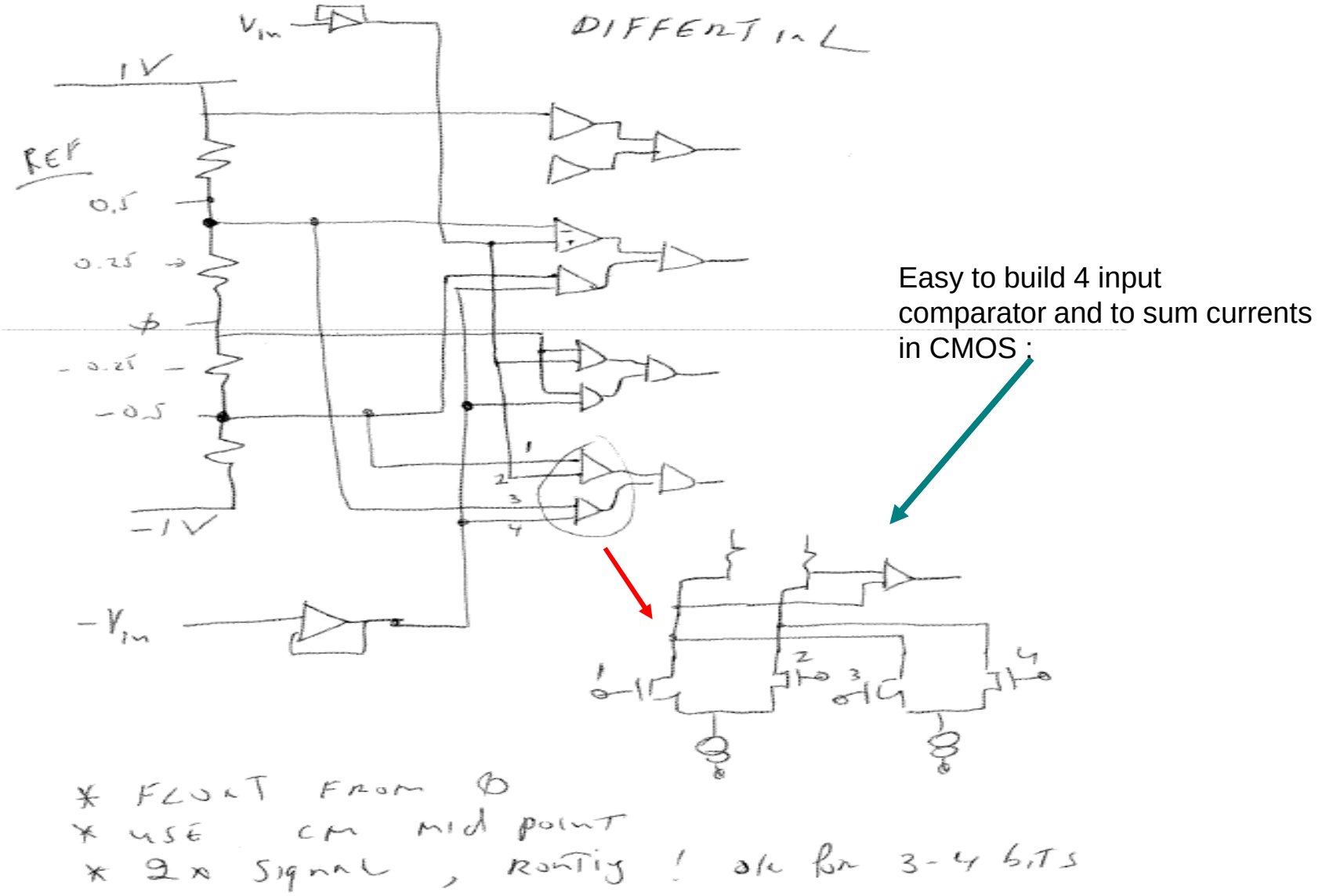
Fully differential implementation:

- wider dynamic range
- better noise immunity
- better linearity

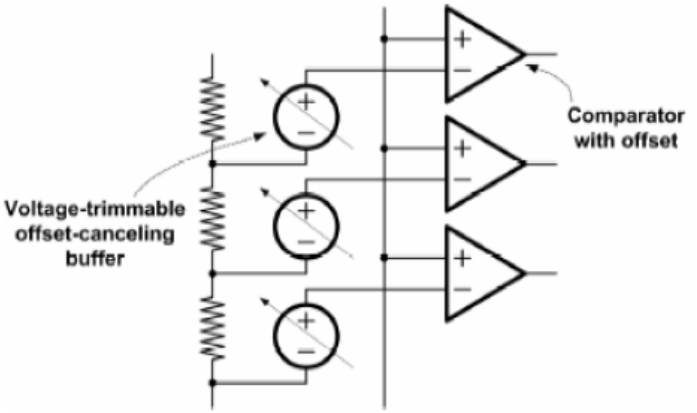
Other reasons :

Symmetry is preserved HD2, HD4 get reduced/cancelled

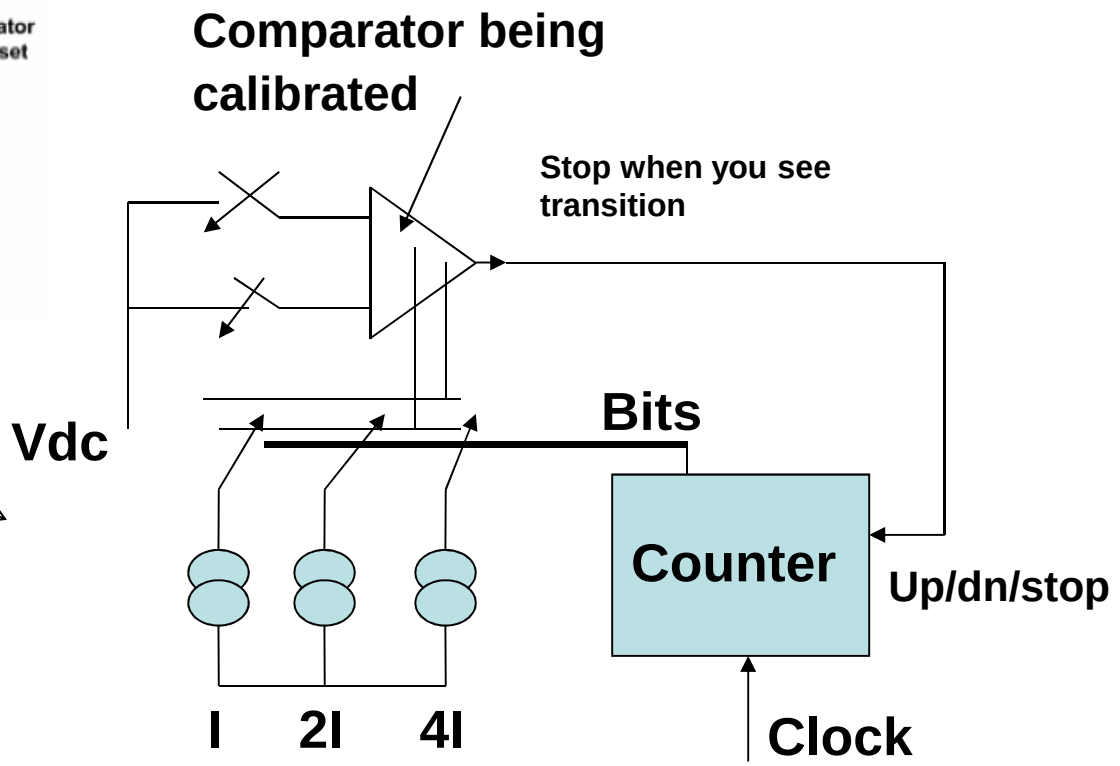
DIFFERENTIAL-details



Offset Cancellation/reduction



B. E. Boser



Select ~7I for maximum offset possible

Source: KU Leuven

Alternative offset cancellation

Easy to do in start up.

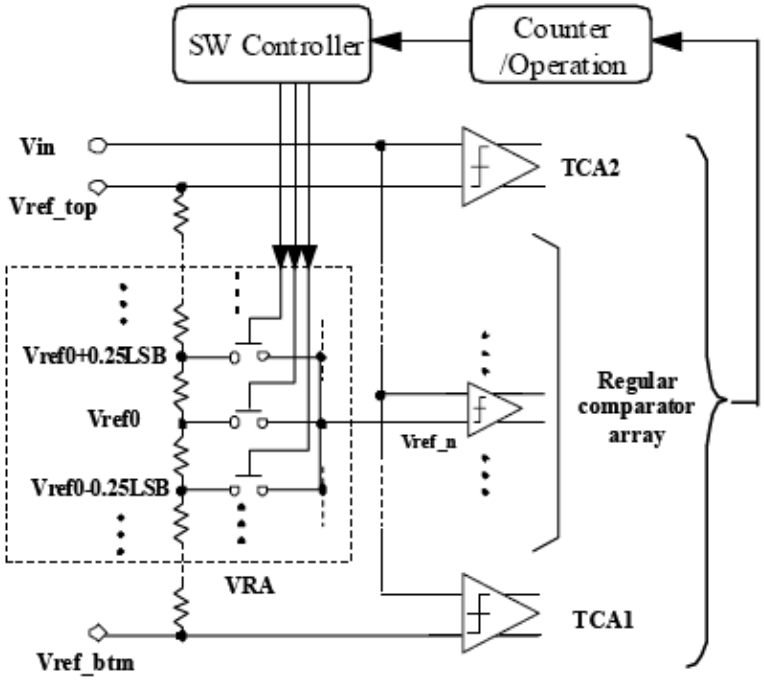


Figure 2: Architecture of offset cancel circuit.

We can go "wild" with good ideas:

Find offset connect comparator to different point on the ladder

Add small DAC to each comparator find trip point (Feed back)- last foil.

Remember the offset in digital code and offset the digital information

Offset Calibrating Comparator Array for 1.2-V, 6-bit, 4-Gsample/s Flash ADCs using 0.13-um generic CMOS technology

Hiroyuki Okada, Yasuyuki Hashimoto,
Kohji Sakata, Toshiro Tsukada, Koichiro Ishibashi

End lecture 07 part a.

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