Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

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TEL AVIV UNIVERSITY אוניברסיטת תל אביב

Lecture 7

SUCCSSESIVE APROXIMATION ADC: Operation

Design of Time Continuous SARs

Design of Switch C SAR

Error sources

Lectures are placed in my site:
http://www.gigalogchip.com/lectures.html

Agenda

- ADC Architectures
- SAR ADCs
- Error Sources

A/D Converter ca. 1954

- 19" × 15" × 26"
- 150 lbs
- 500W
- $8,500.00

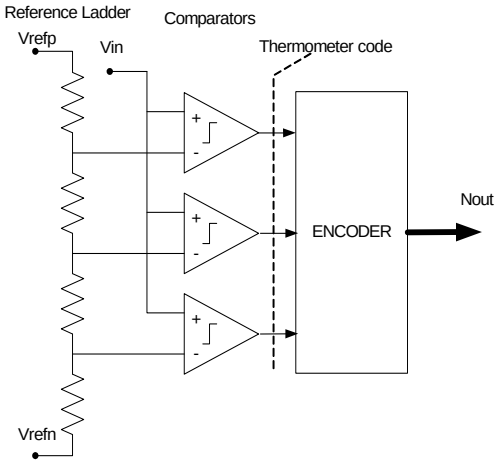
Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

http://www.analogic.com

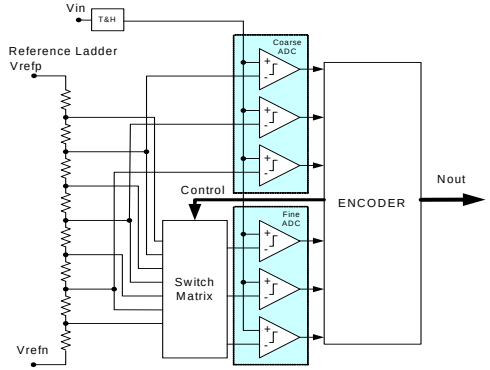
Figure 4.3: *1954 "DATRAC" 11-bit, 50-kSPS SAR ADC Designed by Bernard M. Gordon at EPSCO*

B. Murmann 7

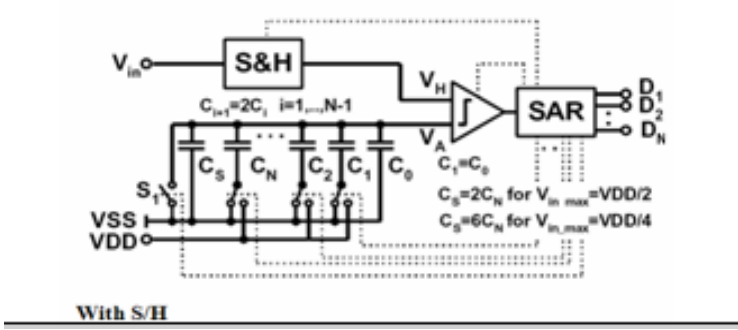
Common aata acquisition architectures



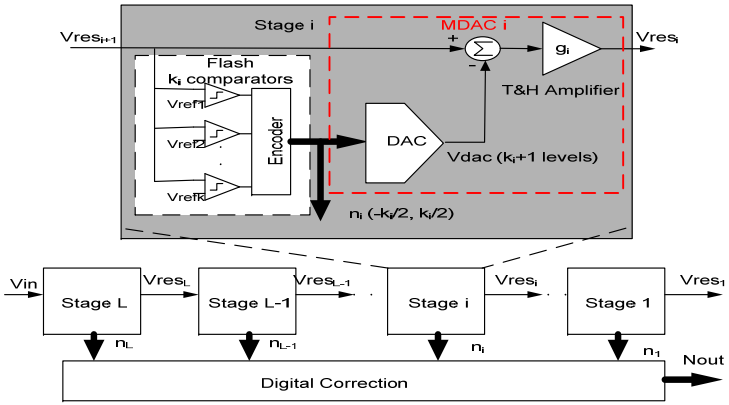
FLASH ADC



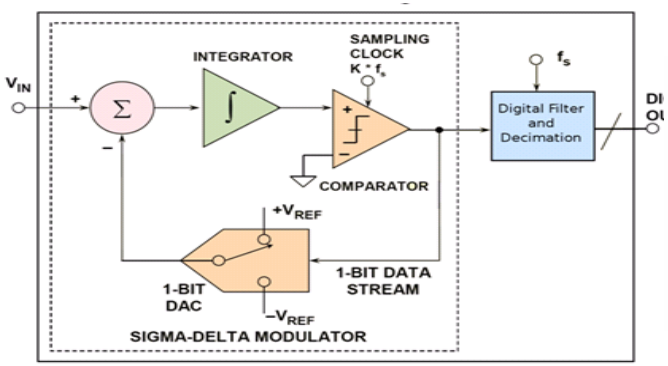
Sub ranging



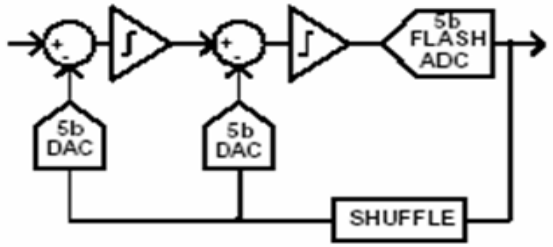
SAR



Pipe Line

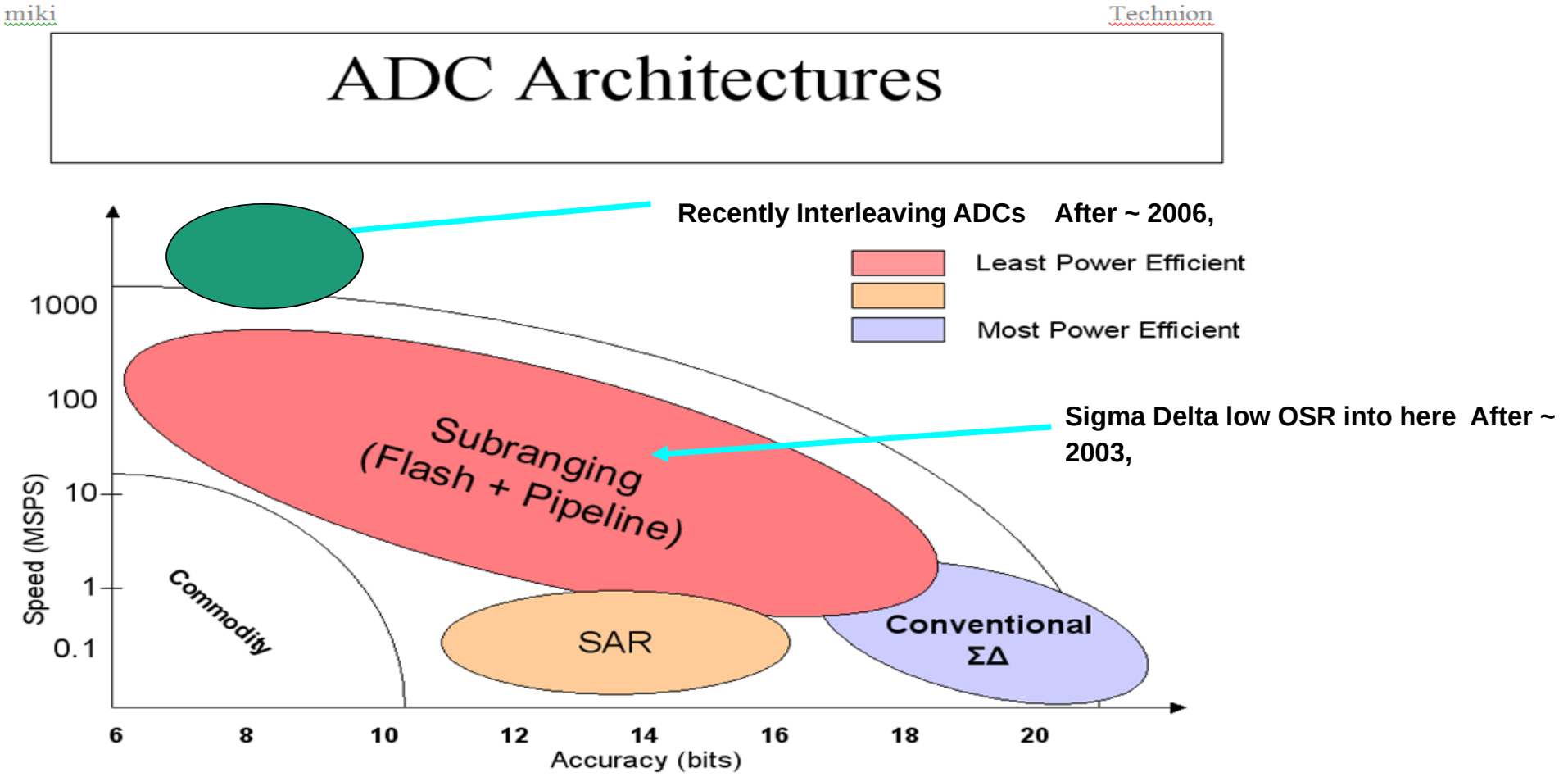


Sigma Delta

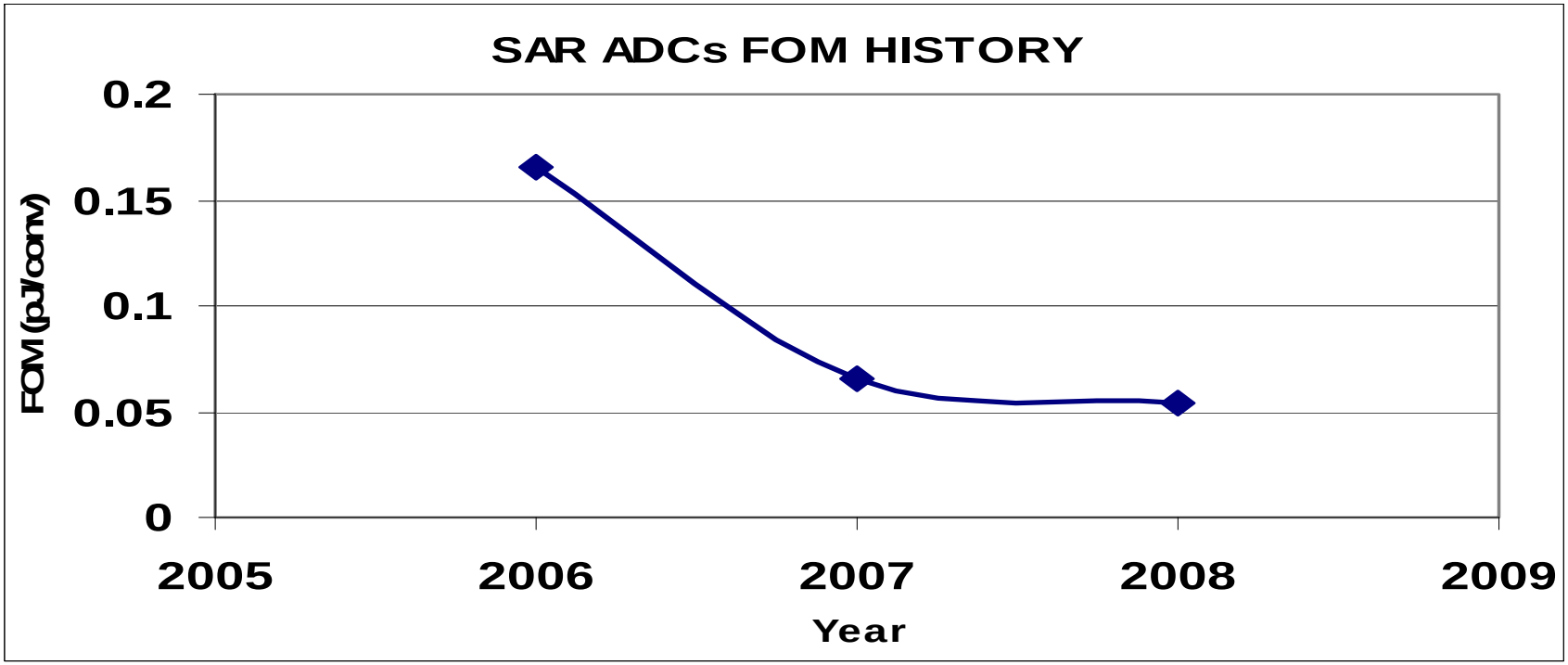


SD multi bits

Which ADC to use and why



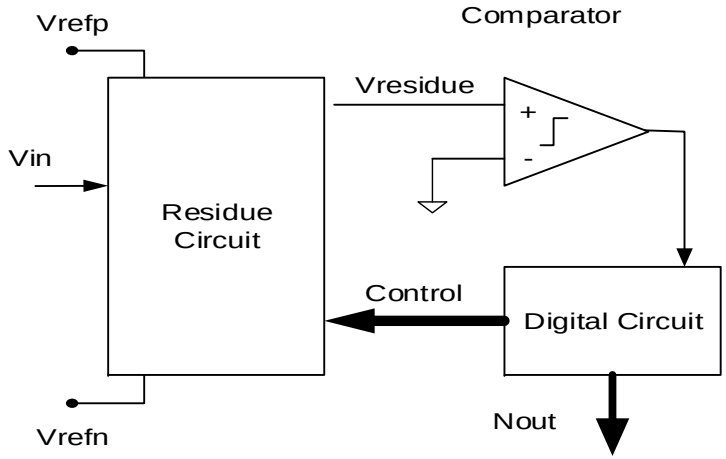
SAR ADC FOM History



2006 ➔ 12b & 100Ks/s (180nm CMOS)
2007 ➔ 9b & 50Ms/s (90nm CMOS)
2008 ➔ 9b & 40Ms/s (90nm CMOS)

$$\frac{Energy}{Decision} = \frac{Power}{SamplingRate \times 2^{Nbit}}$$

Generic ADC:



- $V_{residue}$ is a function of Vin – Vref .
- The Residue sets the source of Linearity Errors
- The Comparator set the source Speed (Offset may be a problem)

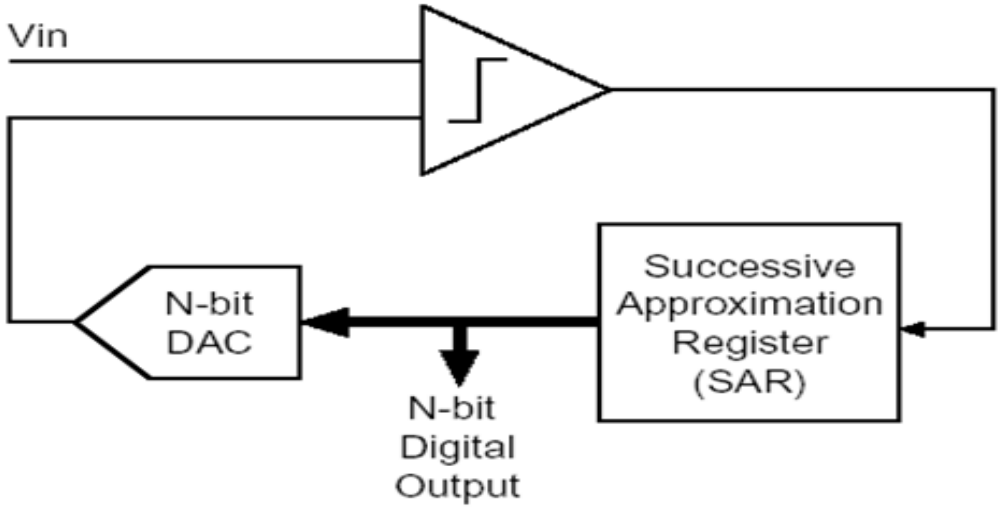
- Must check always:
  - Distortion (non linearity's) and ckt noise.
  - Speed and Power

Successive approximation ADC

If Ts is twice maximum BW

And if N =desire bits

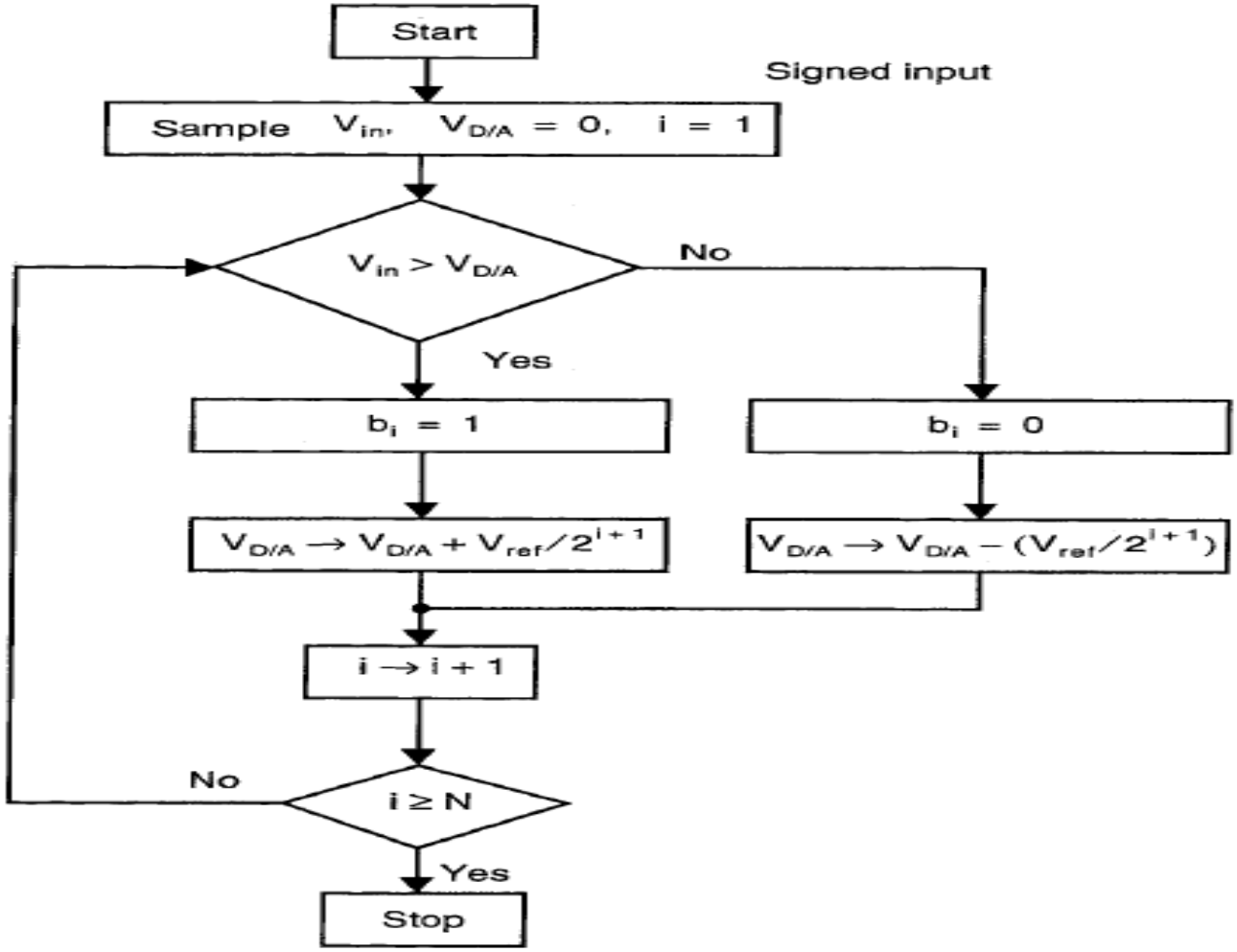
It requires minimum of p= N xTs passes to generate N bit
Output words limiting the through put
It requires N-bit accurate DAC
It requires faster settling elements



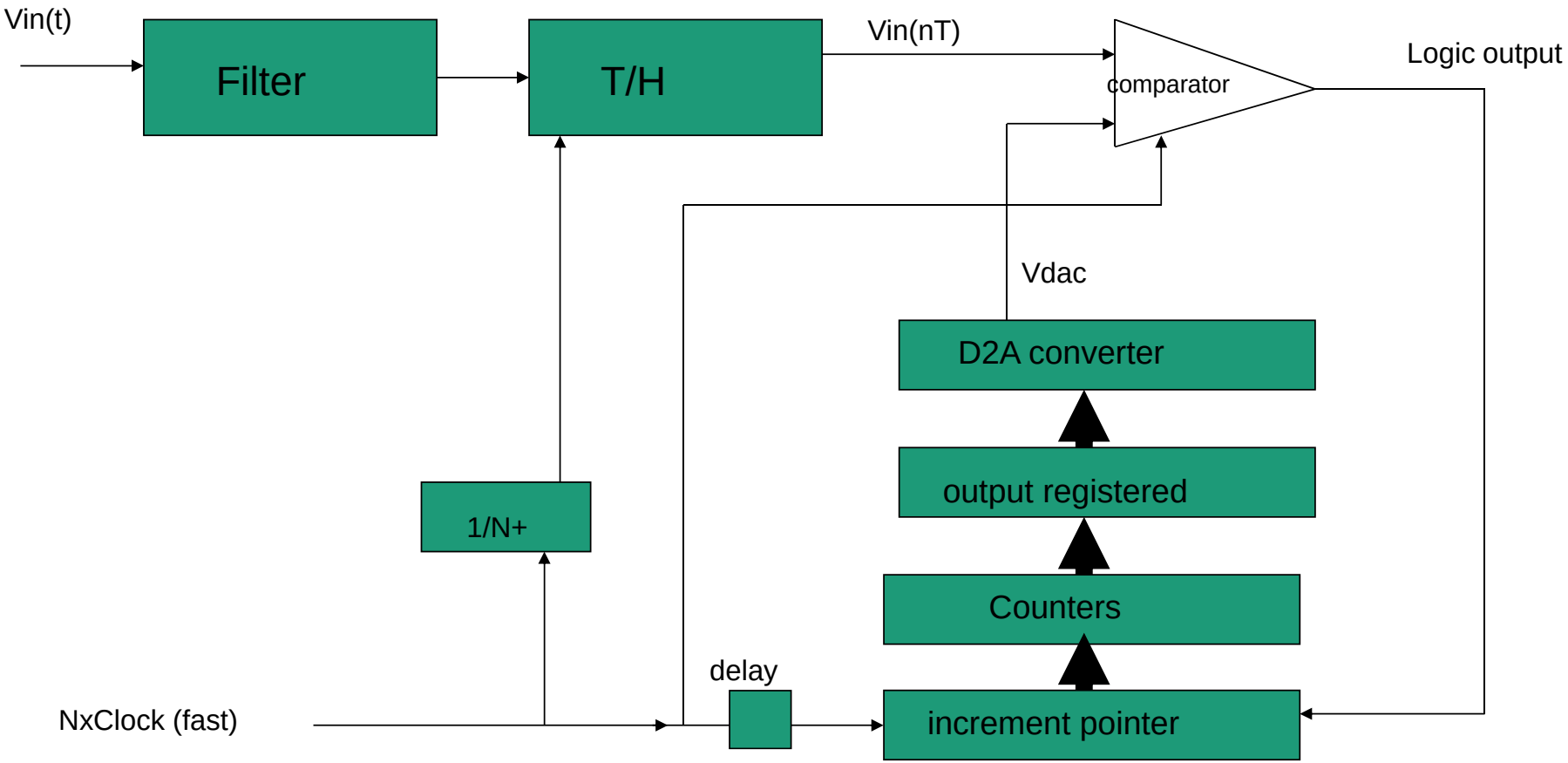
Strict timing is involved- transforming analog to digital each cycle

Comparator runs inside an open loop circuit
therefore stability and closed loop Band width is not an issue.

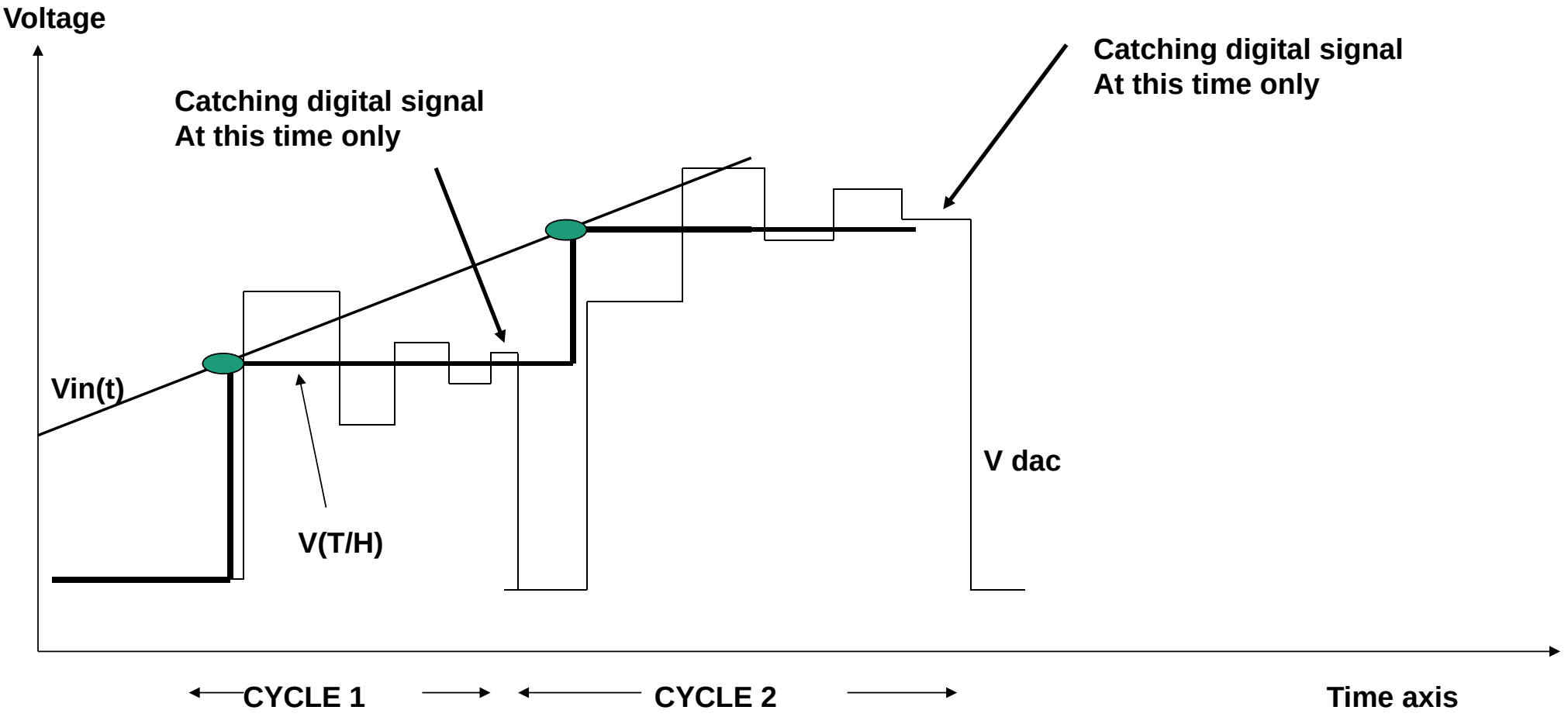
Flow chart of SAR ADC



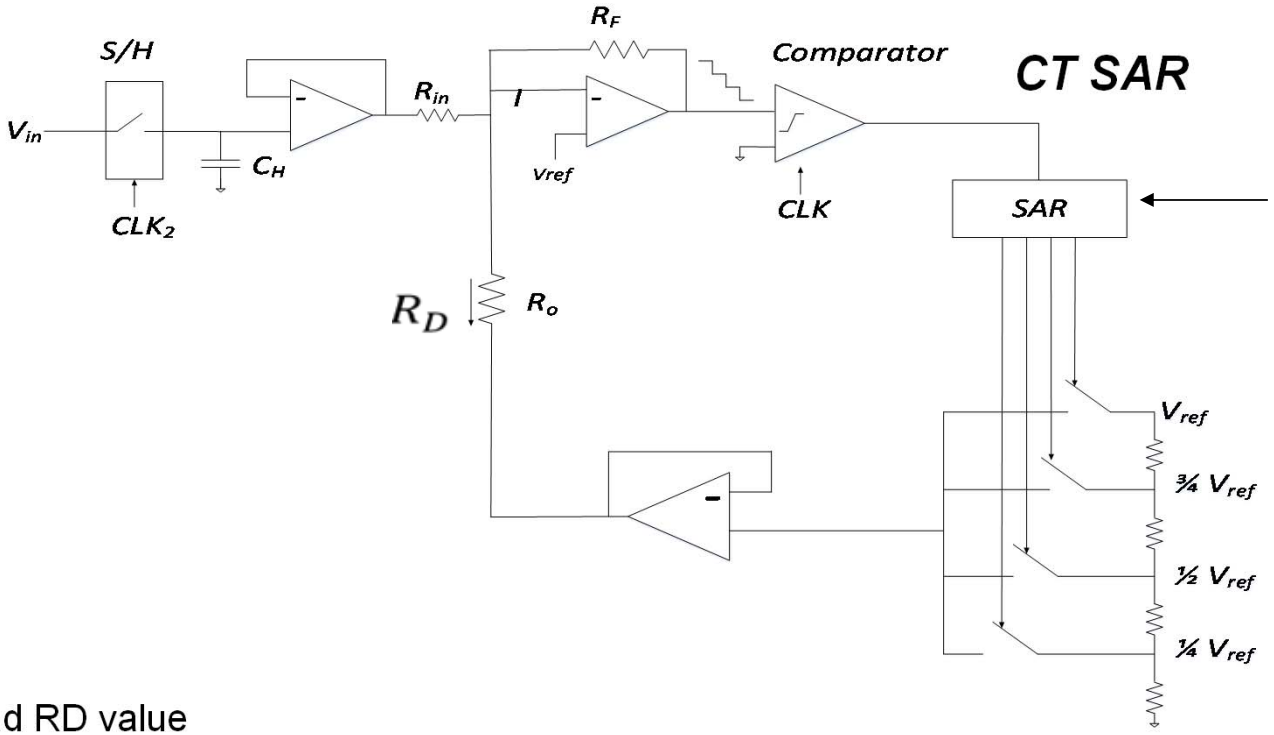
SAR ADC Details



SAR ADC – Timing



SAR design- determining full scale



= Time Continuous

Continuous,
w. sub tractor

How to find RD value

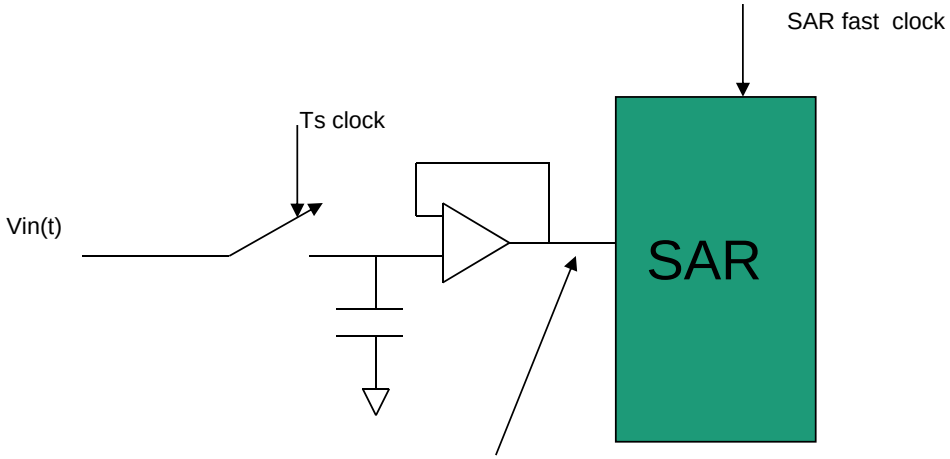
$$R_D \gg \frac{V_{in\_max}}{R_{in}} = \frac{V_{ref}}{R_D}$$

$$R_D = \left[\frac{V_{in_{F.scale}}}{V_{ref}}\right]^{-1} R_{in}$$

Time Continuous only means we use non switched C for dac

Time continuous SAR block

- 1st step sample and hold

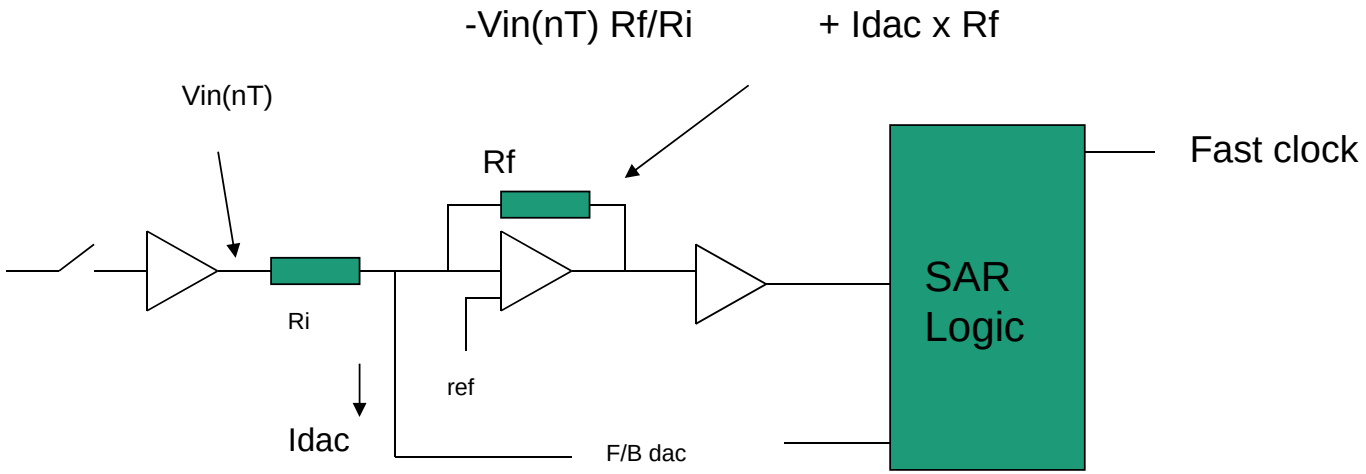


Covered already. Note the buffer

- We know the errors
- We know the speed needed
- We can proceed to build the block

SAR analog Loop

- 2nd step the sampled voltage part is being converted to I

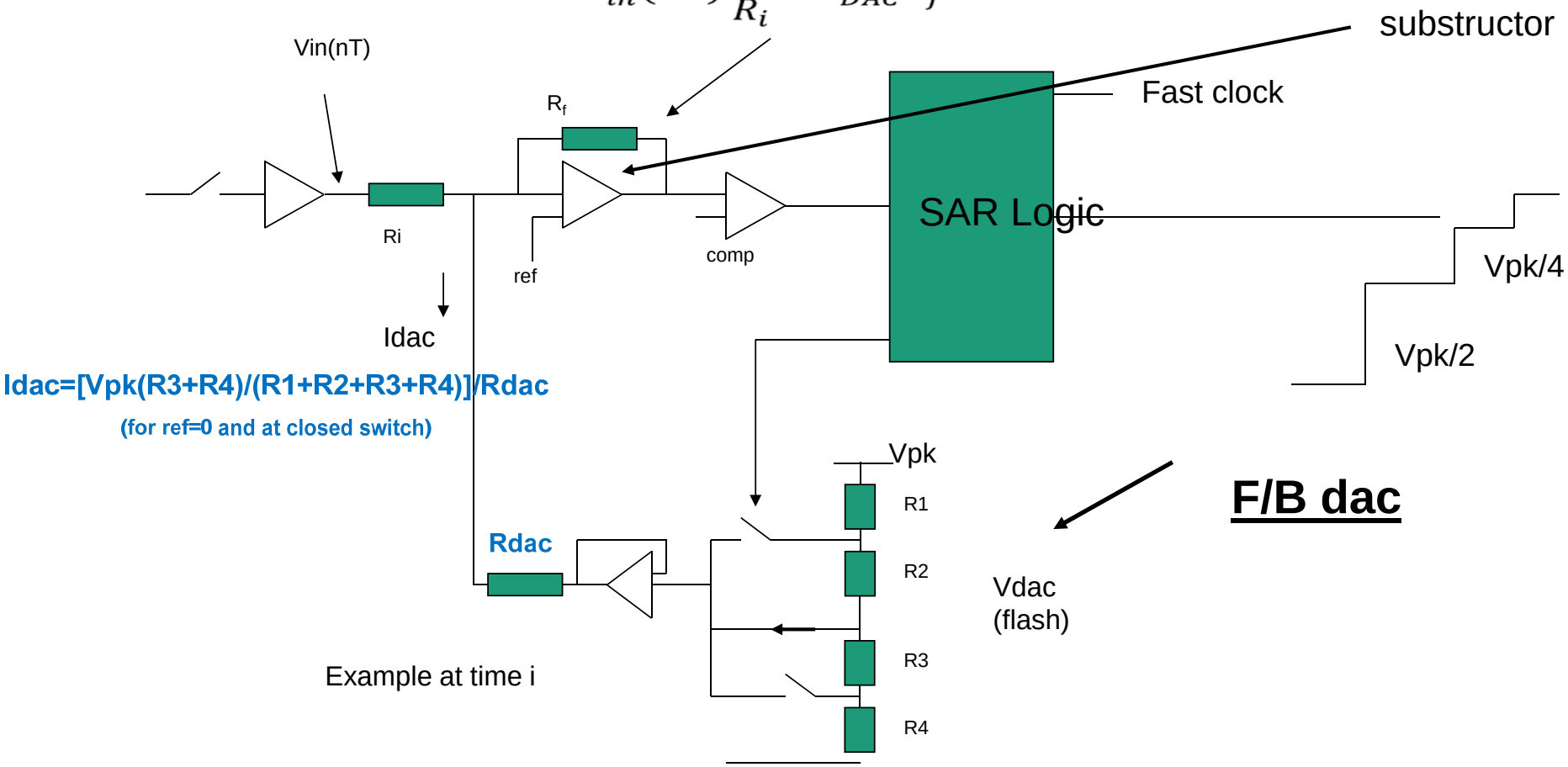


Next how to build IDAC

SAR IDAC feedback generation

- 3rd step the I_{in} and Idac is compared around the loop n times

$$-V_{in}(nT)\frac{R_f}{R_i} + I_{DAC}R_f$$

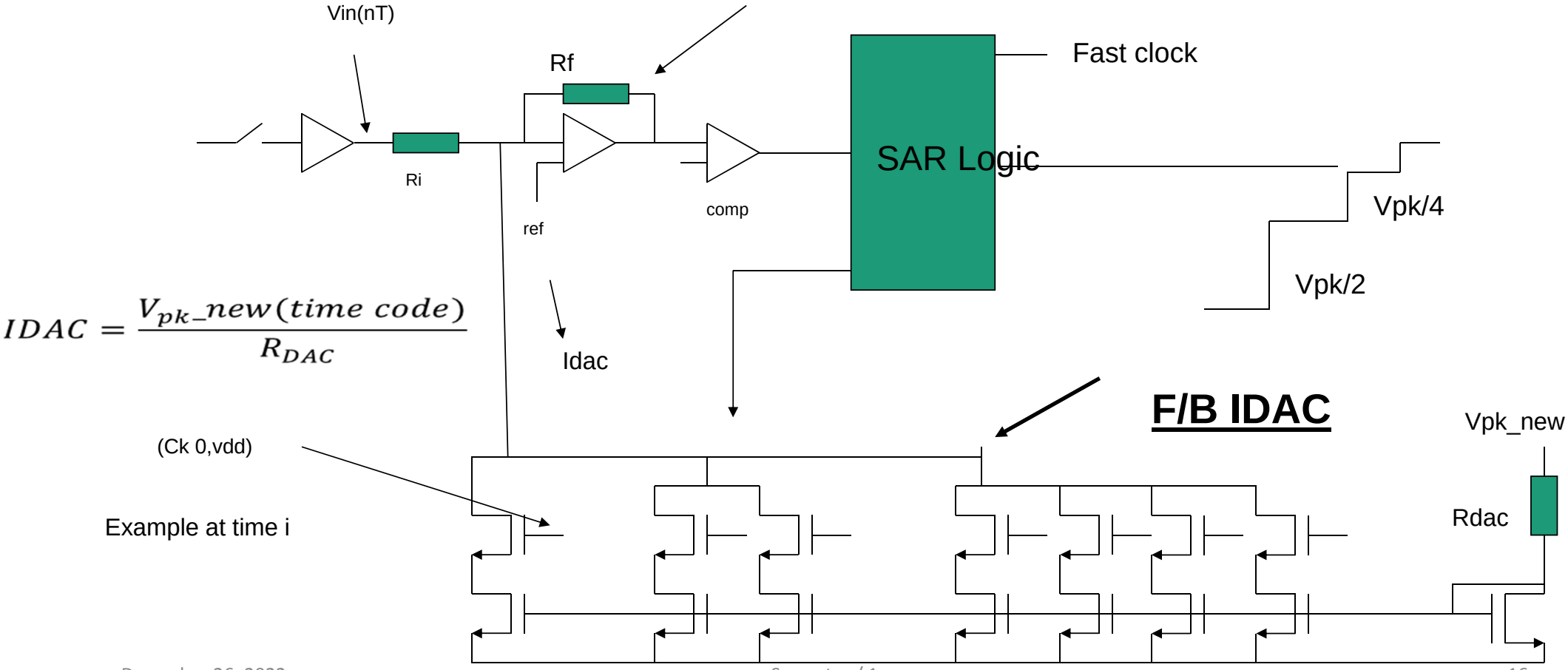


SAR DAC – use an another alternative to R-Ladder

- Go to DAC lecture pick another type ?
- We got transistors they are small
- Current is always easy to generate with transistors

SAR DAC – another DAC – speed and area Improvement

$$-V_{in}(nT)\frac{R_f}{R_i} + I_{DAC}R_f$$



$$IDAC = \frac{V_{pk\_new}(time\ code)}{R_{DAC}}$$

SAR DAC – another DAC – speed and area Improvement

- We used “not so efficient design”

- Speed issues:
  - BW amplifier,
  - Subtraction with amplifier
  - S/H - or Track and Hold.
  - Area

- Can we do it other way?
- Lead to a simpler architecture
- No amplifiers !
- **With capacitors we can easily subtract**
- Speed per cycle may be faster

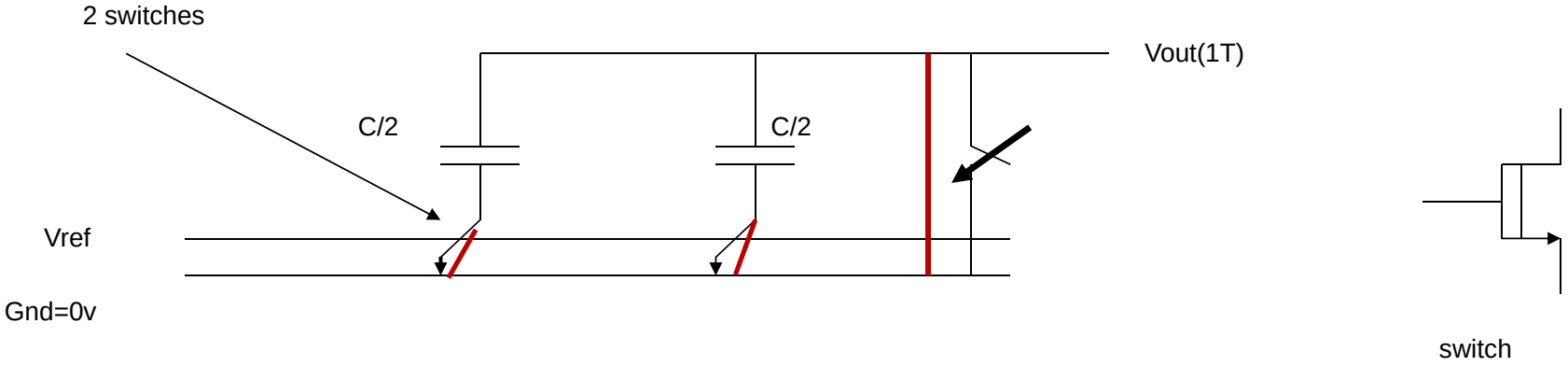
We want to generate

Vref/2….	1st clock cycle
Vref/2 +/- Vref/4..	2nd clock cycle
Vref/2 +/- Vref/4 +/-Vref/8	3rd clock cycle
Etc..., ,	

So lets use capacitor DAC to do this.

Charge Distribution SAR DAC Operation

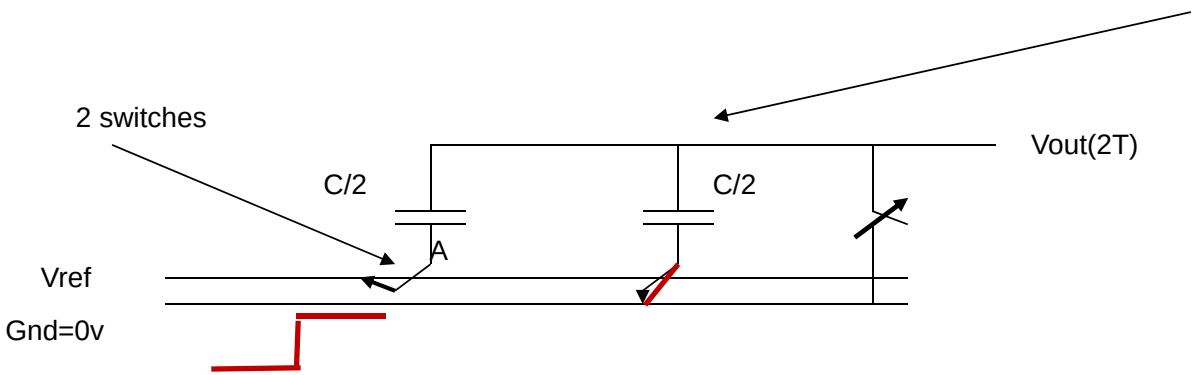
Step 1.- clock n=1, reset everything to 0 point – “wasted state” but needed because capacitors plates are held at a “value” for DC



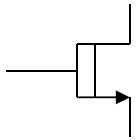
Vout = 0v all capcitors plates are shorted to 0
In reality after nRonC/2 time (Ron=1/ucox(vgs-vt)(w/l)

Generate $V_{ref}/2$ to Compare

Step 2.- clock n=2, generate vref/2 to compare with input

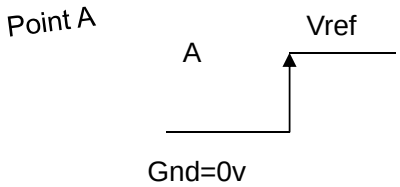


Voltage divider action



switch

Vout = 1/2vref at the end of the clock time



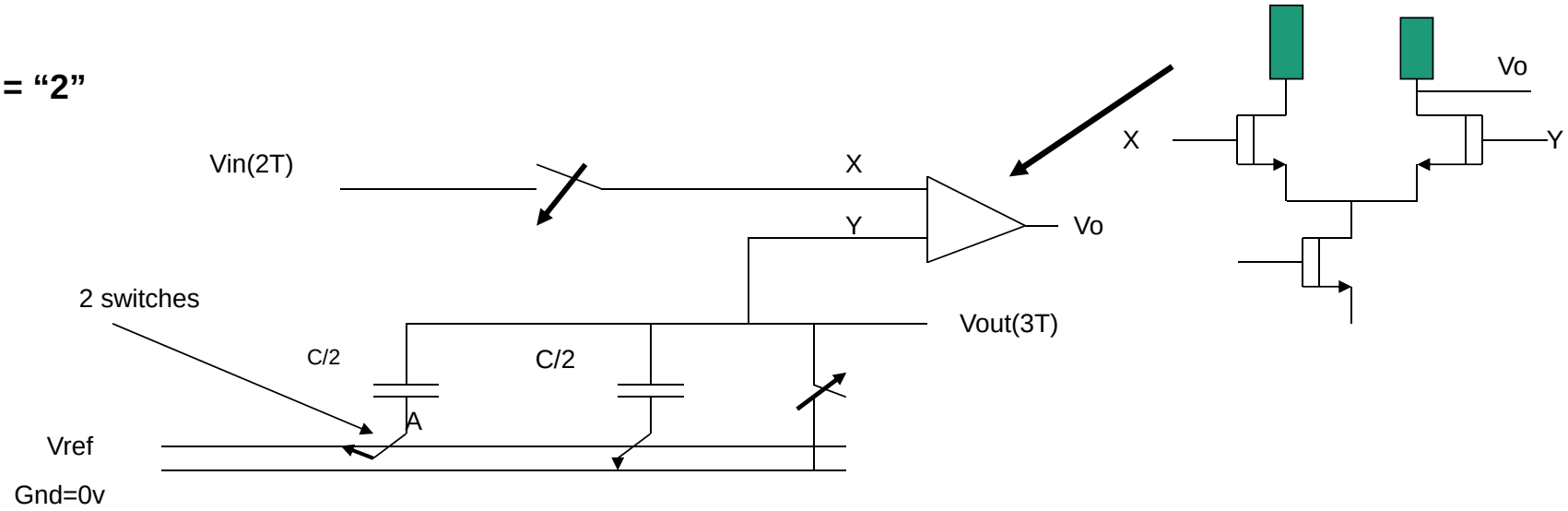
Vout(2T)= 0 + 1/S0.5C/(1/S0.5C+1/S0.5C) Vref

Vout(2T)= 1/0.5 / (1/0.5+1/0.5) Vref

Vout(2T)= Vref/2

Compare to $V_{ref}/2$ and Generate $V_{ref}/2 + V_{ref}/4$

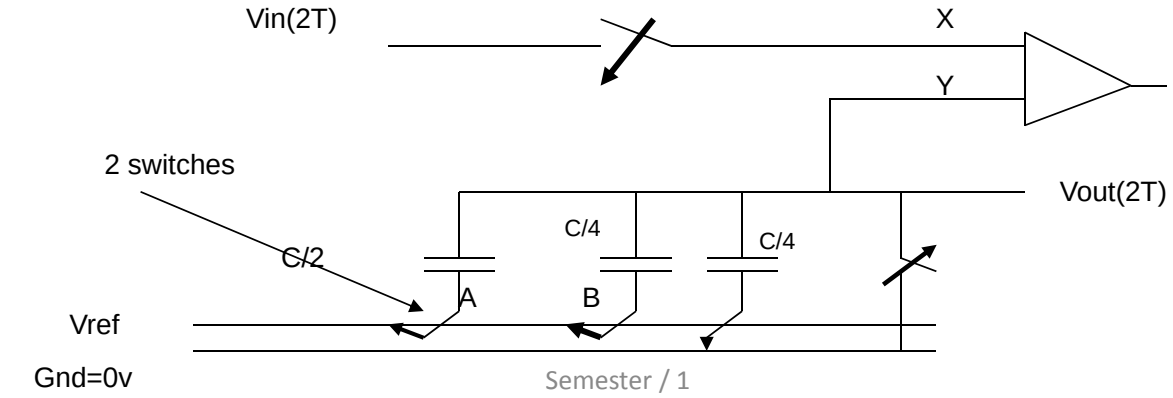
still in time = “2”



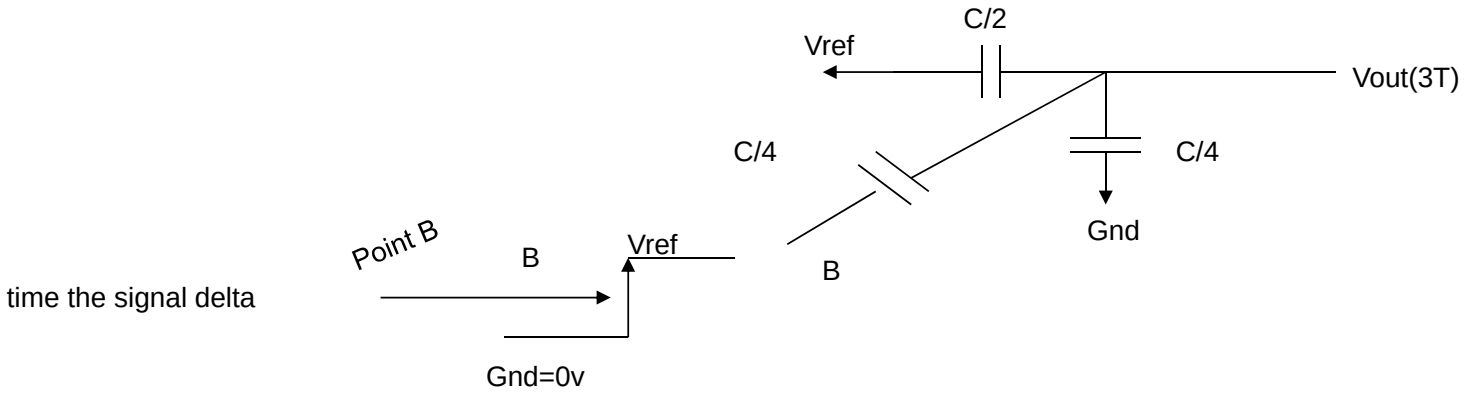
Vo =

in time = “3 ” add ¼ vref

Re arrange C to units



Generate $V_{ref}/2 + V_{ref}/4$



delVout(3T)= (0.25C / C) Vref

Del Vout(3T)=1 /4 (time the signal delta)

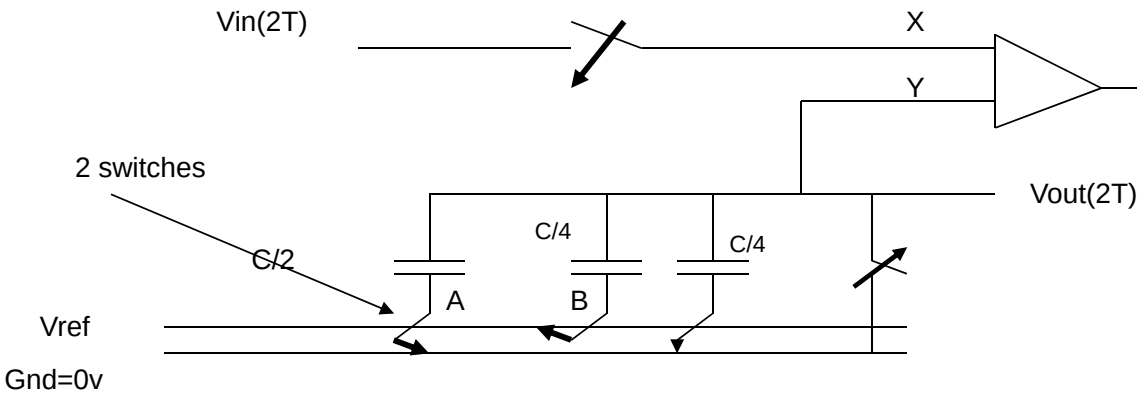
Vout(3T)= Vref(2T) + 1/4 Vref

Vout(3T)= Vref/2+Vref/4

Generate the Minus ➔ $V_{ref}/2 - V_{ref}/4$

in time = “3 ” add -¼ vref

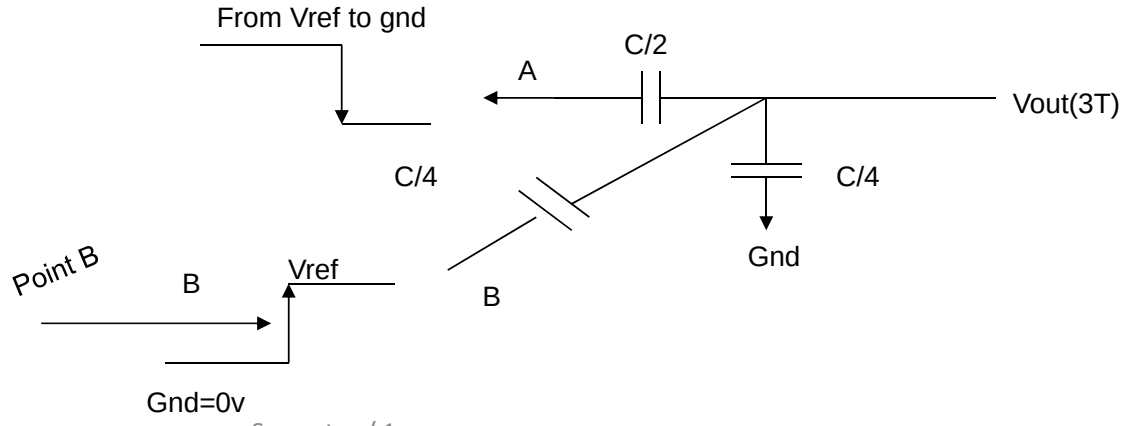
2 operations



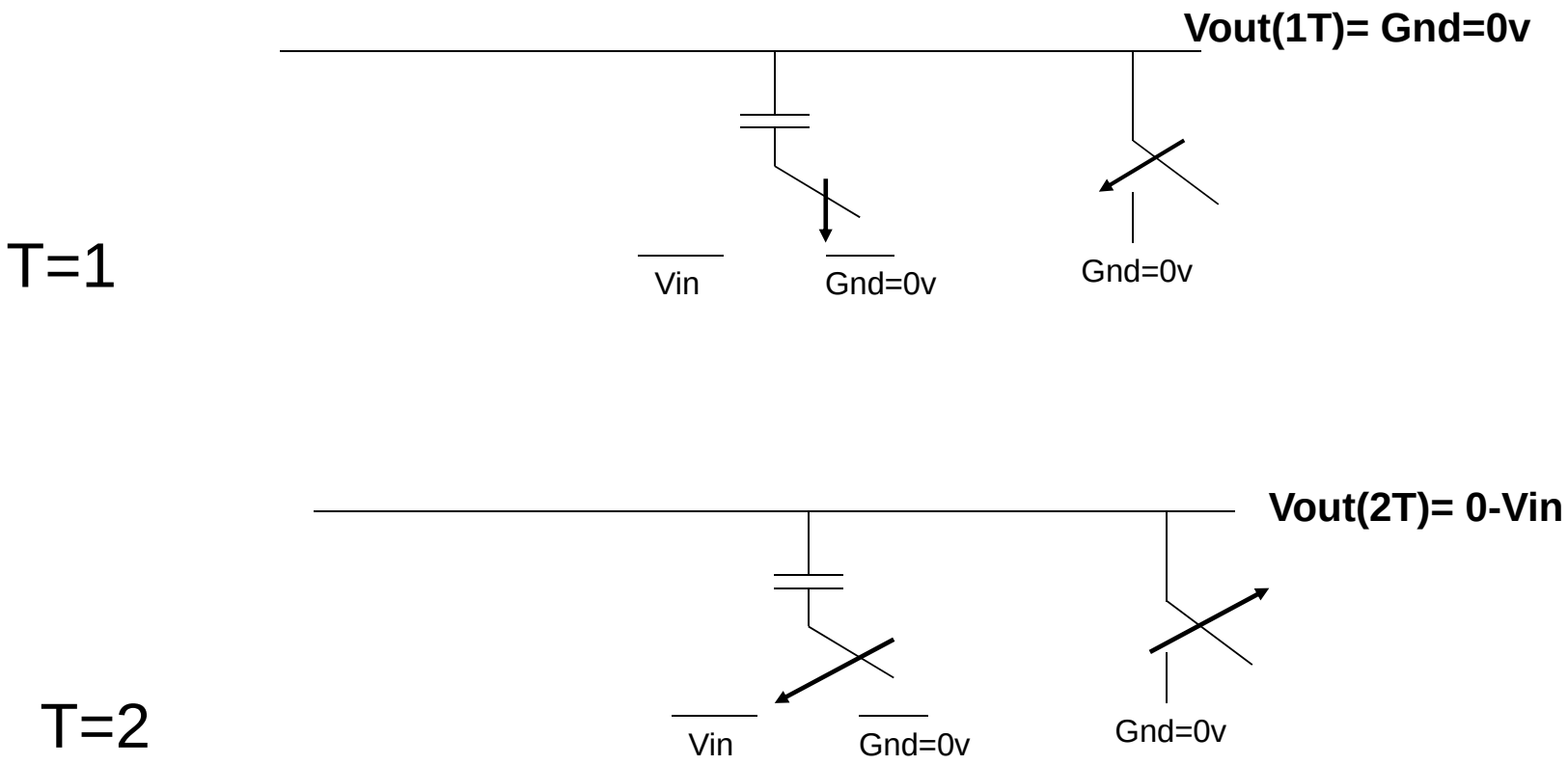
delVout(3T)= -0.5+0.25

Vout(3T)= V(2T) + -0.5+0.25

delVout(3T)= 1/4Vref

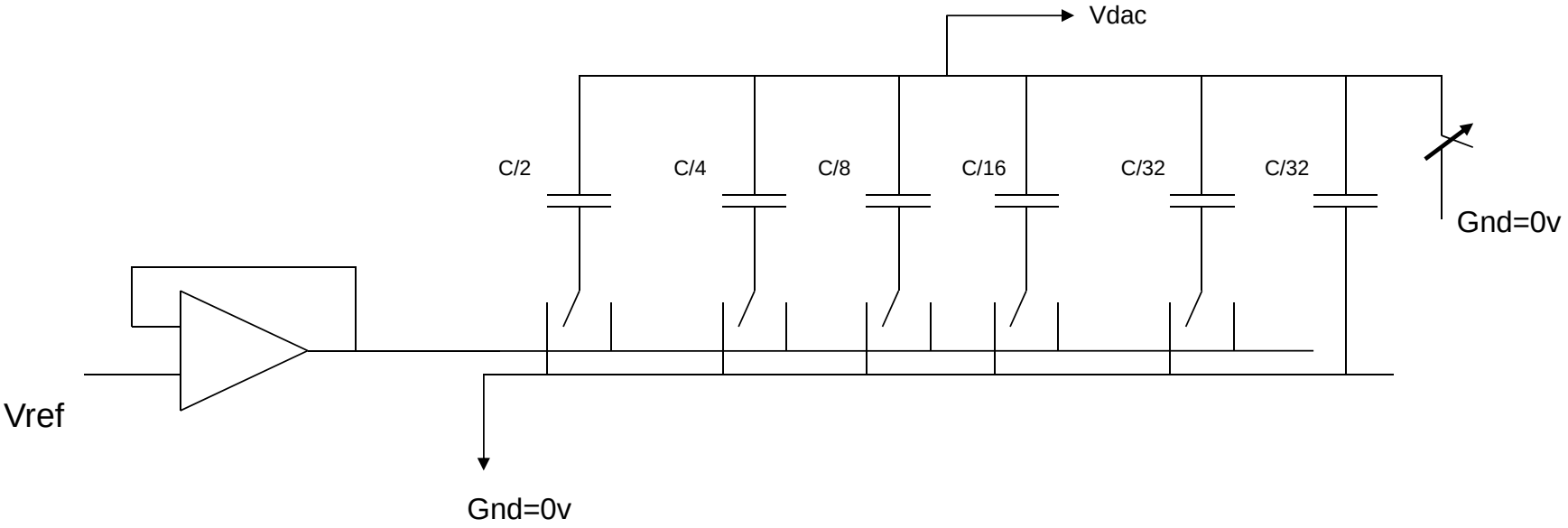


Generate the Minus of the Input as well Easily



And on.. And on.. Until the number of bits M+1

…. Let's Look at complete C-DAC SAR

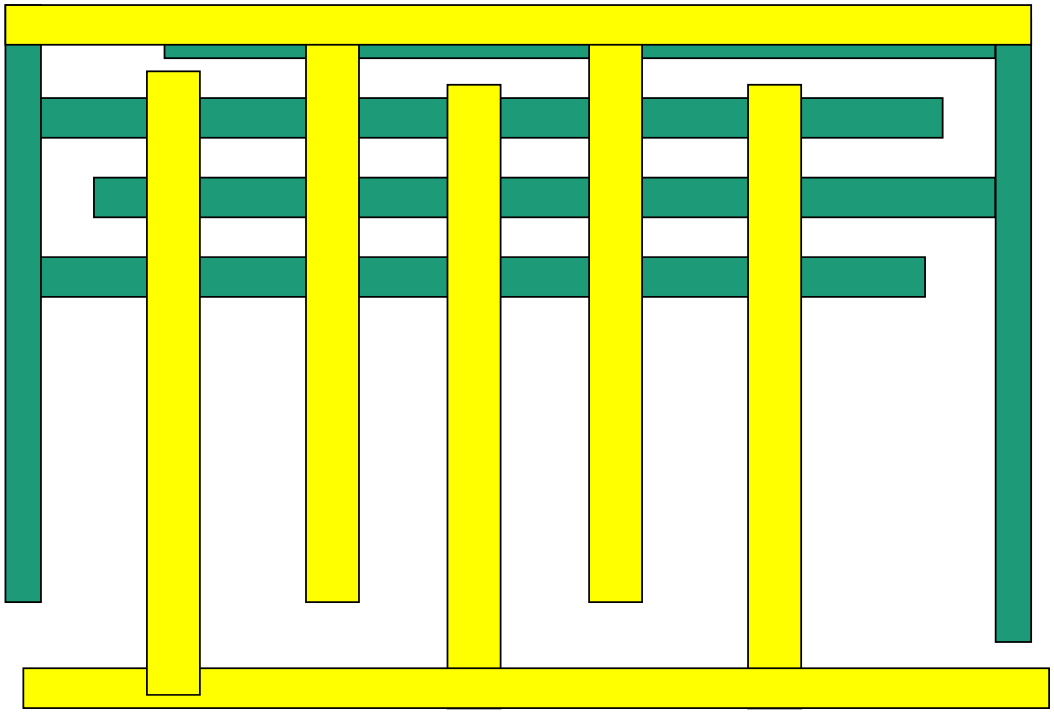


5bit dac

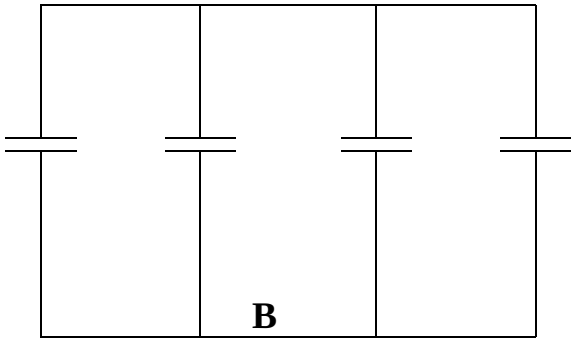
Fring. Caps to improve area density (capacitors on IC)

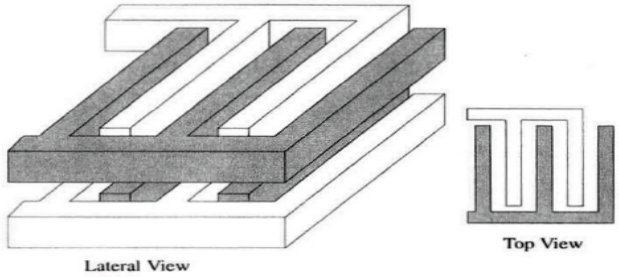
$$C = C_o WL \longrightarrow C = C_o WL + 2C_{fr}(W + L)$$

A



B

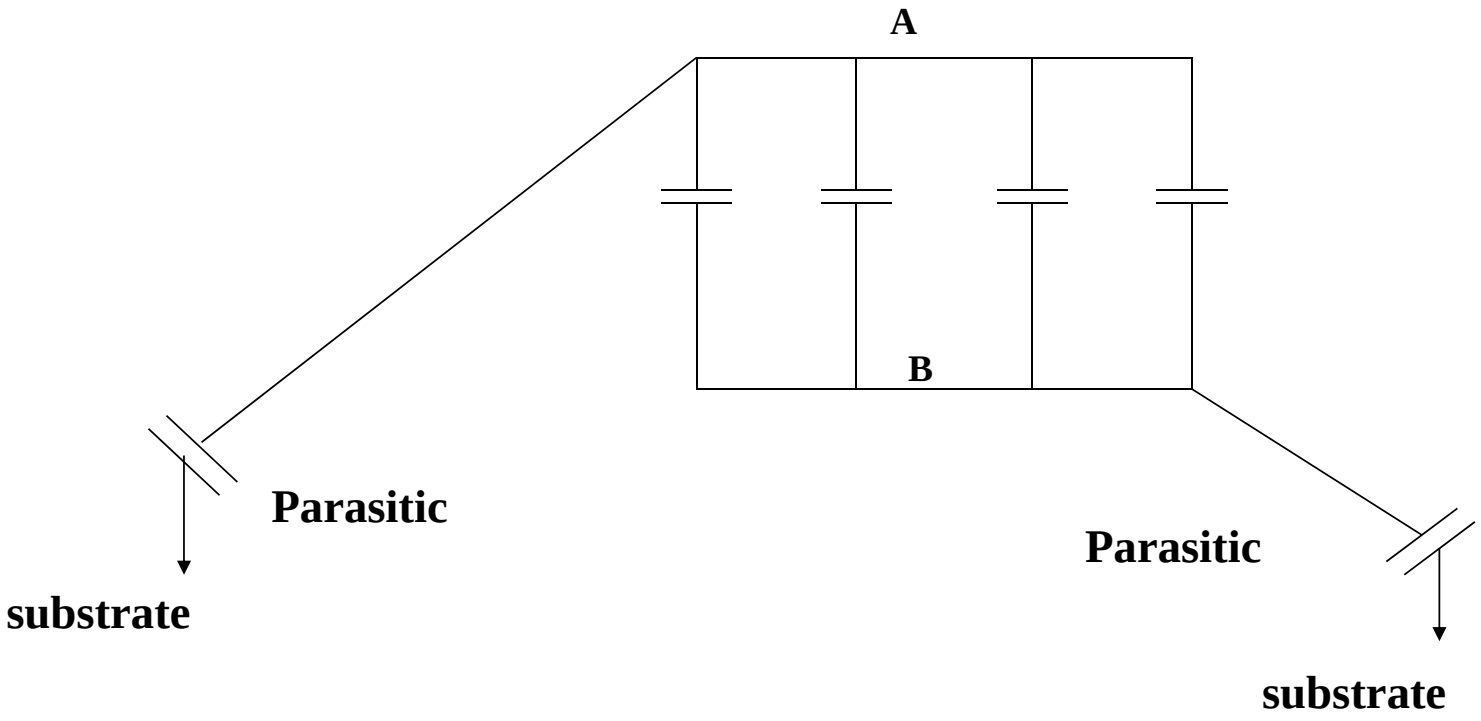




Accuracy in silicon is low ~ +/-20%
Low temperature/V dependency
Matched well. What about plate parasitic ?

Co= 1-2 ff/uu if Metal to Metal sand witched
With Fringing effect into the picture:

Fring. Capacitors-Parasitic Errors



C parasitic ~0.1-0.2C total! – how to design it out..

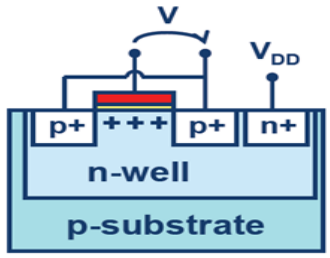
Capacitors from MOS (transistor)→triki.- watch the plates potential.

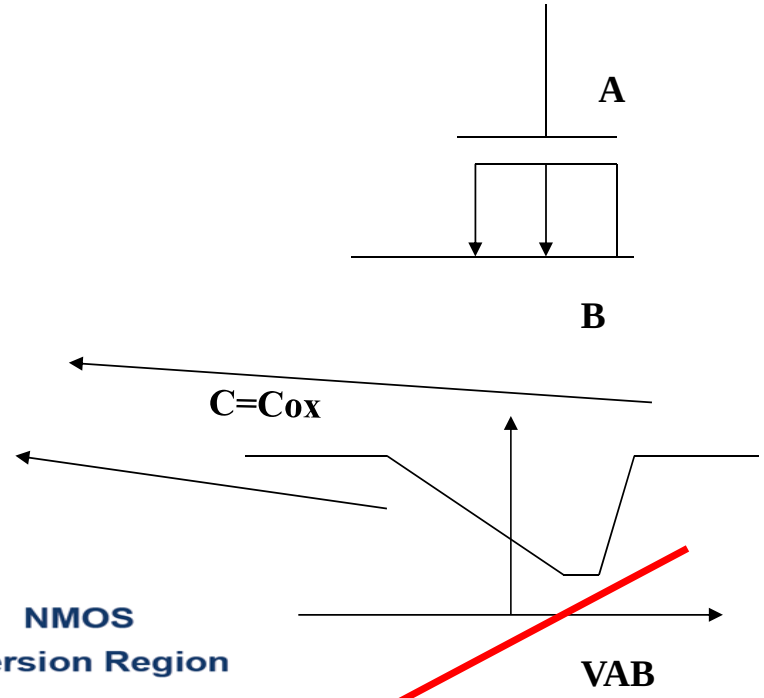
In accumulation (off)-------→ Vgs < Vt (n ch)

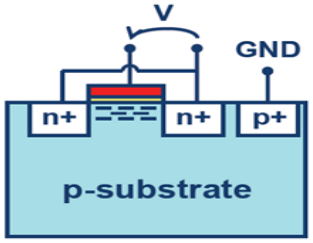
$$C = C_o WL$$

Co ~ 12ff if thin oxide is used (90nm)
Cap is to the substrate (N well probably)
In depletion (on) ---------→ Vgs >Vt

P can be in both



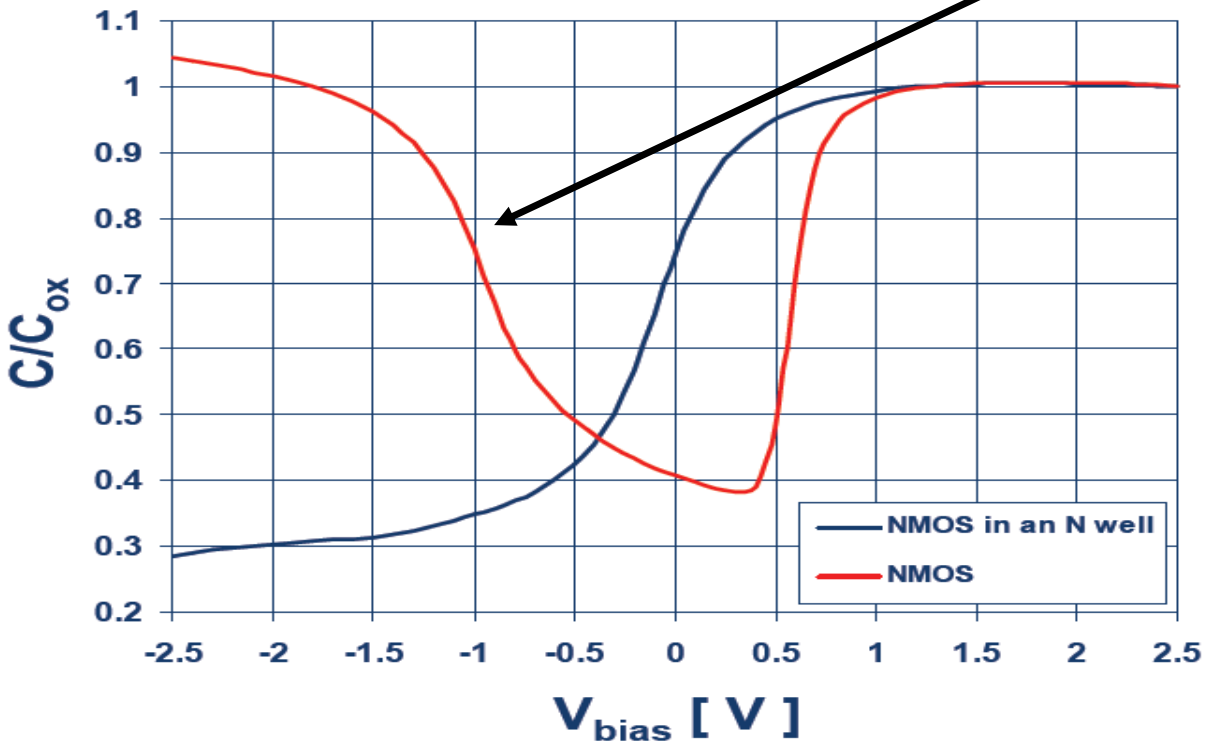


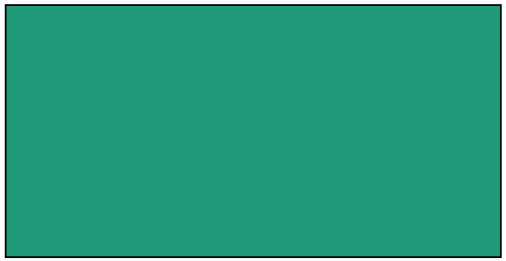


Cap is to the drain sources!
Next to Vt – C drops to ~ 0.3 its max value
It's a voltage dependent capacitor –
doesn't work good with 0 volt across it (integrator and opamp)

Silicon Transistors as Capacitors

Why not work here ? – ah.. Veractor..





The NMOS capacitor is in inversion for V > 0.

Giovanni Anelli, CERN

Errors in SAR ADCs

- Its an accurate structure
- Subtraction using caps
- Low/average power: SH, one comparator, DAC, and Logic
- 8b-200msps is possible
- But: Need Accuracy in the DAC.
- Comparator offset < ~ 0.5 LSB – Easily calibrated

ACCURACY : FUNCTION OF DAC (CAPACITORS) MATCHING

Matching

$$C \approx \varepsilon \frac{WL}{t} \longrightarrow \left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

- Once again can correlate to area with good accuracy
- How is it given

1. A_deltaC/C is based on sigma of (deltaC / C) vs. 1/sqrt(WL)
typ. number 2fF/micron square

To get to the best matched number you need to :

- Use identical geometries
- Use large unity capacitance (minimize fringing)
- Use common centroid arrangement
- Use dummy capacitors
- Use shielding
- Account for the connections' contribution
- Don't run connections over capacitor
- Place capacitor in low stress areas
- Place capacitors far from power devices

An Example

Find the LSB capacitor size (and total capacitors)
for a 12b SAR ADC Given that 10ff unit match to 0.8%. (to 1 sigma)

$$C_{unit} = 10fF \qquad \left(\frac{\Delta C}{C}\right)_{unit} = 0.8\%$$

$$\Delta_{noise} = \sqrt{\frac{\Delta^2}{12} + [Distortions]^2 + \frac{KT}{C_T}}$$

$1pF \sim 64E^{-6}\,V/\sqrt{Hz}$

$$Let\ give\ [Distortions] \gg \frac{1}{3} LSB\ wight$$

$$\left[\frac{\Delta C}{C}\right]_{Full\ Scale} = \frac{1}{3}\left[\frac{1}{2^n - 1}\right] = 0.0081\%$$

$$\left[\frac{\Delta C}{C}\right]_{LSB} = [0.0081]\sqrt{2^n - 1} = 0.518\%$$

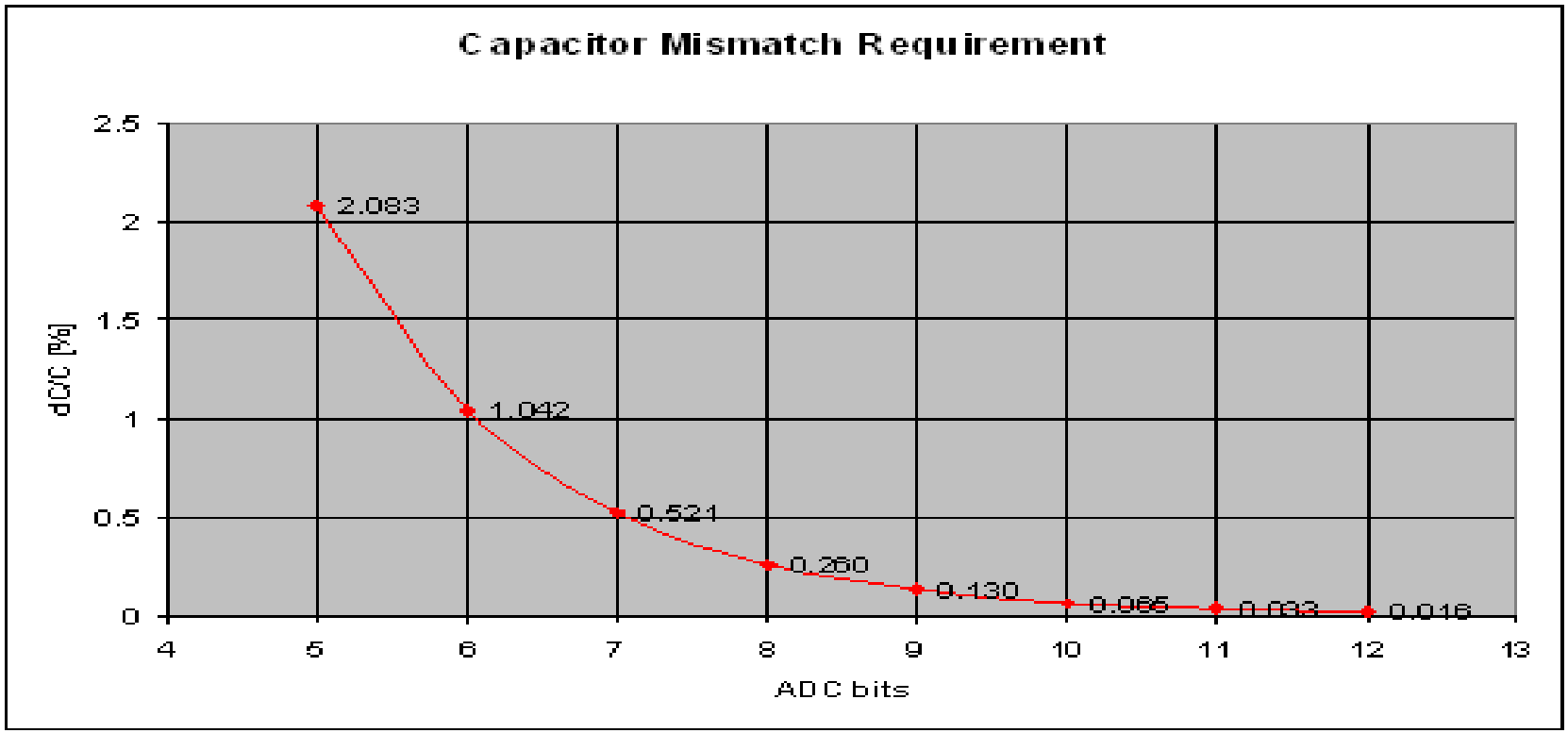
$$C_{LSB} = [C_{unit}]\left[\frac{0.8}{0.518}\right]^2 = 23.85fF$$

$$C_{total} = 97.67pF$$

$$Not\ to\ influency\ the\ converter$$

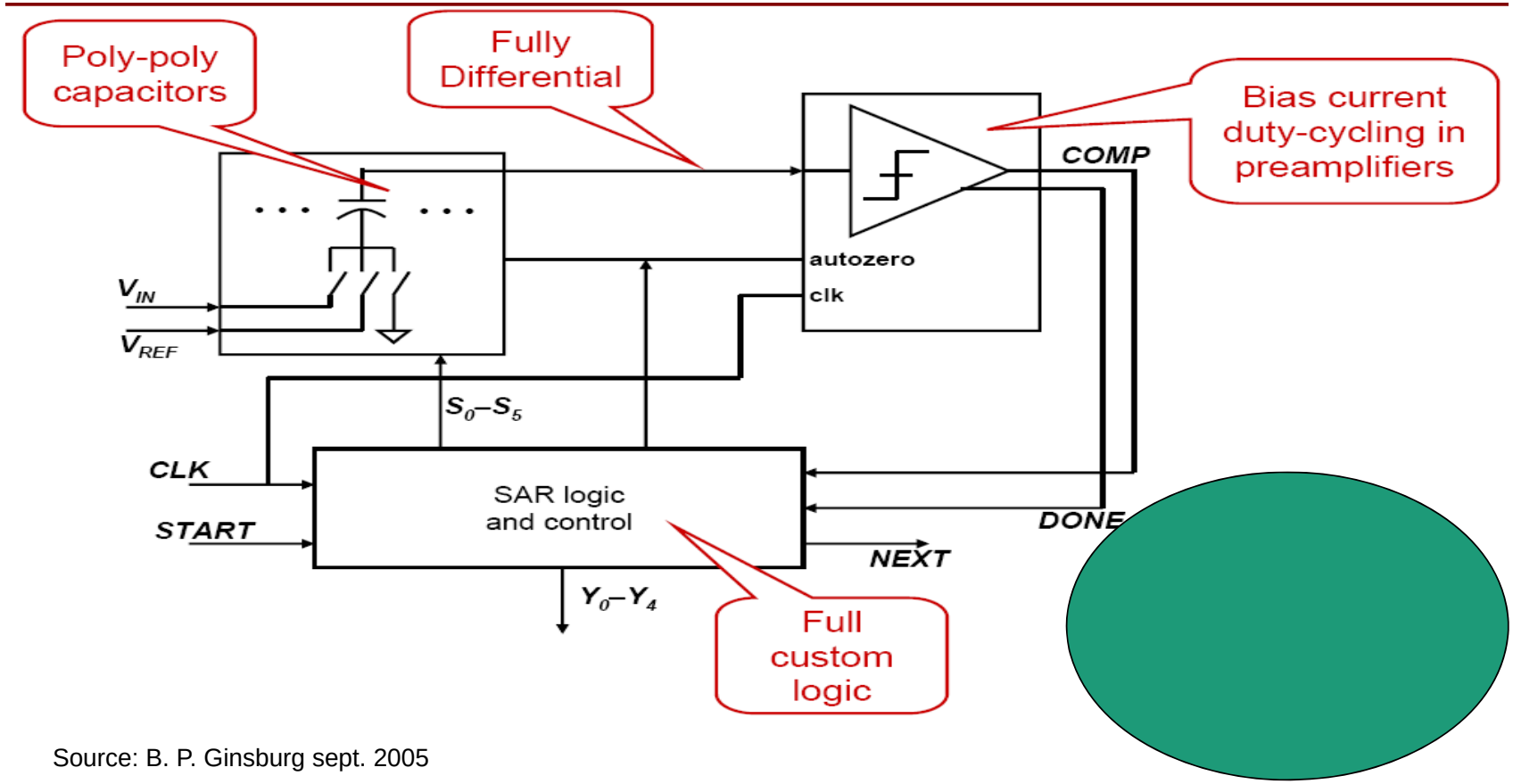
$$C_{LSB} = [C_{unit}]\frac{\left[\left(\frac{\Delta C}{C}\right)_{Full\ scale}\sqrt{2^n - 1}\right]^2}{\left[\left(\frac{\Delta C}{C}\right)_{unit}\right]^2}$$

Example of Matching Requirement on F. Scale (MSBs)



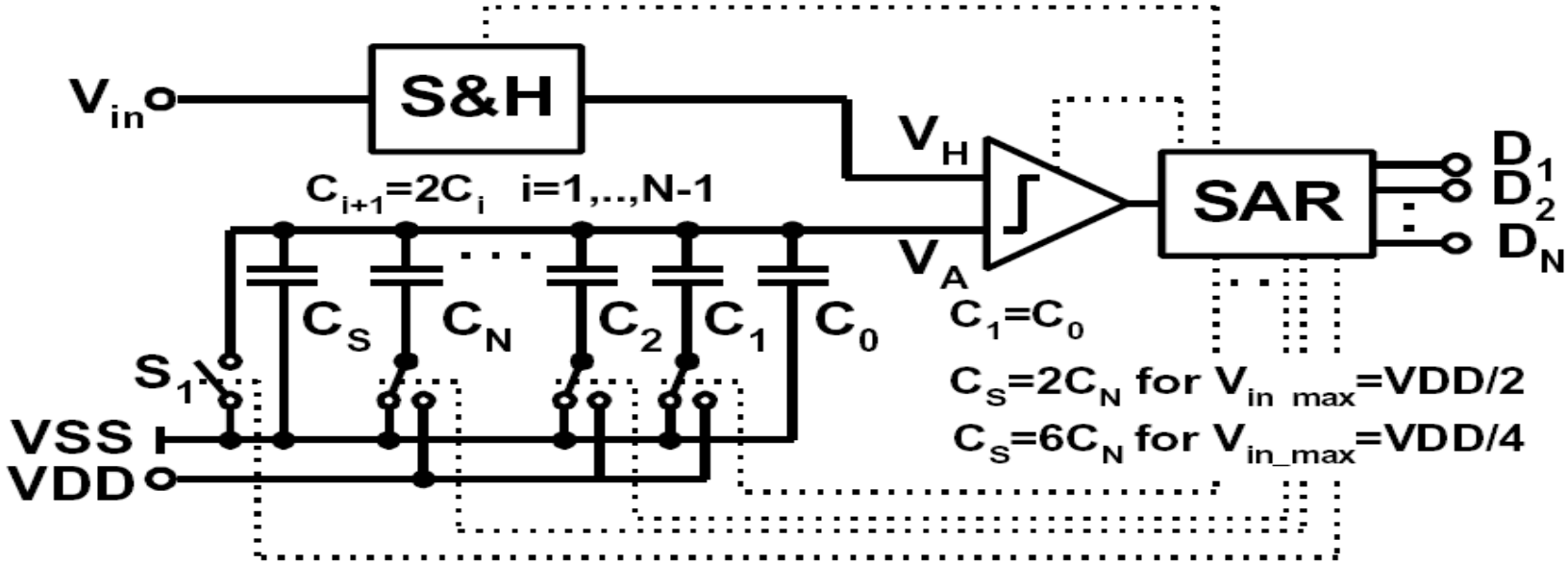
2 to the n x 2/3
(2/3 only as example not to give all the error to the linearity)

How to Build One – What is Needed to Look for



Source: B. P. Ginsburg sept. 2005

Design Examples

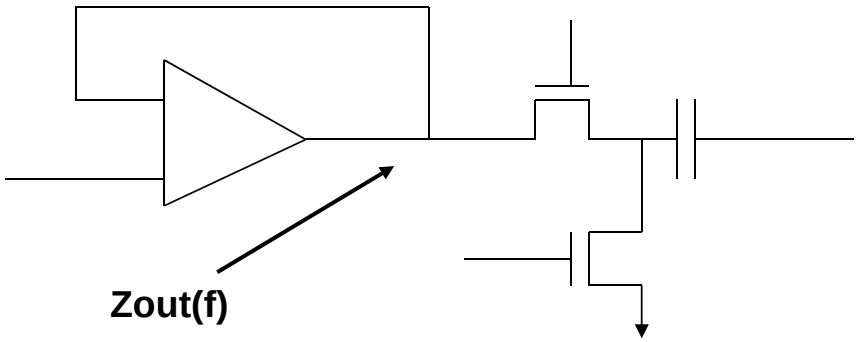


Word on the References

References issues:

REFERENCE HOLDING BREF IS HARD TO DO:
During switching phase references
has to settle every clock (fast) They are op amp
driven therefore make the design almost as op-amp based

Also the comparator must settle every cycle. (faster)



Summary – C or R DAC

- Most time absolute value can move =+/-15% to +/-20% and does not significantly matter but ratio's do
- However, the bigger the area the better the matching
- Typical values 30ff can match 3-sigma to better ~ 0.5%
- Matching is area dependent generally by the root of (W x L)
- In SAR there is contradiction large is good for matching however speed is degraded a lot R switch x C and its multiplied N bit for a complete cycle.

Power / Analog Components

- Without amplifiers power is set by S/H, References, 1 comparator, and digital blocks+clocks
- Generally for lower number of bits – logic may be significant
- Area. For many bits analog set the power waist.
- Logic running multiple times for each conversion and capacitor size (forcing a large drive current)
- Power waist : S/H + Comparator + Reference + Switching/logic

Good:

- **Lowest possible power- FOM**
- **Fewer analog elements,**
- **T/H or S/H drive low capacitance**

SAR- Key Points

- The Feed Back ADC (SAR) offers significant hardware savings compared to flash ADCs because the coarse Quantizer (comparator) resolution m can be much smaller then the converter resolution. N

- However, its suffer from drawbacks making it not suitable for many applications because:
  - It requires p= N/m passes to generate N bit output words limiting the through put
  - It requires N; bit accurate DAC
  - It requires faster settling elements
  - but No need amplifiers !

- **So, if speed is a problem should we combine SARs in time ?– tiem interleaved 50gsps nice to do..**

End Lecture 7