Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

Instructor: Dr. Miki Moyal

TEL AVIV UNIVERSITY אוניברסיטת תל אביב

Lectures
http://www.gigalogchip.com/lectures.html

Lecture 06

ADC Types

FLASH ADC

Quick summary up to date

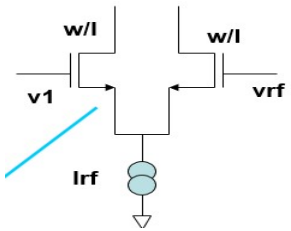
Covered Transistor Basics sampling……

Covered Transistor/passives noises……

Covered Quantization Noise of ADC/DAC

Covered Timing Jitter/inaccuracy……..

Covered Mismatch of elements……..



$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}}$$

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{ds}}$$

$$\Delta I_{ds} = g_m \cdot \Delta V_{gs}$$

$$f_s X(f) + f_s X(f - f_s) + f_s X(f - 2f_s) + f_s X(f - 3f_s) + \cdots$$
$$f_s X(f + f_s) + f_s X(f + 2f_s) + f_s X(f + 3f_s) + \cdots$$

Quantization energy –

$$\frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{+V_{LSB}/2} V_{err}^2 (V_{in})\, dV_{in} = \frac{V_{LSB}^2}{12}$$

Thermal Noise

$$I_{noise}^2 = \left(\frac{2}{3}\right) 4 \cdot k \cdot T \cdot \gamma \cdot g_m \cdot \Delta f$$

$$V_{in\_noise}^2 = \frac{\left(\frac{2}{3}\right) 4 \cdot k \cdot T \cdot \gamma}{g_m} \Delta f$$

==========
==========

So Now lets have more fun: look at real blocks work.. ADCs/DACs, etc..
And their relations to transistor ICs.

==========
==========

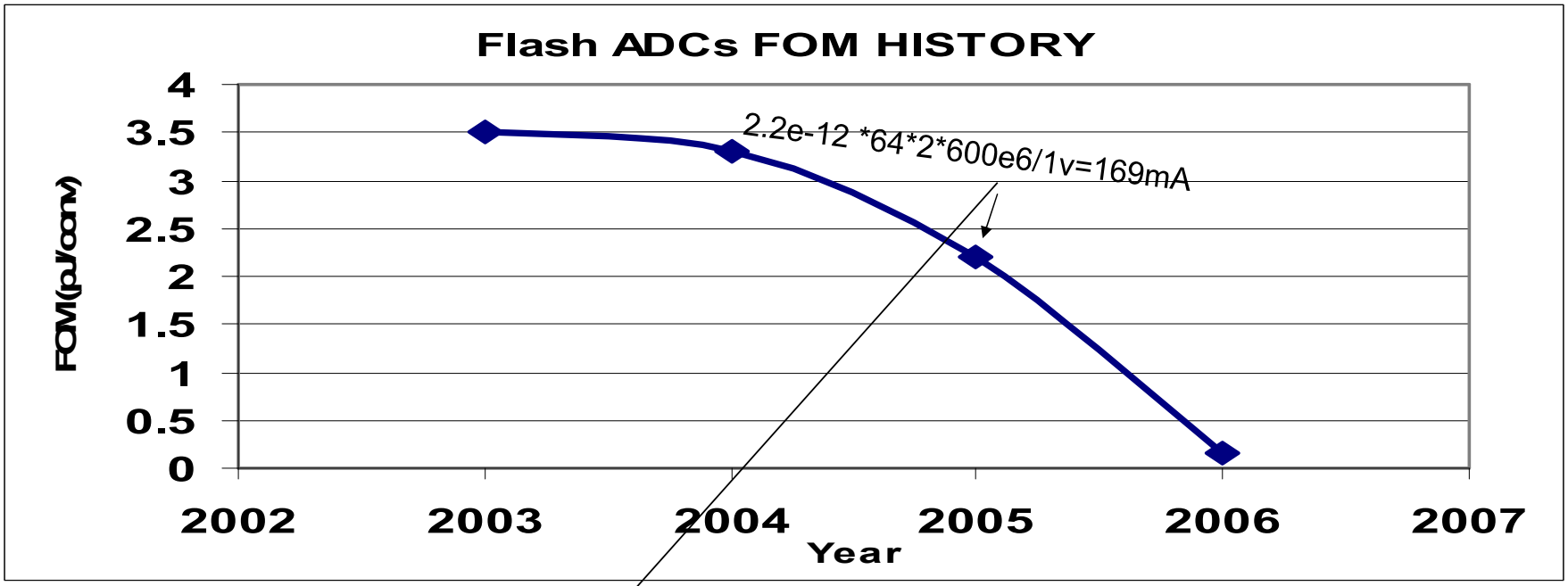
Agenda

ADC Architectures – on going lectures

Flash ADCs

Flash – Design and Error Sources

Flash ADC FoM History



2003 ➔ 6b & 2Gs/s (180nm CMOS)
2004 ➔ 6b & 300Ms/s (0.25um CMOS)
2005 ➔ 6b & 1.2Gs/s (130nm CMOS)
2006 ➔ 4b & 1.25Gs/s (90nm CMOS)

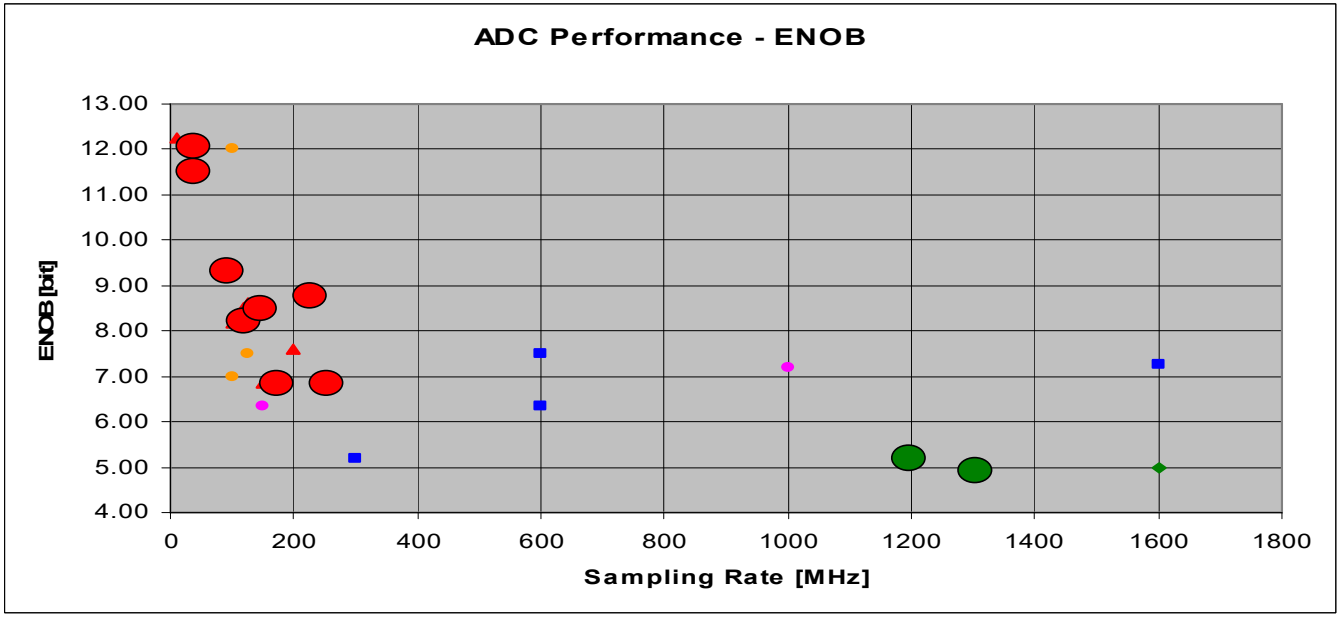
$$FOM = \frac{P}{2^{ENOB} \times 2 \times ERBW}$$

- **Flash ADC – This lecture.**
- **Two Steps (Sub Ranging) ADC – if time allow.**

Other ADC's

- SAR ADC
- Pipelined ADC
- Over Sampling ADC
- Folding/Interpolating ADC
- Algorithmic ADC
- Combined Parallel ADC

The ENOB: General trends



Green – Flash
Red – Pipe Line
Blue – Folding
Pink – Open Loop Pipe line
Sigma delta ADC ?
(0-200MHz, 9-14bit)

- SNDR (AC) Measured Converter S/N
- N Quantization
- D Distortions

Basic split

- Architecture suited for very *high input frequency* (less bits)
  - Flash ADC
  - Folding ADC
  - Open Loop Pipe Line – can still have many bits
  - Time interleaved ADC

- Architecture for *high precision* (more bits)
  - Flash Sub Ranging ADC
  - SAR ADC
  - Sigma Delta ADC
  - Pipeline ADC
  - Time interleaved ADC

Basic Split

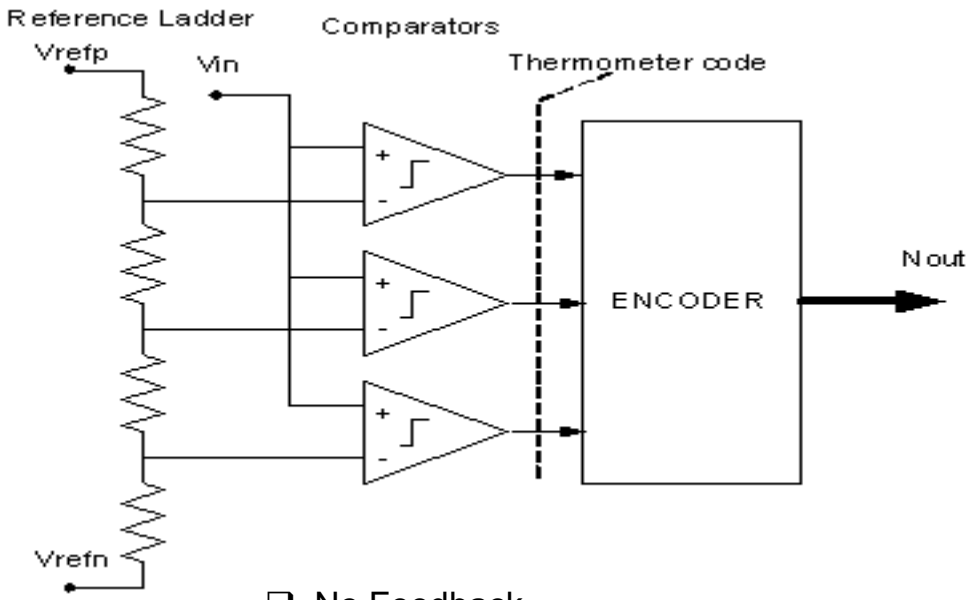
- Architecture suited for very *high input frequency* (less bits)
  - Flash ADC
  - Folding ADC
  - Open Loop Pipe Line – can still have many bits
  - Time interleaved ADC

- Architecture for *high precision* (more bits)
  - Flash Sub Ranging ADC
  - SAR ADC
  - Sigma Delta ADC
  - Pipeline ADC
  - Time interleaved ADC

Rest of the slides will address only the FLASH ADC (and its types)

Basic flash ADC

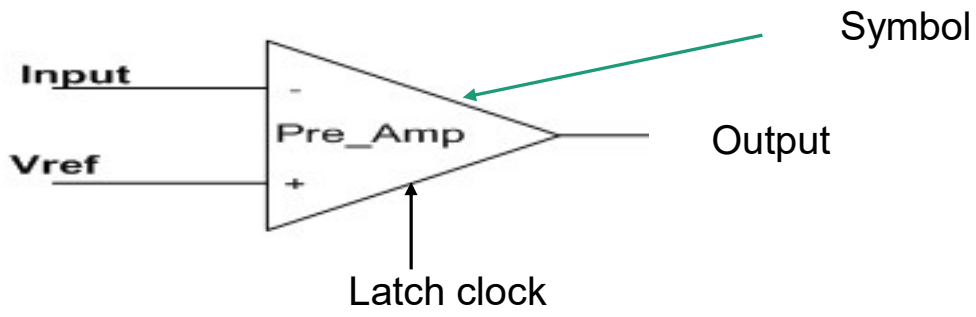
"Classic Mixed Signal"

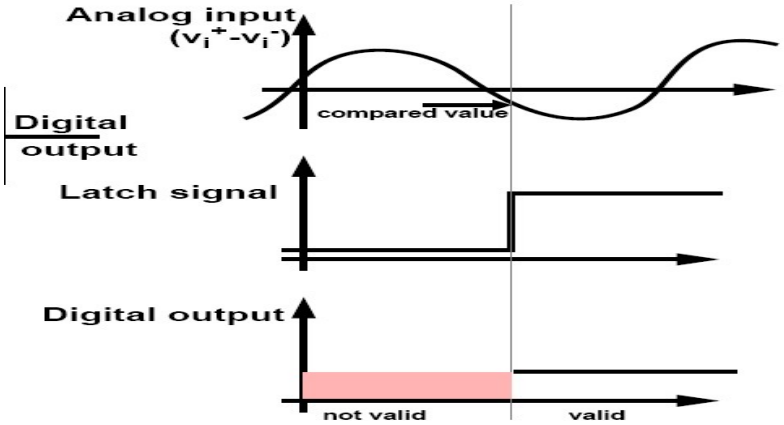


- No Feedback
- No Amplifiers all in "Open Loop"
- Monotonic increasing: no missing codes due to R
- Comparator is the main element.

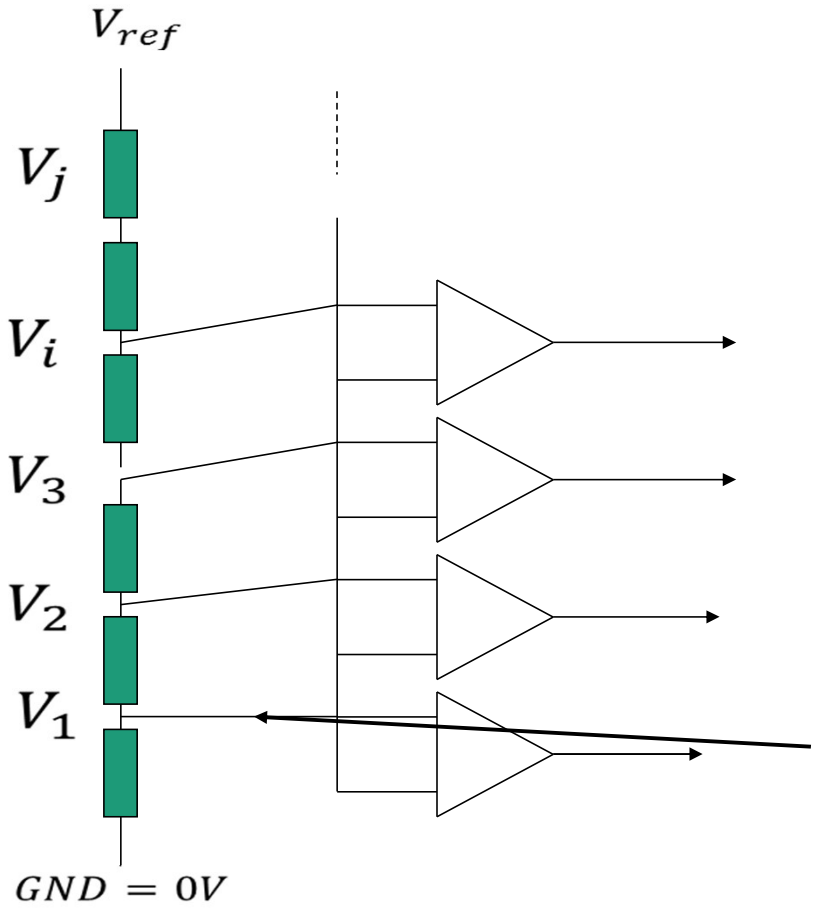
What's a Comparator- done on prev. lectures.

- It's a chain of gain stages (unlike op amp) to achieve fast response





FLASH continue: 0peration equation



$$V_1 = \frac{R_1}{(R_1 + R_2 + R_3 + \cdots + R_j)} \cdot V_{ref}$$

Simple voltage divider

$$if \quad R_1 = R_2 = R_3 = \ldots = R_j = R$$

$$Vi = iR * Vref \quad /(\sum_{i=1}^{j} Ri)$$

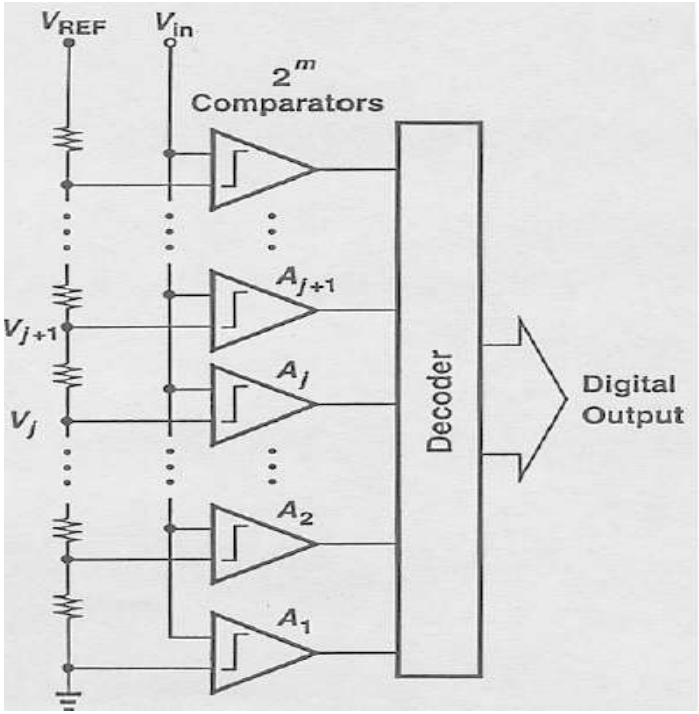
$$V3 = 3R * Vref \quad /(\sum_{i=1}^{j} Ri)$$

$$V2 = 2R * Vref \quad /(\sum_{i=1}^{j} Ri)$$

$$V1 = R * Vref \quad /(\sum_{i=1}^{j} Ri)$$

- For n bits need 2^{n-1} Comparators
- For n bit need 2^n Resistors

FLASH continue: number of comparator needed



- Suited for up to 7-8 bits of resolution
  - 127 - 255 Comparators
- Flash speed
  - As the comparator, logic, and input impedance driving the comparators.
- Output is like a thermometer

Example
Bottom-to-Top
111111111111 **maximum input**
..
...
000000001111
000000000111
000000000011
000000000001 **Input passed LSB,**
000000000000 no input

Total number of Comparators required is $2^N - 1$, where N is the resolution of the ADC

8 bit 257 lines 0000000000000000000000..

FLASH – detail each element

- Comparator Offset
- Resistor Mismatches
- Power
- Speed limit first stage
- Signal Feed Through
- Gain
- Dynamic Range – Max V_{ref}
- Comparator Meta Stability (and speed)
- Following stages – (bubbles)
- Clock distribution

- A good way to see the errors is to go over the flash design

Task: Need to build: 8 bits Flash ADC

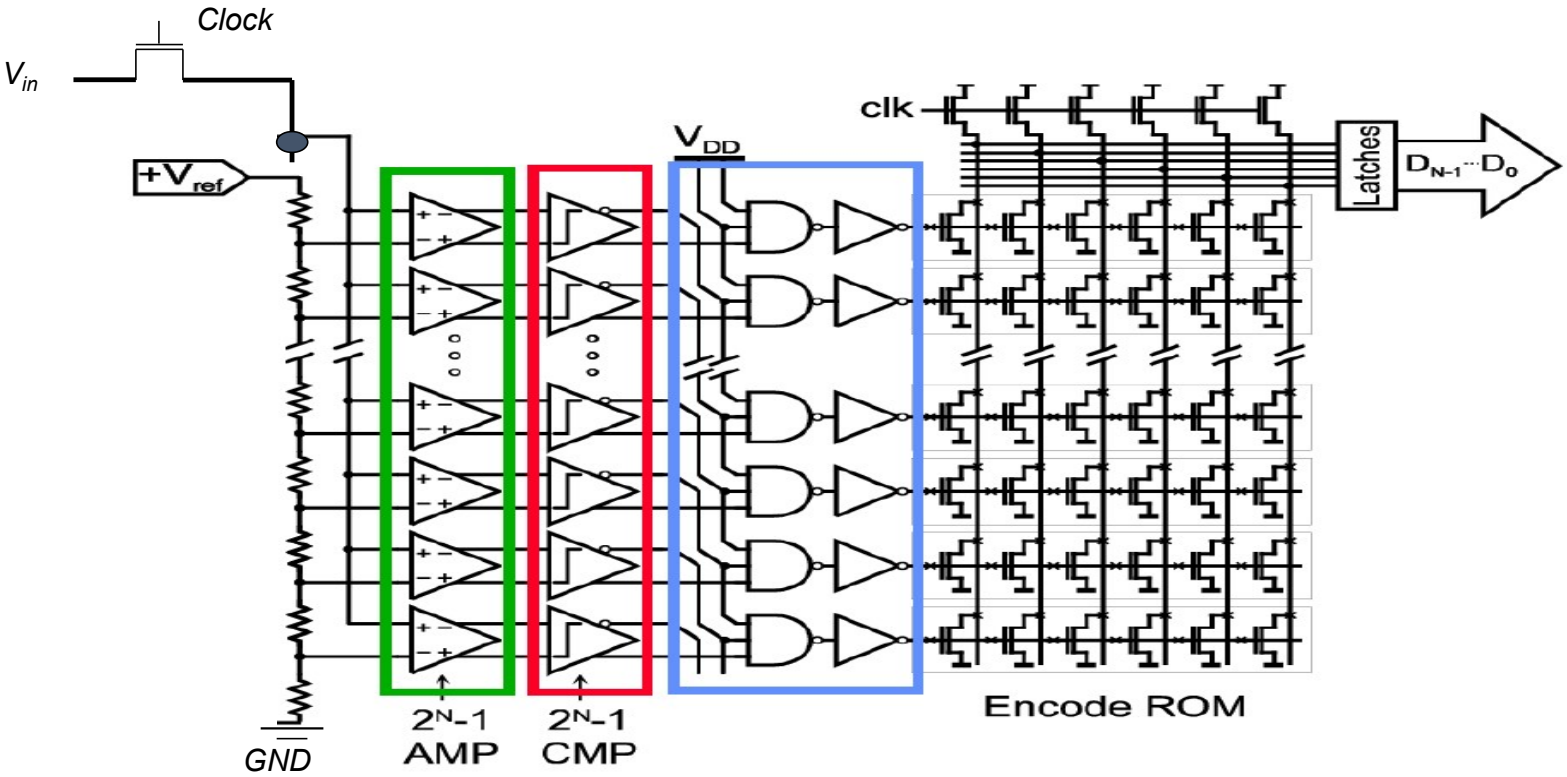
- Assuming:
  - Process 0.18um/1.8V
  - C_{ox}~6ff/u^2,
  - K_p=20e-6
  - K_n= 60e-6

$$K_n = \mu Cox$$

We can control the rest: sizes , we are the artists..

Step1: Choose an Architecture – our task

FLASH – Architecture



Source : K.. Leuven

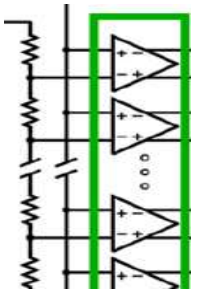
- Step1:Inventory:
  - 255 Comparators/Amp, 255 resistors
  - Logic decoder
  - Thermometer/binary
  - Missing T/H
  - References

Step 2:

- ❑ Design the Converter:
- ❑ (W/L) with Correct Accuracy:

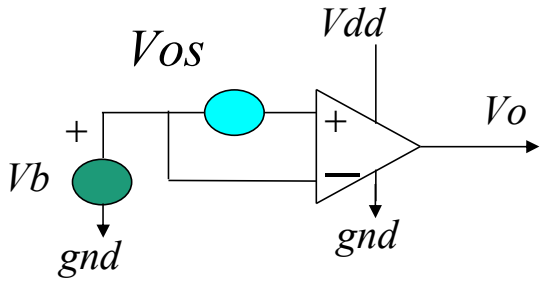
Find/look for:

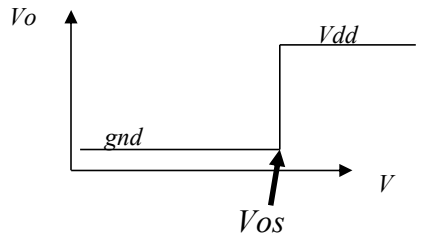
- ❑ Accuracy:
  - ❑ where in the design Non Linearity is created
- ❑ Comparator offsets – Random mechanism
- ❑ Resistor ladder – Random



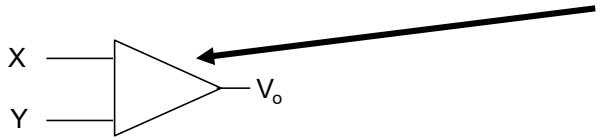
Design Example

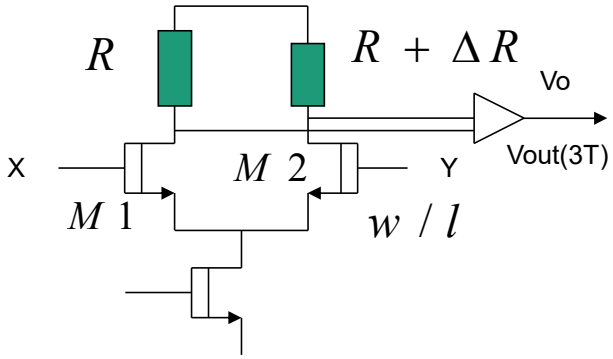
- Comparator Offset:
  - Find W/L of the Comparator





Offset – at which V_{os} the comparator switch without "effecting" lsb





$$Vos\ 1 = \Delta R / R \bullet (I / gm)$$

$$Vos\ 1 = C1 / \sqrt{Weff * Leff}$$

$$=$$

$$M\ 2 = M\ 1$$

Comparator offset

- Given process 180nm
- C_1 is:

$$C1 = 5(mV / \mu)$$

We use the equation from prev.

$$\sigma(\Delta Vt) = C1 / \sqrt{Weff * Leff}$$

But, now we need 3 Sigma's – so "no" error is created - yield

$$Vos \leq 3 \bullet \sigma(\Delta Vt)$$ oopsss.. now yield is important…3..

Remember:

- Could be the biggest problem: bad for low voltage technologies

Comparator Offset Calculations cont.

$$Vos\ (\max) = 1/2 \bullet LSB$$

$$Vos = 3 \bullet C1 / \sqrt{Weff * Leff}$$

½ of 3.92 = 3 C1/..

$$VFs = 1V \qquad Vlsb = 1/255 = 3.92\ mV$$

$C1 = 5(mV / \mu)$ → Process given

$$\sqrt{Weff * Leff} = 5mv /(1/2(Vfs / 255) = 3 \bullet (10\ mv / 3.92\ mv)$$

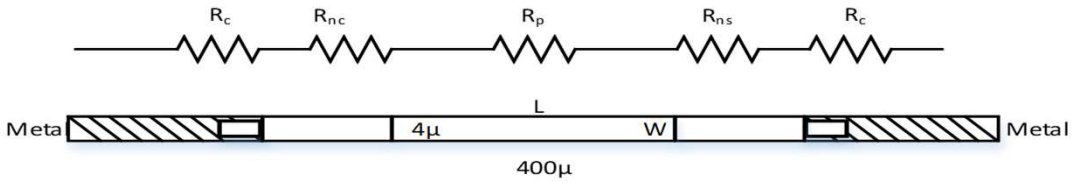
$$Weff \bullet Leff = 58.52$$

❑ *Implies L=0.18u W=325un*

We assumed comp input stage was all..but got feeling how big can things be…

Ladder Mismatches – Length Determinations

Silicon Resistors



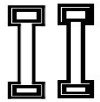
$$R_p \sim 90\% - 99\%\ of\ R \quad Saliside\ is\ removed = 2$$

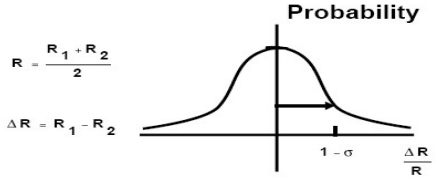
$$R_{nc} \sim Exposed\ Area\ to\ Saliside \sim 5\frac{\Omega}{v}$$

$$R_c \sim Contact\ Resistor\ to\ Metal \sim 1 - 20\frac{\Omega}{CT}$$

R Matching

$$G\left(\frac{\Delta k}{R}\right) = \sqrt{\left(\frac{A_{Rp}}{\sqrt{W \times L}}\right)^2 + \left(\frac{A_{Rnc}}{\sqrt{W_{nc} \times L_{nc}}}\right)^2 + \left(\frac{A_{nc}}{\sqrt{Contact\ Area}}\right)^2}$$





Need ½ LSB=0.196%

R Length =937um

Example:

- ❑ Ignore all but poly resistance (see next slide), and
- ❑ If $\frac{\Delta R}{R} = 2\%$ (1um x1um) – Process given
- ❑ Take 3 sigma's = 1u x 1u ➔ 6%.

$$\Delta R < \frac{R}{2^{n-1}} \cdot 0.5 \quad \gg \quad Need\ \frac{\Delta R}{R}\ of\ {}^1/_2\ LSB = 0.196\%\ ({}^{100}/_{510})$$

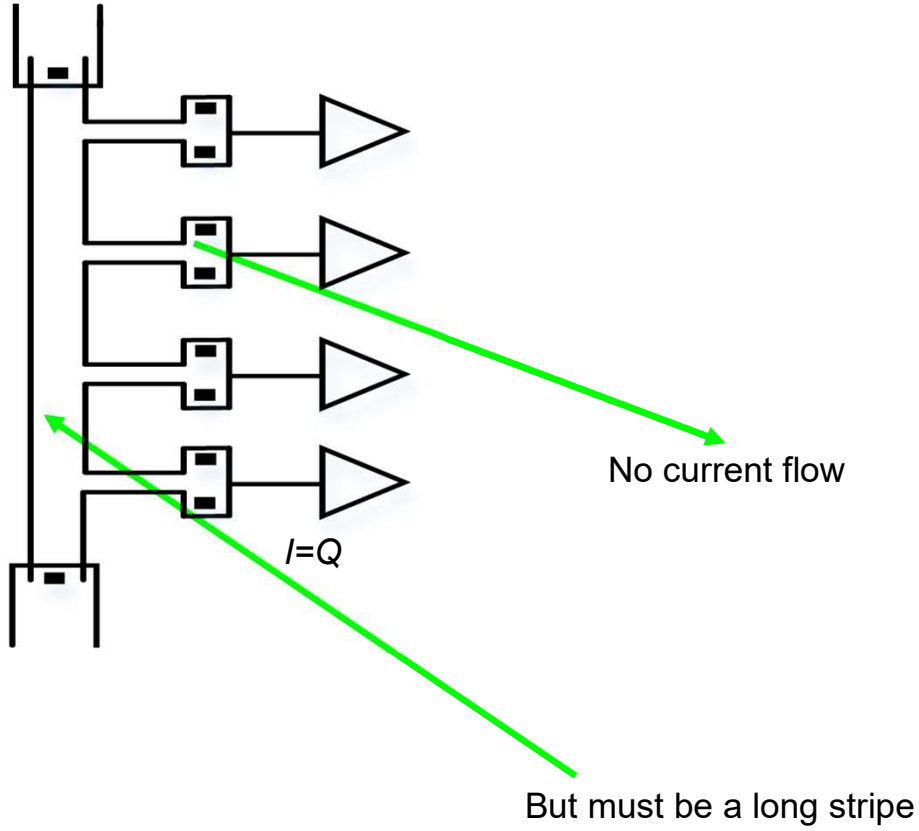
$$\frac{0.06}{\sqrt{Area}} = 0.00196 \quad \gg Area = 937\mu^2 \quad \gg use\ 1 \times 937\mu m$$

Generally: matching possible up to 10-11bit

Get Rid of Contact Errors

Avoid Contacts – Matched Resistors

$$R_{cont} = 20\frac{\Omega}{CT}$$



Step 3. Power Dissipation

Power – An Estimation

Power (due to comparators I_{in})

$$\rho = V_{OD} \times I_{comp} = V_{OD} \times 2 \times k\frac{W}{2L}(V_{GS} - V_T)^2[2^n - 1]$$

$$For:$$
$$K_n = 60E - 6,$$
$$L = 0.18\mu$$
$$W = 325\mu$$
$$and\ if\ V_{GS} - V_T = 0.1$$

$$I_{DS} = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{GS} - V_T)^2 \times 255 = 541\mu A \times 255 = 138mA$$

big assumption

P= Without T/H, logic, clock, resistor ladder we re at 248mW

- *Should we increase L? (keep WxL, drop Power?)*
- *Should we check real speed to get I?*
- *Should we calibrate offset and not increase W/L?*

Stop and re think:
Isn't power based on I,
shouldn't we look at speed first? For min I

And we didn’t even start talking about thermal noises..etc..

We have R we have comp gm(I and w/l)…

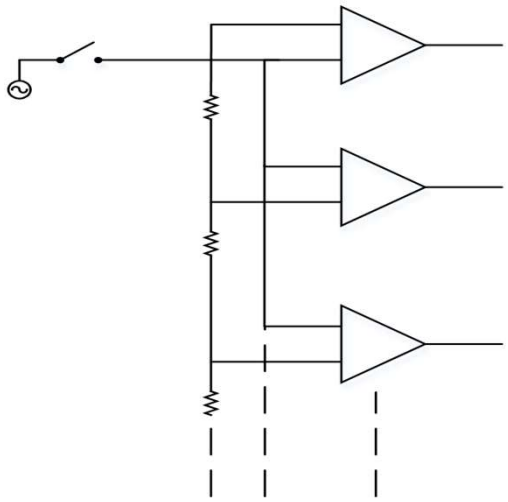
So should be **easy to check..**

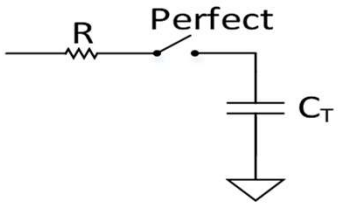
If in fs/2 we don’t generate >1/2LSB..(from 4KTR, and 8/3KT/gm

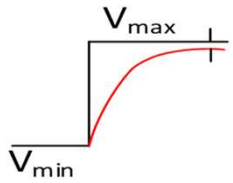
What's the catch ? do all comp contribute ?

Step 4. meet speed limits

Speed Limit due to Front Stage – A Model

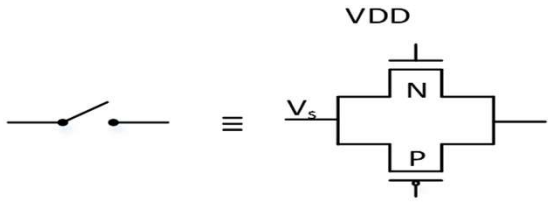




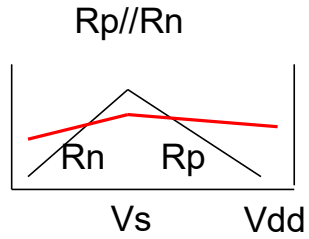


$$R_p \parallel R_n = \frac{1}{k_p \frac{W}{L}(V_{DD} - V_T)} \parallel \frac{1}{k_n \frac{W}{L}(V_{DD} - V_T)}$$

V_s



C_{in} is so large that R_{in} is important



1st identify region of operation vds~0

$$I_{ds} = \mu C_{ox}\left(\frac{W}{L}\right)\left[(V_{gs} - V_{th}) \cdot V_{ds} - \frac{1}{2}{V_{ds}}^2 \qquad V_{gs} - V_{th} > V_{ds}\right.$$

Speed Limit due to Front Stage – Acquisition Time

V_{fs}

1) $V_{in} = V_o(1 - e^{-t/RC})$

2) $V_{in} + \frac{\Delta}{2} = V_o$

3) $\Delta = \frac{V_o}{2^n - 1}$

$$\gg \quad \frac{V_{in}}{V_o} = 1 - \frac{1}{2(2^n - 1)}$$

$$\textit{Plug into [1]} \gg \quad 1 - \frac{1}{2(2^n - 1)} = 1 - e^{-t/RC}$$

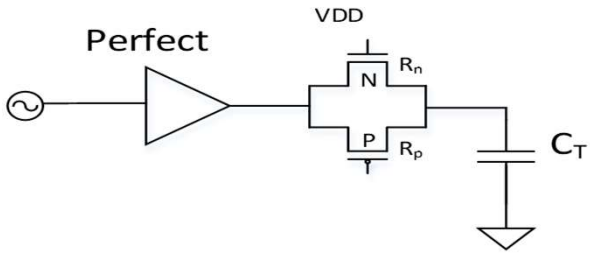
$$\textit{If} \quad \frac{1}{(2^n - 1)} \approx \frac{1}{2^n} \quad \gg \quad t = RC \cdot ln2 \cdot (n + 1)$$

$$\boxed{t = 0.693RC \cdot (n + 1)}$$

or

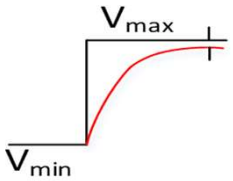
$$8bits \gg RC \cdot ln(255 \cdot 2)$$

need $6.23\ RC's$



$$R = R_p \parallel R_n$$

$$C = C_T \quad (ADC)$$



n [bits]	# of RC's
4	3.46
8	6.23
10	7.62

Speed limit due to front stage – calculation

$$C_{ox} = 6\,ff/\mu^2 \qquad R = 50\Omega \;\; (an\;Assumption)$$

$$W/_L = \frac{325}{0.18}$$ From offset calculations W/L=325/0.18

$$C_T = \frac{2}{3} C_{ox} \cdot 255 + C_{Routing}$$ *Assume all in Saturation (Too optimistic)*

$$C_T = 6\,ff \times 325 \times 0.18 \times 255$$

$$C_T = 59.7\,pF$$

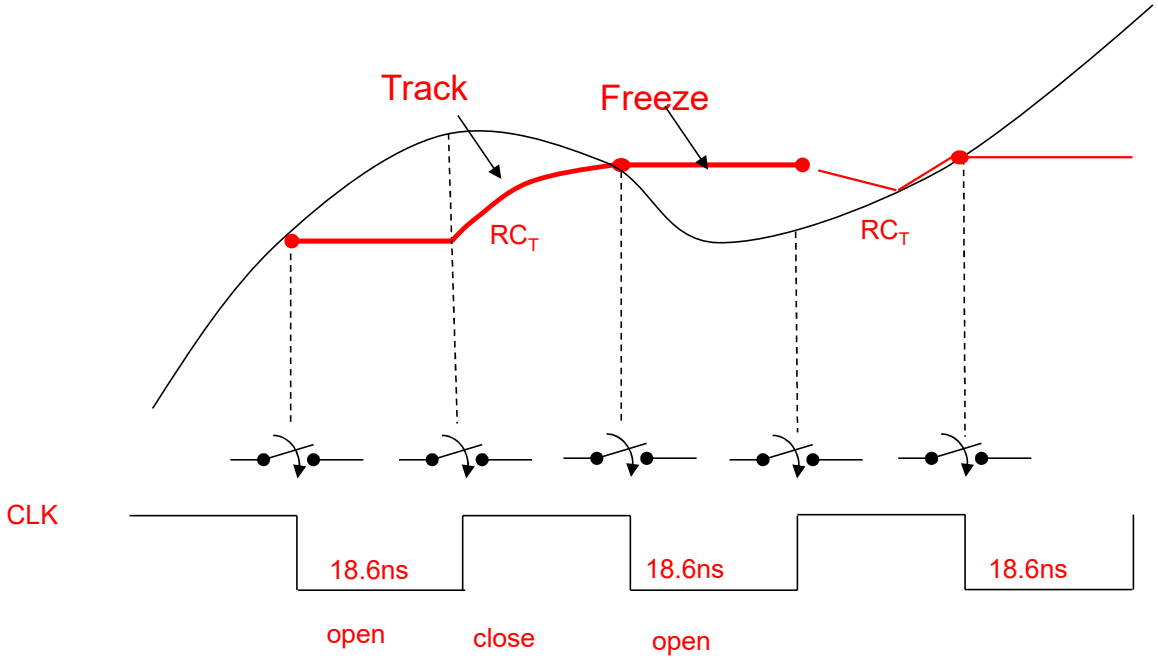
Disappointing low frequency

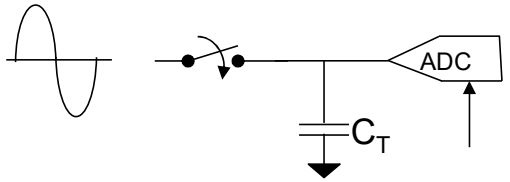
$$t\,(8\;bits) = 6.23\,RC = 18.6ns \gg 53.7\,MHz$$

Stop and re think:

- New buffer to drive low cap?
- Re-look at matching – calibrate to reduce C_T?

Speed limit due to Front Stage – View

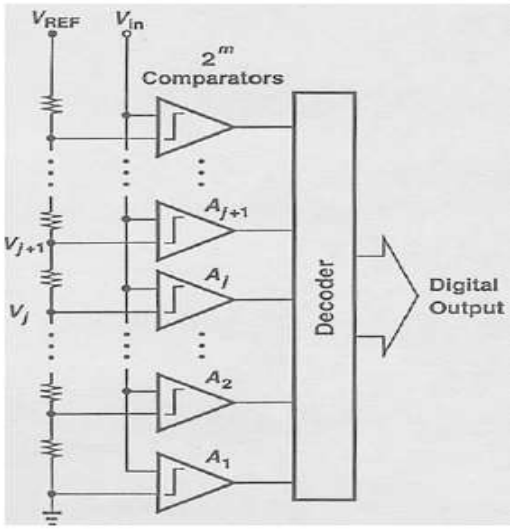




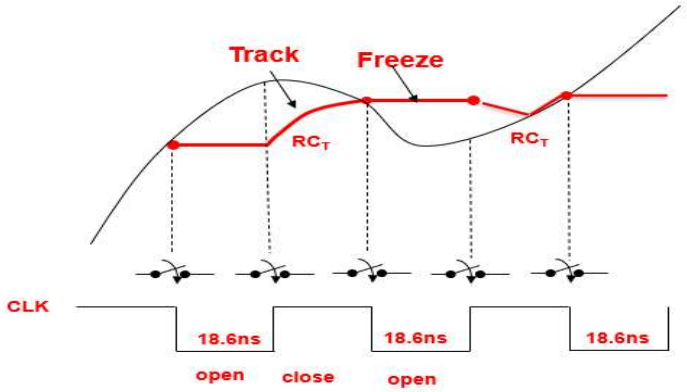
53.7MHz

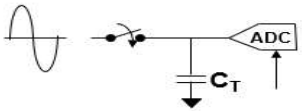
But when is min to full scale
Happen ?

Quick summary prev. lecture



R





53.7MHz

Do we FFT the red ? Disaster…

Problem with Cin-speed-.. Area..- but

- If $\frac{\Delta R}{R} = 2\%$ (1um x1um) – Process given
- Take 3 sigma's = 1u x 1u ➔ 6%.

Rlsb=R/256. Rlsb can be off 50%..

$$\Delta R < \frac{R}{2^{n-1}} \cdot 0.5 \quad \gg \quad Need \ \frac{\Delta R}{R} \ of \ {}^1/_2 LSB = 0.196\% \ ({}^{100}/_{510})$$

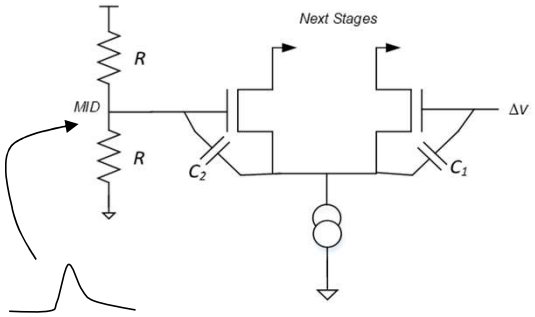
$$\frac{0.06}{\sqrt{Area}} = 0.00196 \quad \gg Area = 937\mu^2 \quad \gg use \ 1 \times 937\mu m$$

$$\Delta R < \frac{R}{2^{n-1}} \cdot 0.5$$

Speed Limit: feed through speed

Signal Feed Through

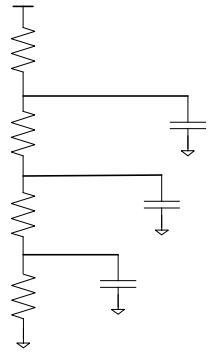
Who is in Sat? $C_{gs} = 2/3\ C_{ox}$
Who is in Off? $C_{gs} = C_{ov}$, C_{ox} to Bulk = C_{ox}
Who is in Lin? $C_{gs} = ½\ C_{ox}$



$\frac{2}{3} C_{ox}$

Worst Case Mid Ladder R/2, $\frac{C_1 \cdot C_2}{C_1 + C_2} \approx \frac{1}{2} C_{gs}$

	Sat	Off	Lin	
IF	*1/3*	*1/3*	*1/3*	» $\tau = RC = \left(\frac{R}{2}\right)\left[\frac{2}{3} C_{ox} \frac{n}{3} + \frac{1}{2} C_{ox} \frac{n}{3}\right]$



To reach ½ LSB of 6 bits » 4.8 RC

Add big filter on Ladder

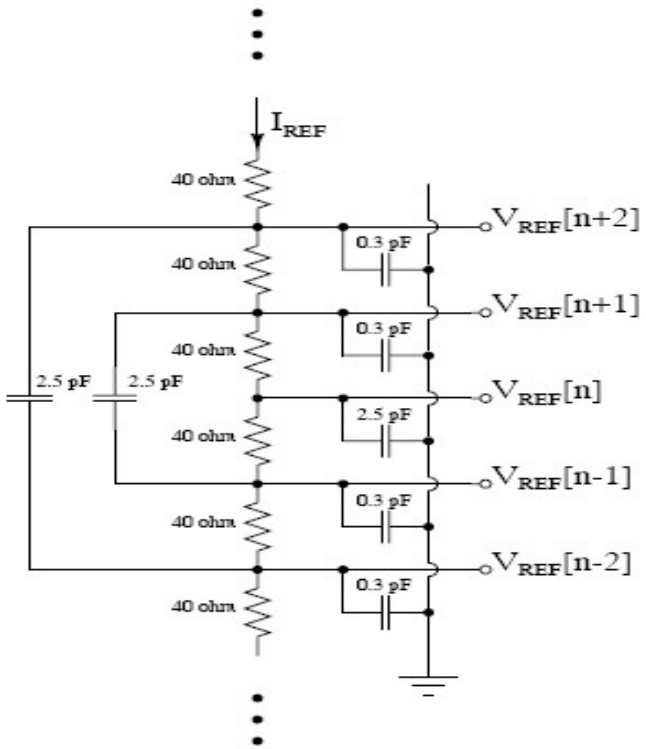
$$\frac{V_{mid}}{V_{in}} = \frac{\pi}{4} \cdot f_{in} \cdot R_{ladder} \cdot C$$

Source : Esscirc 2002. Leuven

C total capacitance
Find max input ladder R.
for no effect on feed through

(After matching calculations are satisified).

An Example – reduce/removed feed through effect

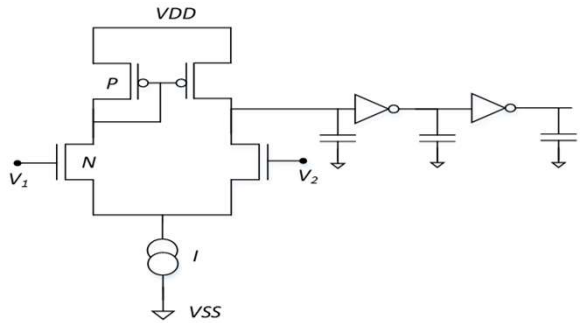


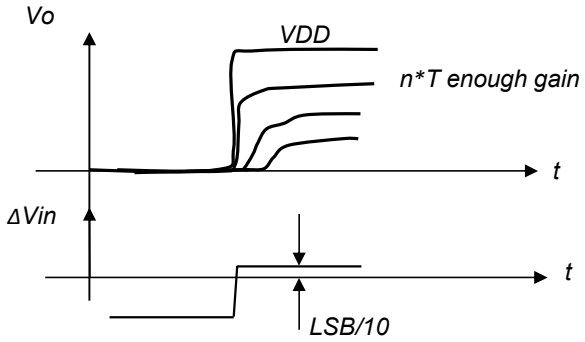
Example: Cap stabilization 5b 1GS.s flash
Source: Esscirc 2006 Helsinki univ, Olli Viitala

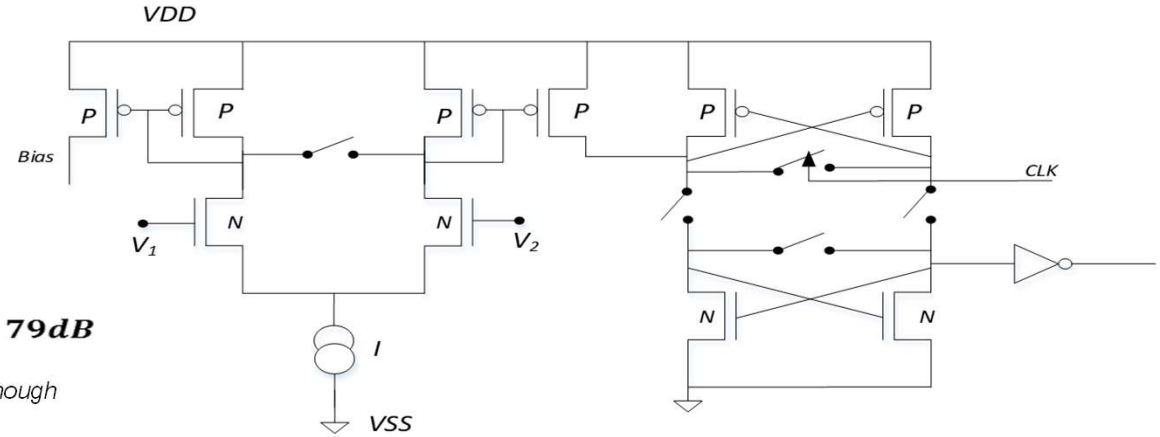
Step 5. Spec of the needed comparator

Comparator Gain – More in Comparator Design

Comparator Gain







Need Enough Gain

1. $\Delta V = V_1 - V_2 = \frac{1}{10} LSB$

$VDD = 1.8V, \qquad n\ bit$

$A_0 = \frac{1.8}{\frac{V_{FS}}{2^n}} \cdot 10 = \frac{1.8}{\frac{0.5}{2^8}} = 18 \cdot 2^9 = 9,216 = 79dB$

1 or 2 Stages – Not Enough

Need minimum of 300mV
Before the invertor trips

2. After gain we need to also look at speed response

3. ***Let's creat a Latch on Positive Gain***

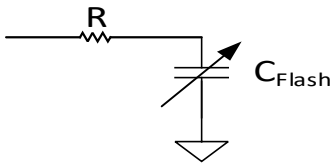
More details in comparator design

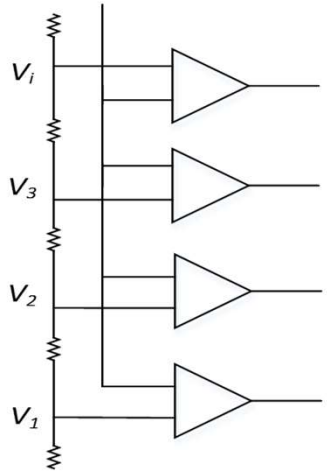
More on Distortions – Variable BW – Flash Specific

capacitors	Saturation	Linear	Off
C gate to S	2/3Cox+Cov	1/2Cox+Cov	Cov
C gate to D	Cov	1/2Cox+Cov	Cov
C gate to B	0	0	Cox//Ccb+..

$$HD_2 = \frac{V_o \omega C_1 R}{2\sqrt{1 + (2\omega C_0 R)^2}}$$

Source : Esscirc 2002 Leuven

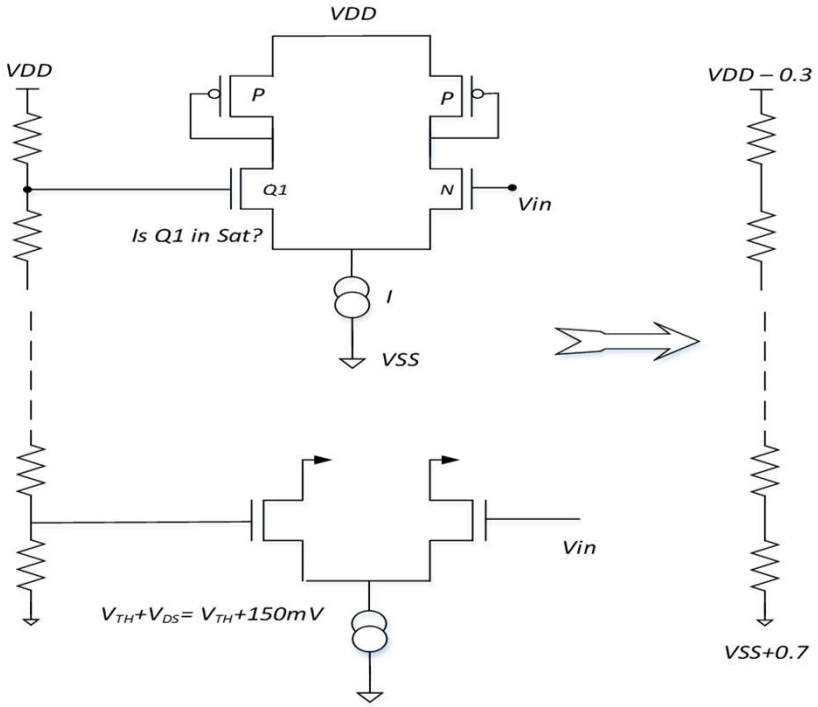




Step 6. Set the Maximum Dynamic Range

Dynamic Range – Max Vref

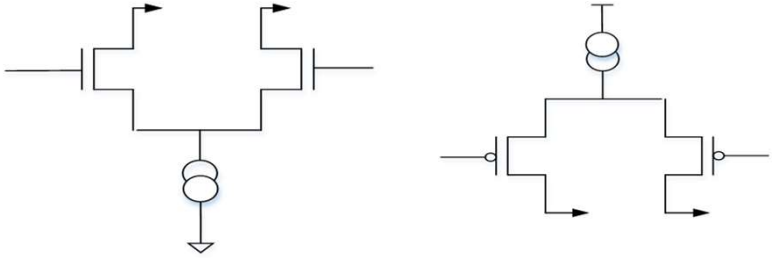
Full Scale Possible



- *Limit the Ladder Full Scale*
- *Limit the SNR*
- *Or – 2 Comparator Type*

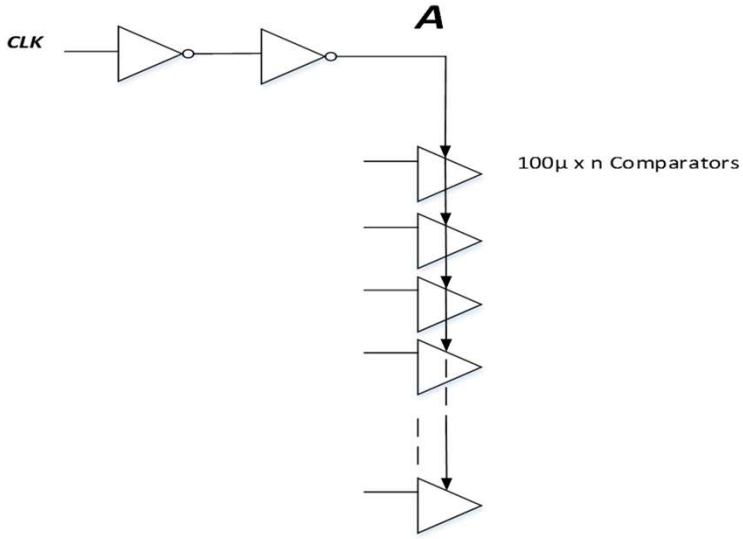
V_{FS}=1.8-5%-0.7-0.3=0.71V
(so we made error assuming 1v)
In step 2.

V_{FS} limit the ladder full scale
Limit the SNRD→ VLsb.
Need to be maximized most times

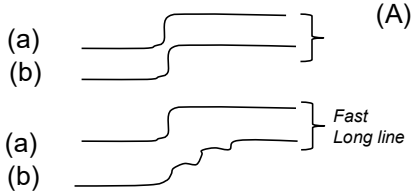


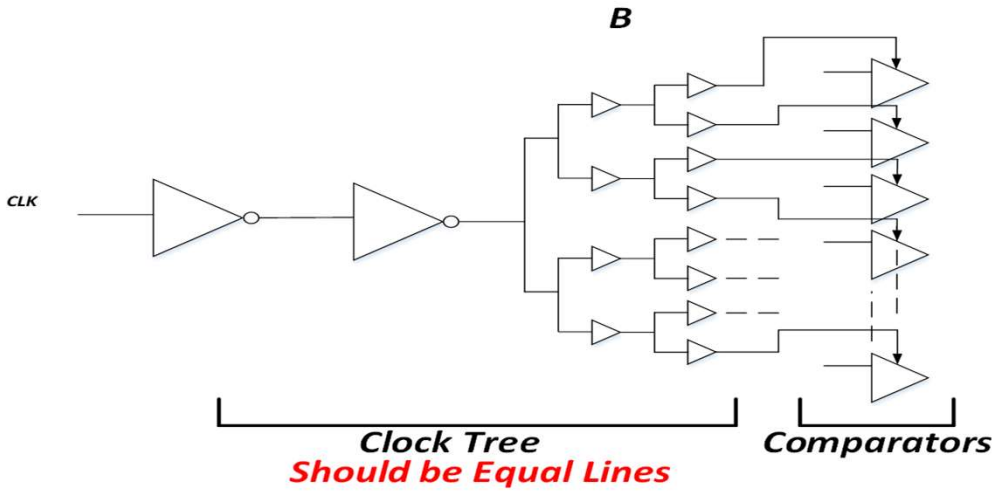
Step 7. Clock – Jitter Requirement
Set Requirements

Flash Clock Distribution Errors



(A)





An Estimation = 1ps/µ

$$T_d = 2\pi\sqrt{LC} \approx 2ps/100\mu m$$

Last Problem

Deterministic Jitter ΔVCC → ΔJitter

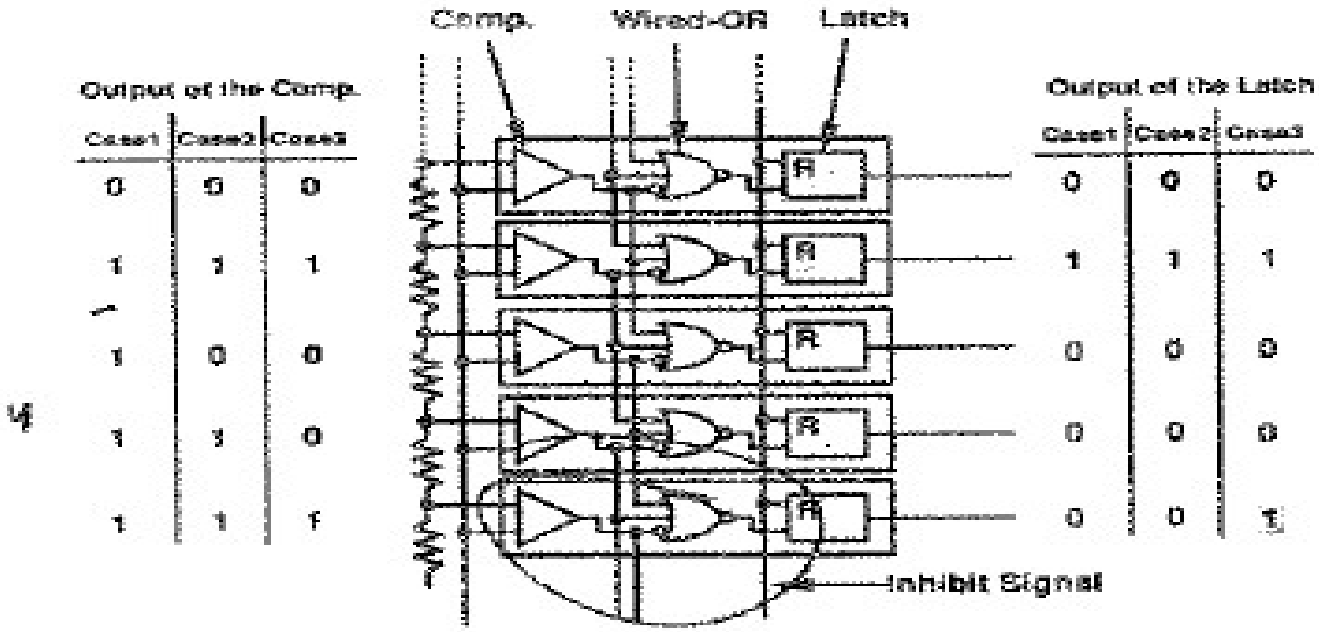
Probability Get Hz

Not every Comp Clock signal at the same time

If NO → S/N bad!

Step 8. Digital design – can we help the analog ? What can we do there..

Error Correction



Bubble error look at your neighbour
Won't correct two errors

Design Check – Are We Satisfy? Lets look at the FOM value..

- Definition 2.

$$FOM = \frac{P}{2^{ENOB} \times 2 \times ERBW}$$

$$Energy\ over\ Decision = \frac{Power}{SamplingRate \cdot 2^{Nbit}}$$

→ Last lect

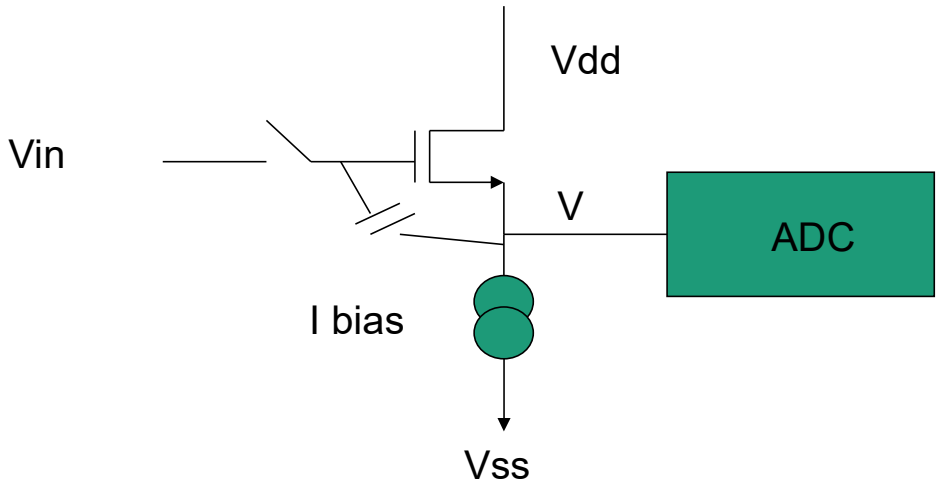
(FOM = 17 is high→ 248mw / (57e6 x 255)= 17e-12

(248 from 138 x VCC.)

Since nothing works well..
How about other architectures ?

Question…

- Why does this circuit reduces capacitance of T/H and help drive the large capacitance of the ADC ?



continue

FLASH ADC ARCHITECTURE

ALTERNATIVES- **2 Step*

ALTERNATIVE DESIGNS OF FLASH ADC

Errors: Meta stability- quick re-look.

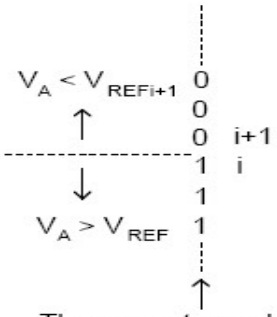
Differential Architecture

Charge Flash architecture

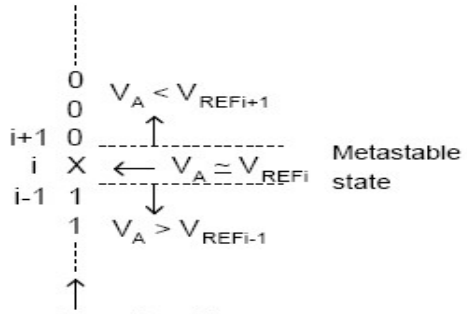
Meta stability

Ref.: IEEE JSSC, vol. 31, pp. 1132-1140, Aug. 1996, 7-b 80-MHz flash ADC

Metastability error: occurs in ADCs when undefined comparator outputs pass through the encoder to the converter output bits.



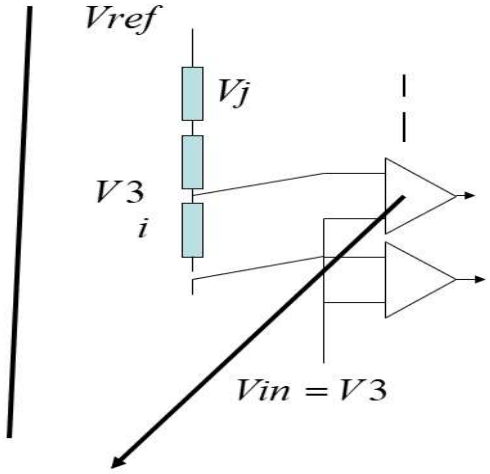
Thermometer code with valid comparator outputs



Thermometer code with metastable comparator

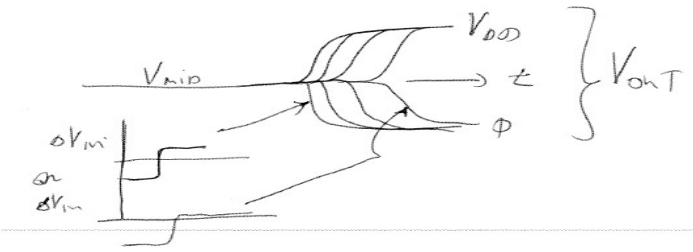
Key:
No one is immune

even a slow system should have fast comparator

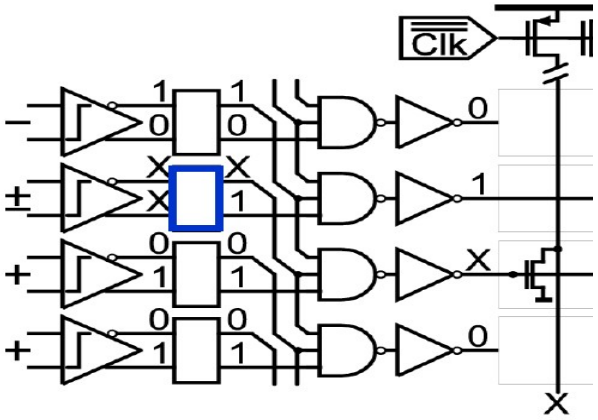


Vout=A(Vin-V3)=vdd/2 ?

Normal response is exponential
It take longer and longer at the 2 comparator input get closer and closer



X means far from 0 or V+ (~vdd/2)
You can't design it out
You can reduce its occurrence



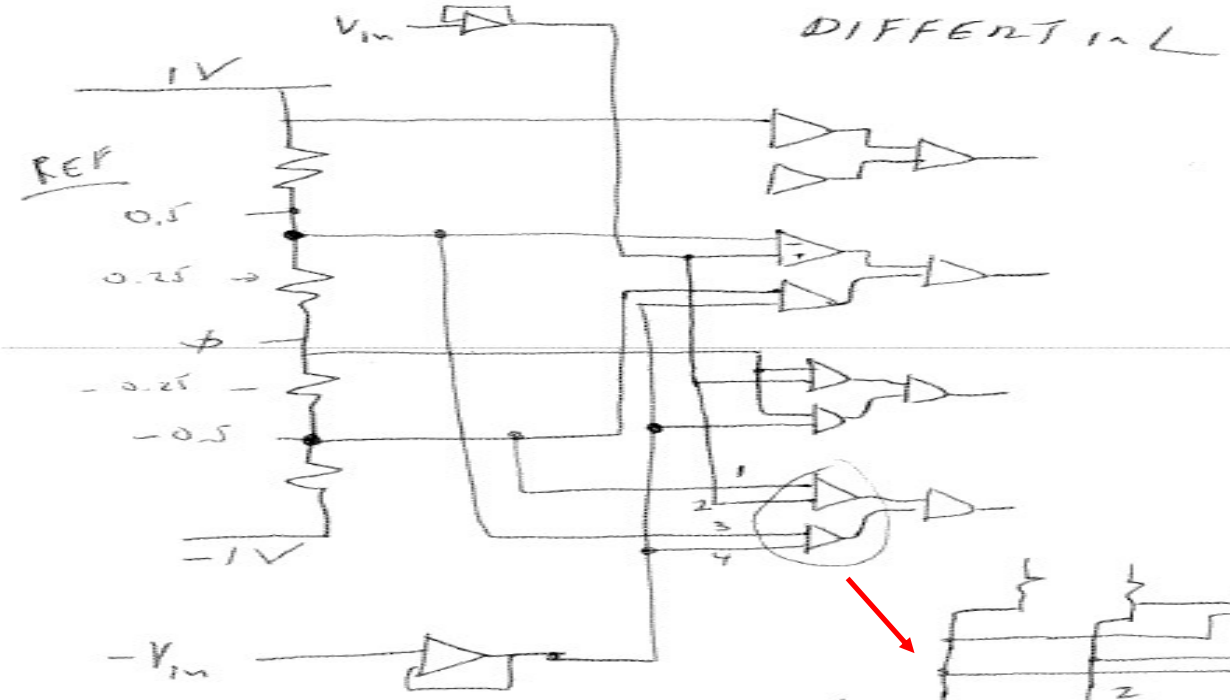
Differential Designs

Differential /improved implementation
FLASH architecture

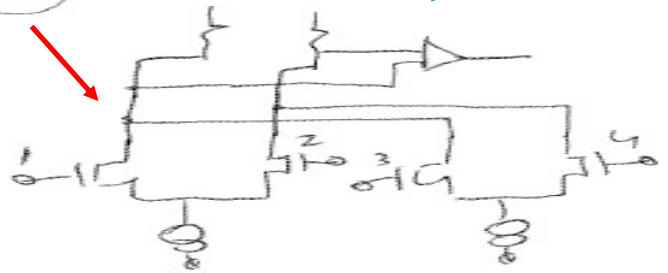
Differential Design

Capacitive Charge FLASH

DIFFERENTIAL-details



Easy to buid 4 input
comparator and to sum currents in CMOS :

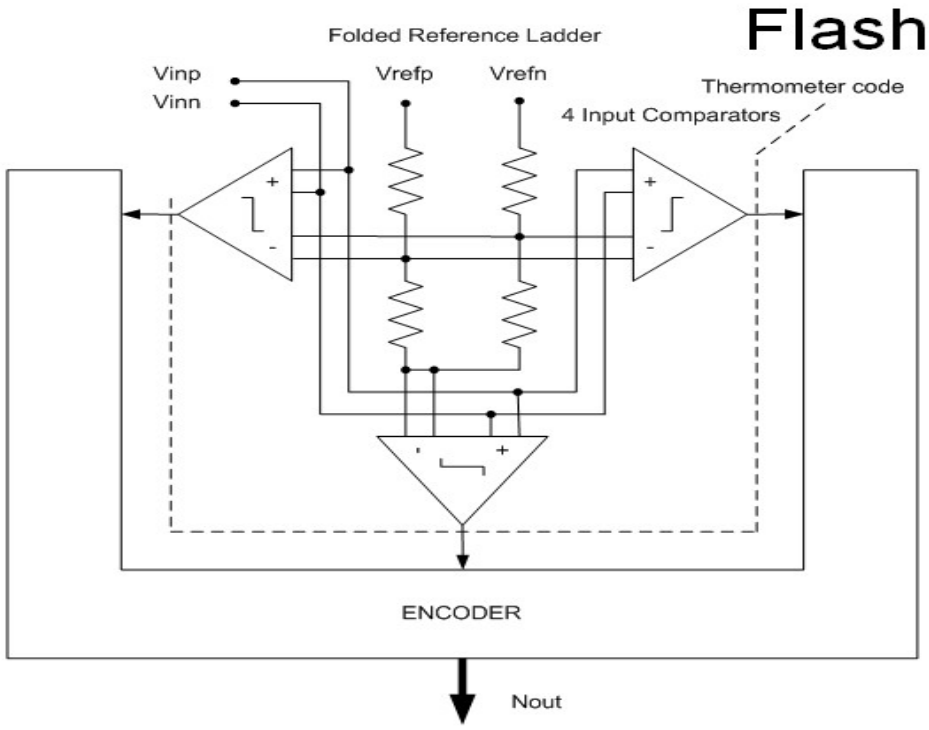


* FLOAT FROM 0
* USE CM mid point
* 2x Signal , Routig ! ok for 3-4 bits

DIFFERENTIAL

INL GOES TO 0 In the middle
Signal is doubled routing is harder

Simple to make differential comparator



Fully differential implementation:

- wider dynamic range
- better noise immunity
- better linearity

Other reasons :

Symmetry is preserved HD2, HD4 get reduced/cancelled

CAPACITIVE CHARGE FLAH

Architecture Alternative: Capacitive Charge ADC

Can we use an inverter as simple gain stage
Use capacitors to transfer Vin-Vref x gain.

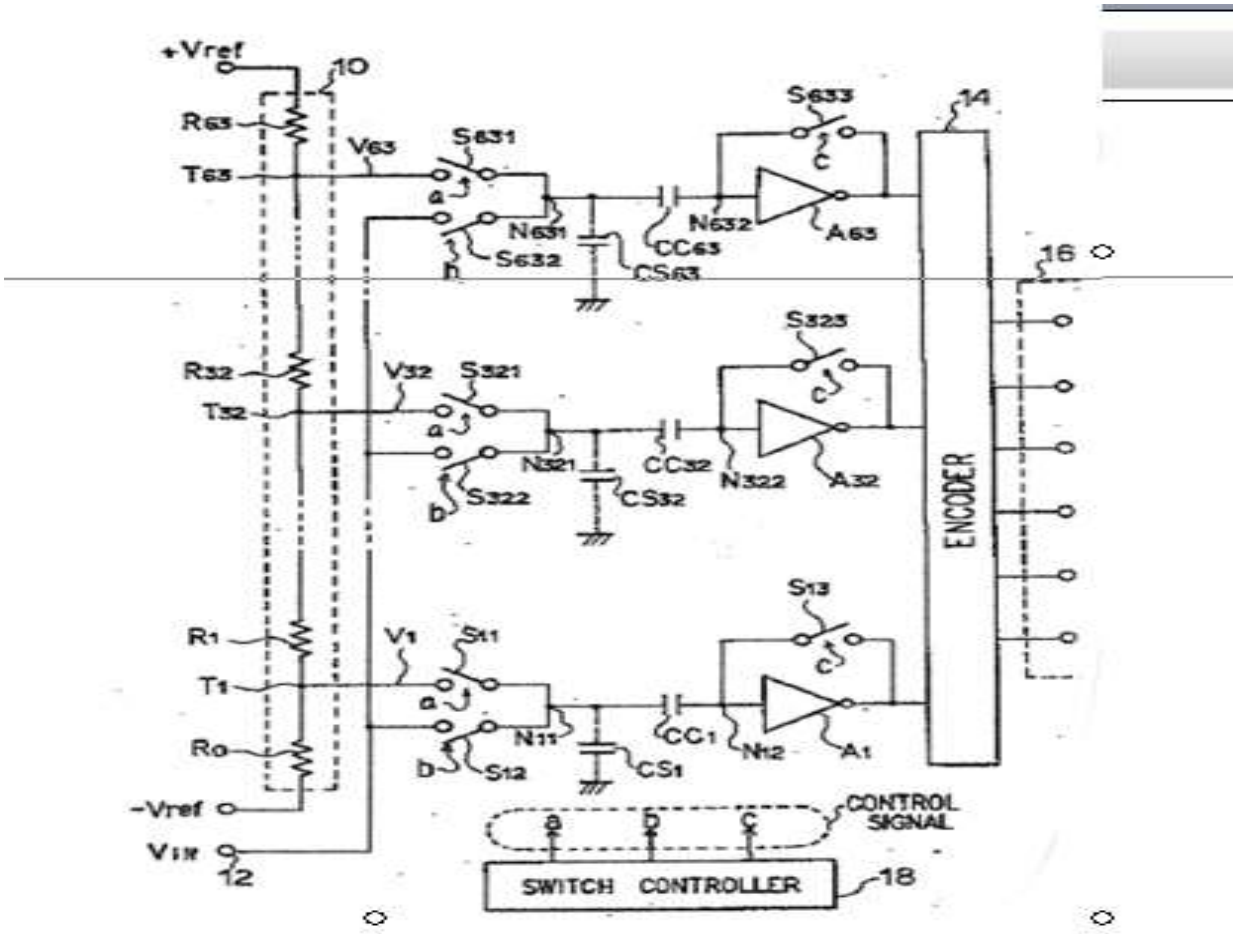
Why ?

Inverter is a digital cell no special process needs
It draw 0 DC current (power)
very fast and simple, power is lower..

the reason…(Offset cancellation is build in) !

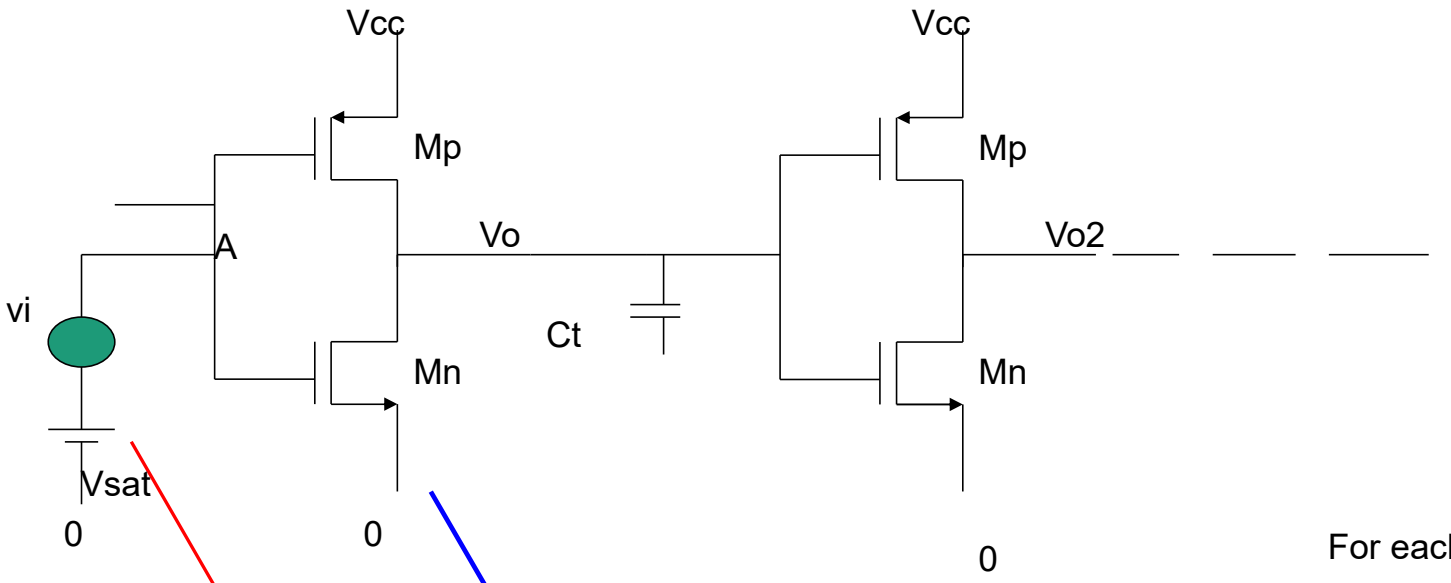
simpler comparator

Example: Create the ladder codes.



Source: Fairchild Data sheet

Operation- Inverter chain- as gain stage



For each stage

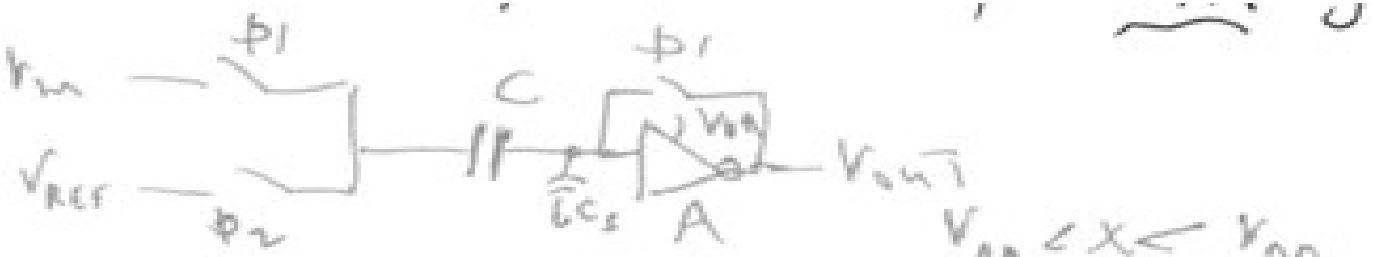
Av(dc) = (gMn+gMp) x rop//ron

Pole = 1/ 2pi Ct (rop//ron)

Amplification is done but

Next how to fix the DC, mid point ? (in saturation)

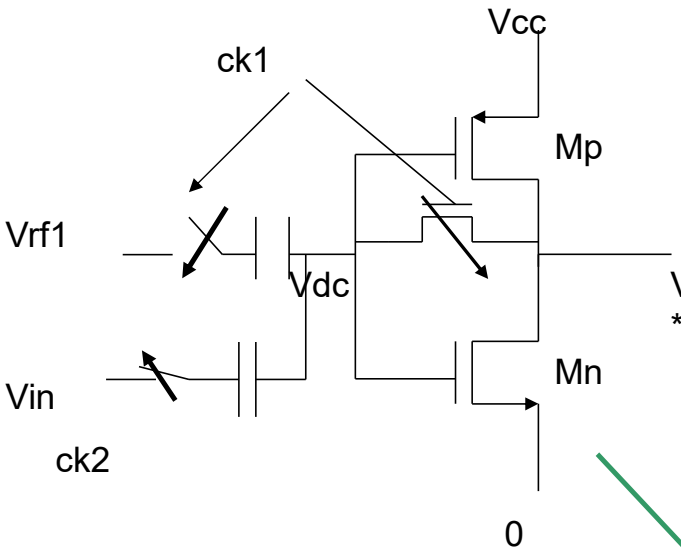
Next: Can we create differences with one input- at A



$V_{SS} < X < V_{DD}$

$$V_{out} = (V_{REF} - V_{in})\left[\frac{C_s}{C_s + C_s}\right] \cdot A$$

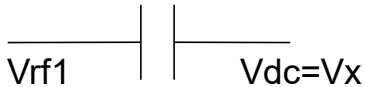
Insert the second level - Subtraction and gain



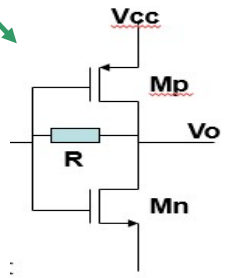
V0 = Vdc
And No offset

Q1=C(Vrf1-Vx)

Model at ck1=1 (closed) ck2=0

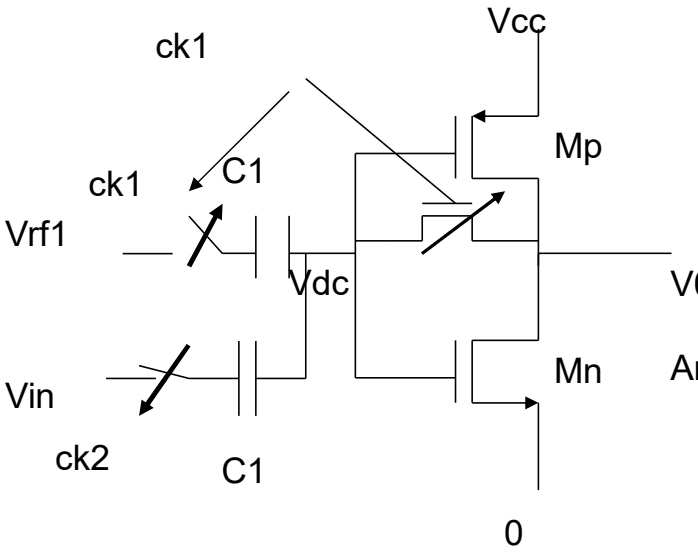


Step 1
Ck1=H closed
Ck2=L open



v0=vi the inv. is for sure in
Saturation and in low gain/impedance

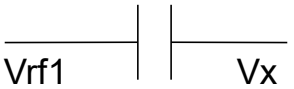
Insert the second level - Subtraction and gain



Step 2
Ck1=0 open
Ck2=H closed

Q1=C(Vrf1-Vx)

Model at ck1=1 ck2=0

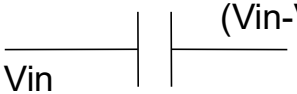


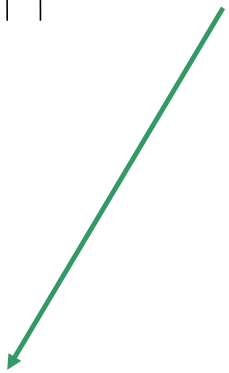
V0=(Vrf1 - Vin)Ao(f) + what it was before(Vdc)

And No offset.

Model at ck2=1 ck1=0

(Vin-Vrf1)+Vx





Speed

Speed Estimation:

6 bit ADC, no S/H
At L min130 nm (Cox ~ 13ff/uu) can get to 1-2 GHz – Flash “only”

Example:
Input Delay= 150ps (5.5/2piRCin + RladderCgs/2 to drive 63 comp/calibrate)
+ 250ps comparator + 100ps logic (25ps/gate) = 500 ps max
Possibly latch after comp and save some of the 100ps. (50ps)

Sample at 2.0GHz max through put (Input frequency)
twice the min delay ~ 1 GHz

FLASH ADC- SUMMARY

Bad-Good

Monotonic

Very fast, No amplifiers, Resistors can match well to 10b

Design:

Big input capacitance

Comparator offset is an issue

Clocking routing sampling time

Meta stability

Decoding to avoid bubbles

If S/H is used – Distortion added

Hardware:

Exponential in complexity

High in power for 7 bits or more (127 comparators)

Could lead to large die size

References may need to be filtered from kick back

Medium: to scale down in technology → power supply!

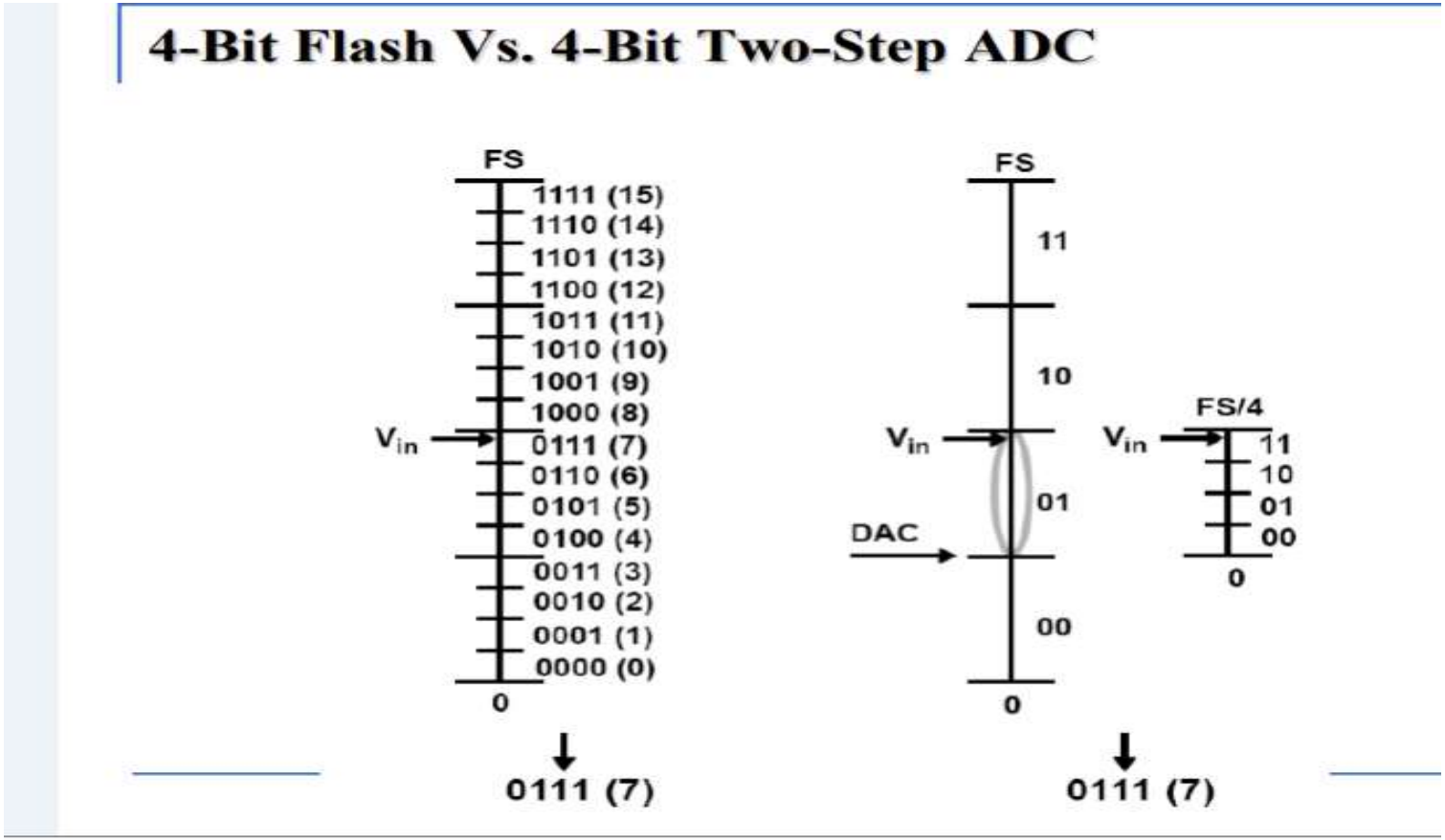
Power	~ 2 to N
Area	~ 2 to N
Cin	~ 2 to N
R ladder	~ 2 to N

Here N is an increase of effective resolution

Since Flash silicon Area and Power grows exponentially
How about different architecture

Sub-ranging ADCs

ADC Architecture Options: Sub-ranging (2-Step) ADCs



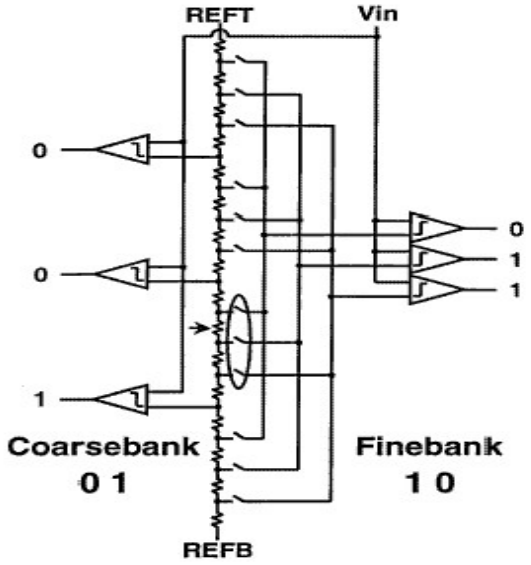
Two-step: subranging ADC

+ $2(2^{N/2}-1)$ comparators

  Coarse bank selects which part of reference ladder to connect to fine bank

- Speed limited by settling of fine references

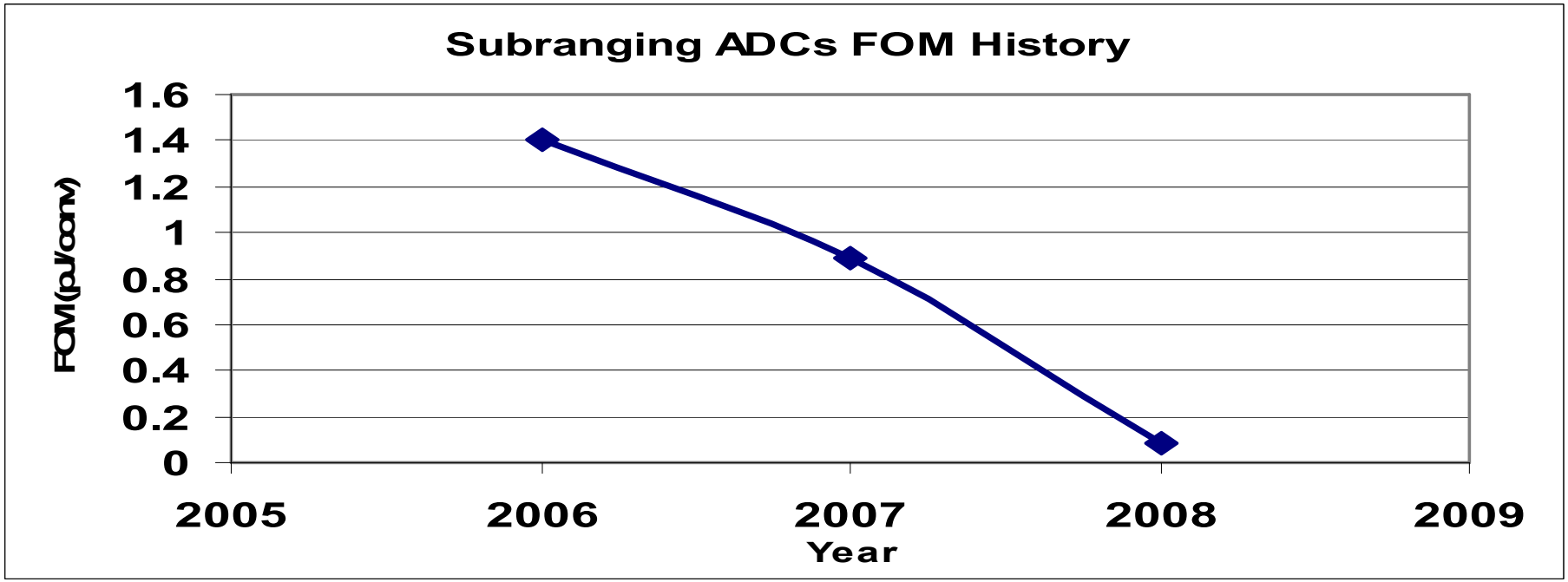
  parasitic capacitance from > 2^N switches + large kickback



Source: BRCM

Lost time- Need twice the time and S/H.
Resistor get glitches now impedance is important
New many switches (2 to the N – M Coarse connection)

Sub ranging ADC FOM History



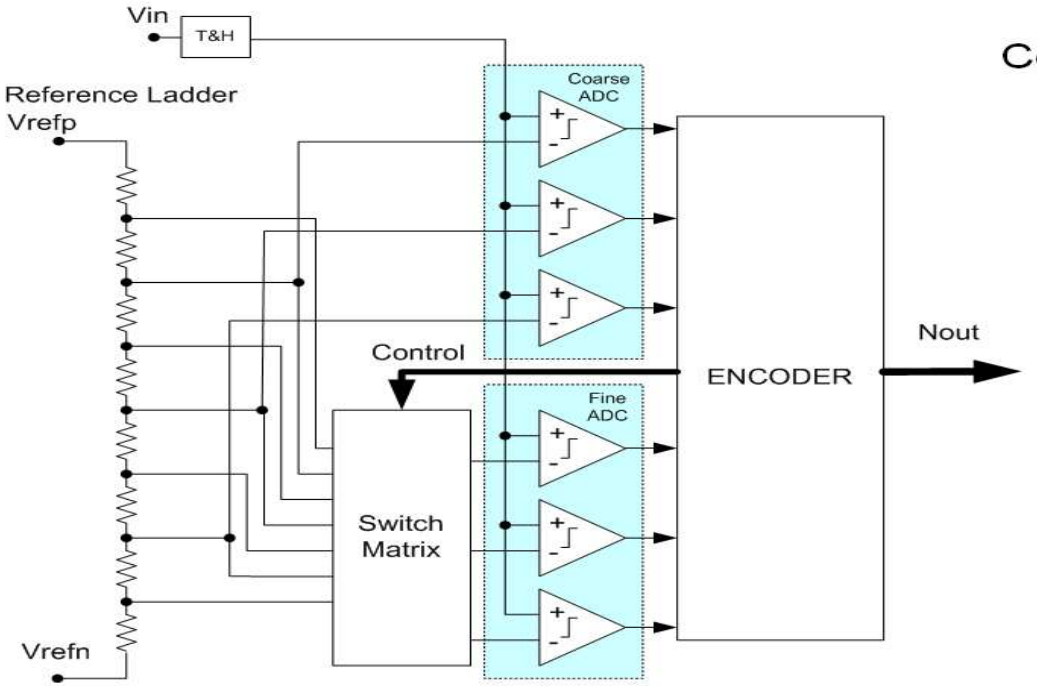
2006 ➔ 6b & 1Gs/s (90nm CMOS)

2007 ➔ 10b & 160Ms/s (90nm CMOS)

2008 ➔ 5b & 1.75Gs/s (90nm CMOS)

Operation details : how to reduce number of comparators

Sub-Ranging ADC Basics



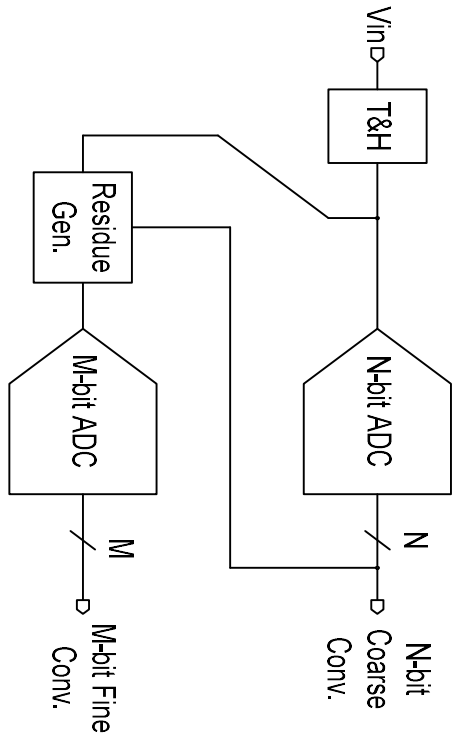
Conversion is done in two steps

- coarse ADC determines the region of the ladder the fine ADC will use
- regions can overlap to produce the redundancy that relaxes the offset requirement for the coarse ADC
- for the fine ADC – strict offset requirements

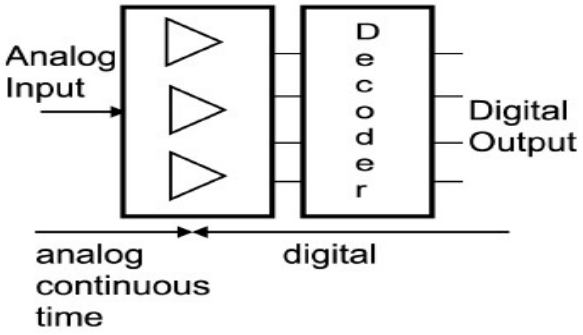
Fine is waiting for the Coarse (MSBs) – need S/H
How to partition ? 10 bit can use 31 comparators for Coarse and 32 for fine = 63 instead of 1024
Or 63 for coarse (6 bit) and 15 for fine ?

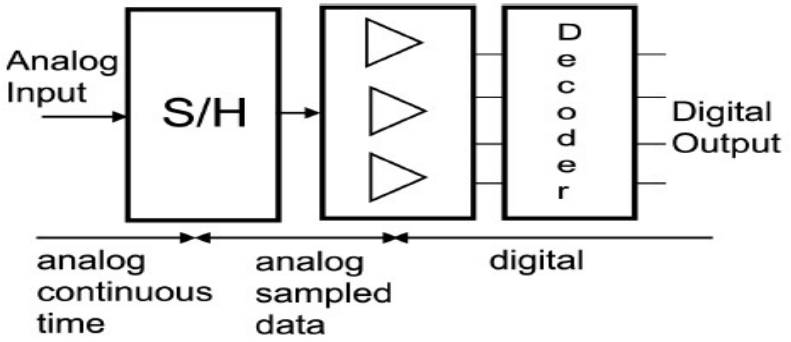
Summary: : Sub-ranging ADCs

- Power efficient
  - Two low resolution ADCs operating in a pipeline manner
- Reduced speed
  - Throughput can be still very high
- T&H is inevitable
  - The most critical component in the architecture
  - Loading is relaxed
- Residue generation
  - Needs M+N bit accuracy
- Interleaving is possible
- State of FOM is around 0.5pJ/conv



SH Versus clocked flash

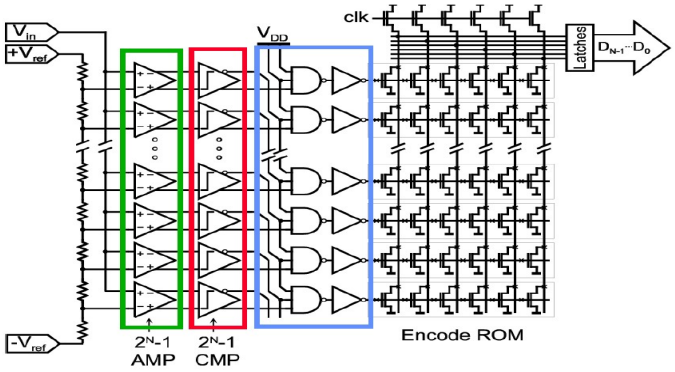




Source: KU Leuven

SH will draw 20-40% more power

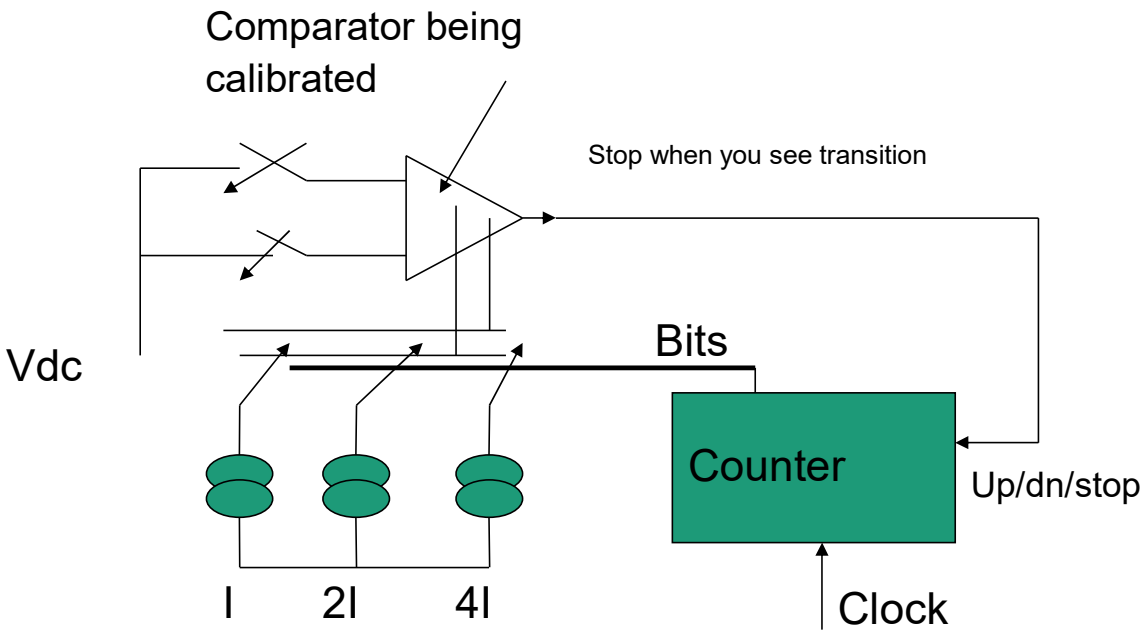
Flash architecture with digital corrections 1GHz/6 bits



Avantages :
Remove sample and hold – make clocking harder
Use comparators as sample and hold
Use pre gain comparator – Option
Error correction logic
ROM Grey encoder
Now task is on the clock to be accurate to all comparators

Offset Cancellation/reduction

Select 7I for maximum offset possible



Source: KU Leuven

Alternative offset cancellation

Easy to do in start up.

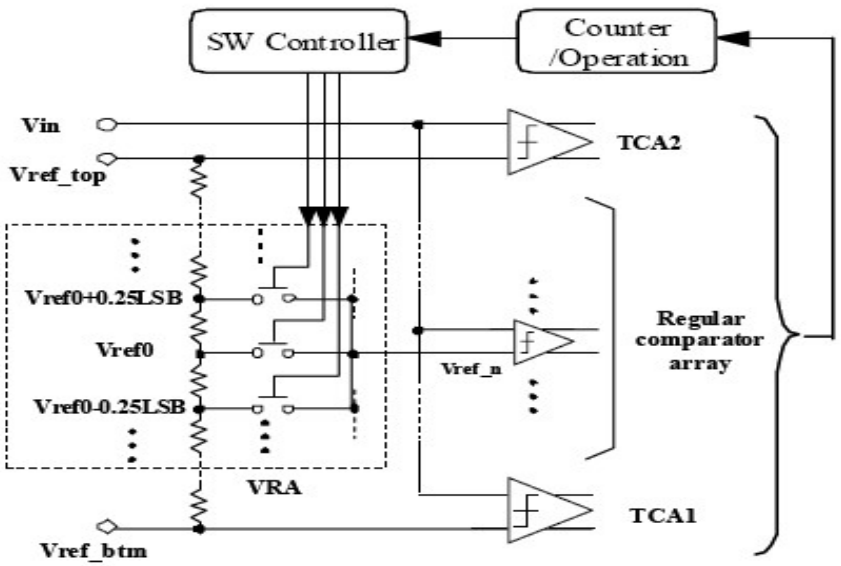


Figure 2: Architecture of offset cancel circuit.

Offset Calibrating Comparator Array for 1.2-V, 6-bit, 4-Gsample/s Flash ADCs using 0.13-um generic CMOS technology

Hiroyuki Okada, Yasuyuki Hashimoto,
Kohji Sakata, Toshiro Tsukada, Koichiro Ishibashi

We can go wild with good ideas:

Find offset connect comparator to different point on the ladder

Add small DAC to each comparator find trip point (Feed back)- last foil.

Remember the offset in digital code and offset the digital information

E N D lect 06