Welcome to
046188 Winter semester 2012
Mixed Signal Electronic Circuits
Instructor: Dr. M. Moyal

Lecture 06

DIGITAL TO ANALOG CONVERTERS

Transfer Function
DAC architectures/Examples
Calibrations

www.gigalogchip.com

Agenda

Transfer Function
DAC architectures
DAC Example
Calibrations

Transfer Function

DAC Basics: D/A conversion does not change the Spectrum of the input signal

Equation (Binary weighted DAC)

Example
A 4 bit DAC having n=4 bits will have 4 digital inputs from 0000 to 1111. (0-15)

Vout (Fscale) = Vref(1/16) x [B0 x1 + B1 x (2) + B2 x (4) + B3 x (8)]. = 15/16 x Vref

Can also be called “multiplying dac”
B’s is a digital code, it is assumed a 0 value or a 1 value (digital codes)

Vref is a reference set by design to control the output range (supply range is the limitation, ~Vdd-0.6)

The minimum step is assume when B0=1 all other B’s are 0! Is the Least significant bit (LSB).

Transfer Function (TF)

A n bit DAC will have the following expression
n is the resolution

n bit converter (DAC)

$$V_{out} = \left[B_0 \cdot 2^0 + B_1 2^1 + B_2 2^2 + \cdots + B_{n-1} 2^{n-1}\right] \cdot \alpha$$

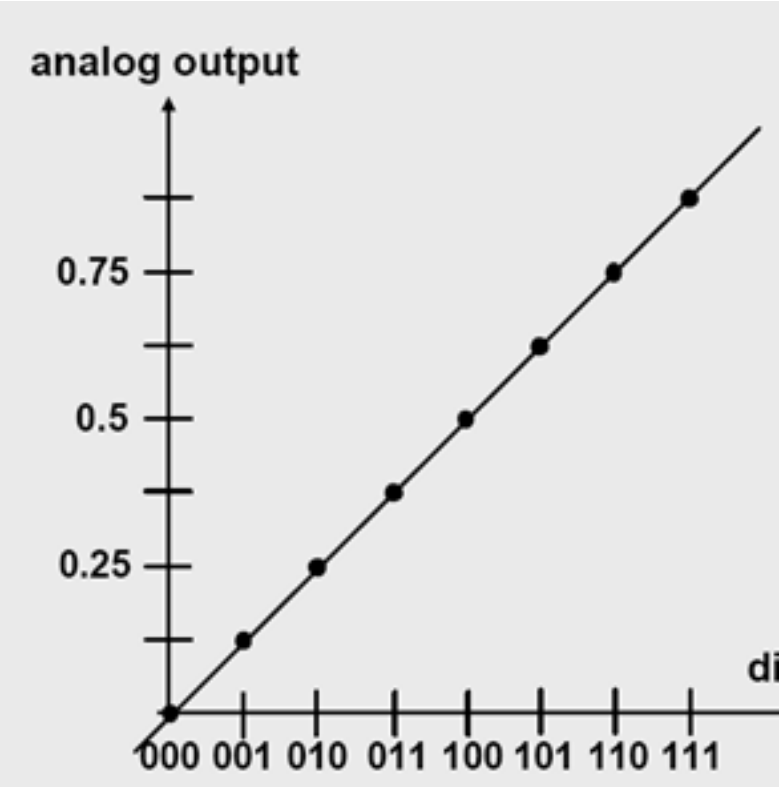
$$\alpha = \frac{V_{REF}}{2^n}, \text{ or } \frac{V_{FS}}{2^n}.$$

$$V_{out} = \sum_{m=0}^{n-1} \left[B_m 2^m\right] \cdot \frac{V_{REF}}{2^n}$$

B_m ∋ are codes, 0 or 1

Bo – is the lsb digital control
Bn-1 – is the MSB digital control
We set Vref, limited by process maximum range

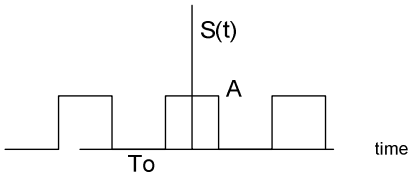
Ideal TF plot

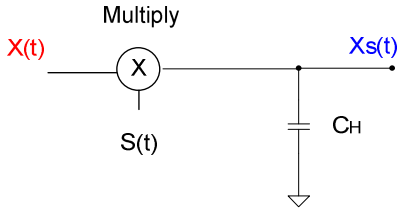


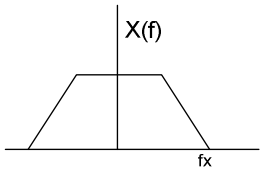
Digital code

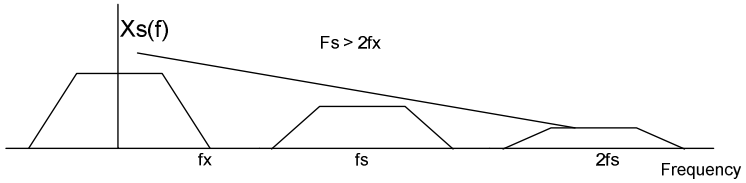
Output = Digital Code x Vref (analog)
Multiplication of analog value by Digital Fraction
Fraction multiplication is done using Matched resistors, Current, or Capacitors

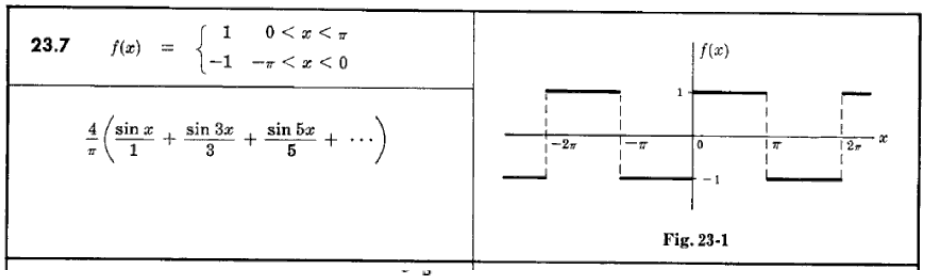
Misc..Frequency domain in sampling

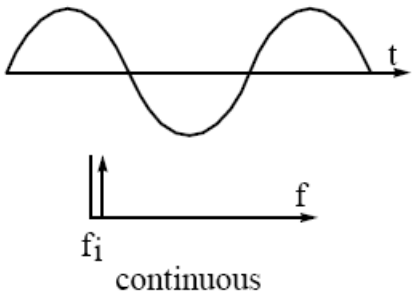


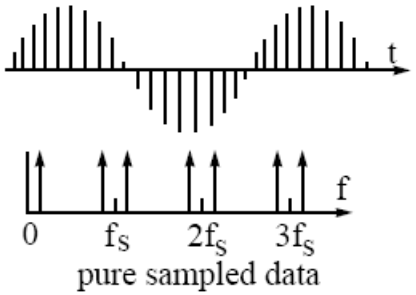


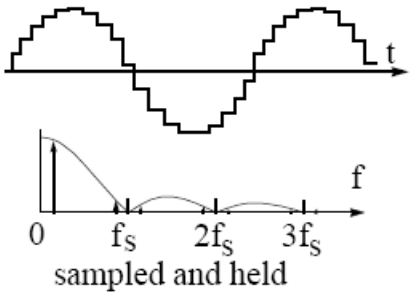












$$C_x(n f_0) = \frac{1}{T_0}\int_{-T/2}^{T/2} s(t)\, e^{-j2\pi n f_0 T}$$

$$|C_x(n f_0)| = \frac{1}{T_0}\int A\, e^{-jn\pi f_0 t}\, dt = A f_0 \tau \frac{\sin(\pi n f_0 \tau)}{\pi n f_0 \tau}$$

$$s(t) = C_0 + \sum_{n=1}^{\infty} 2 C_n \cos(n\omega_0 t)$$

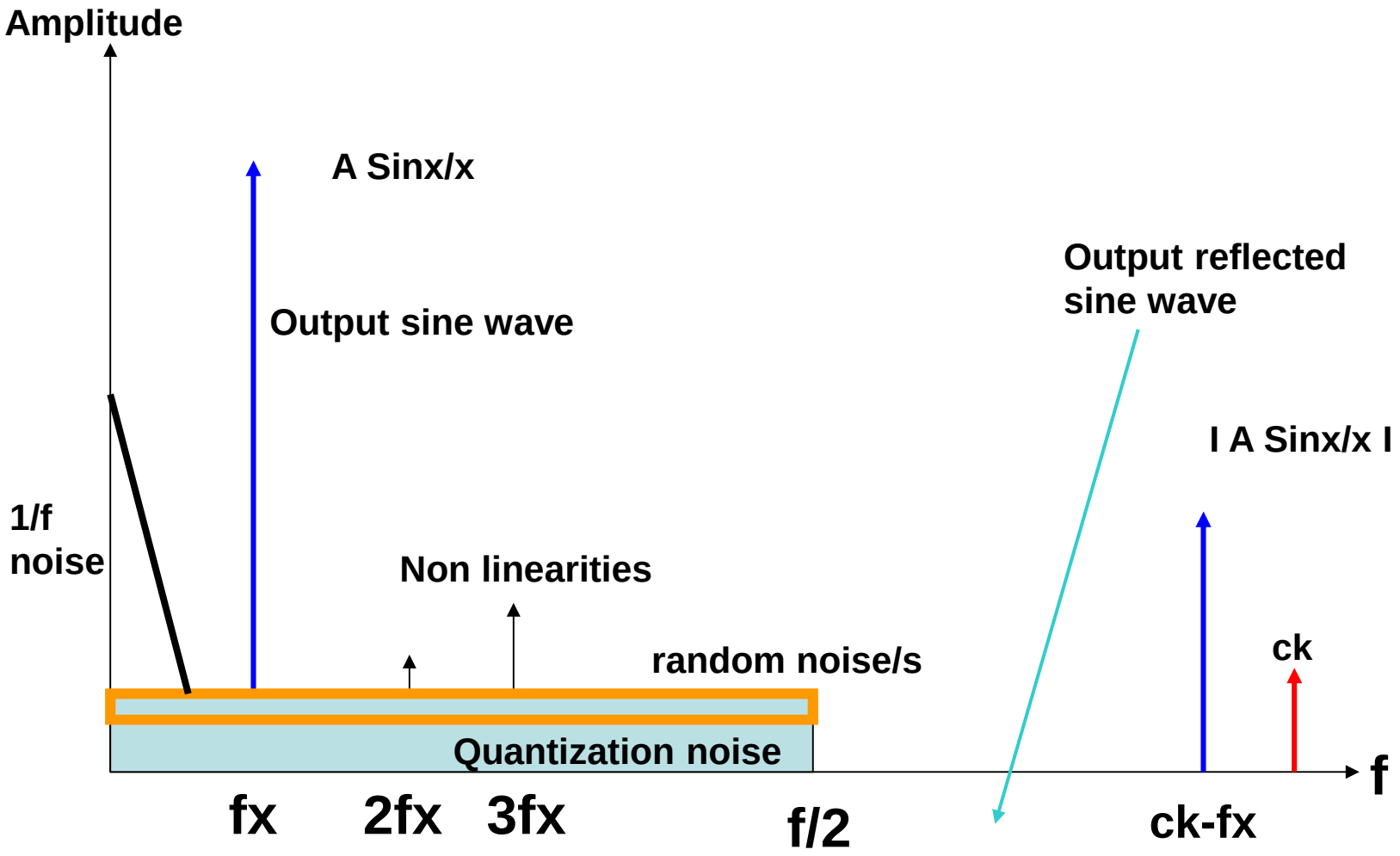
$$C_0 = \tau / T_0$$

$$C_n = A f_0 \tau \frac{\sin(\pi n f_0 \tau)}{\pi n f_0}$$

$$X(f) = S(f) \cdot X(f) = C_0 X(f) + 2C_1 X(f)\cdot\cos(\omega_s t) + 2C_2 X(f)\cos(2\omega_s t)$$

$$= C_0 X(f) + C_1 X[f \mp f_s] + C_2 X[f \mp 2f_s] + C_3 X[f \mp 3f_s] \cdots$$

DAC output: Frequency Domain – sine response no analog filter



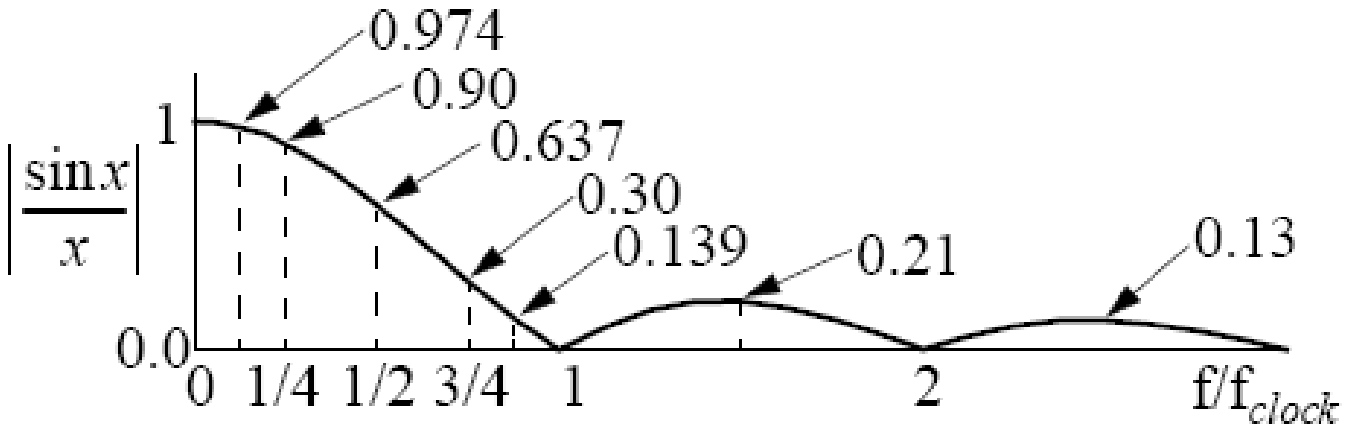
ISinx/xI means what !

Example:

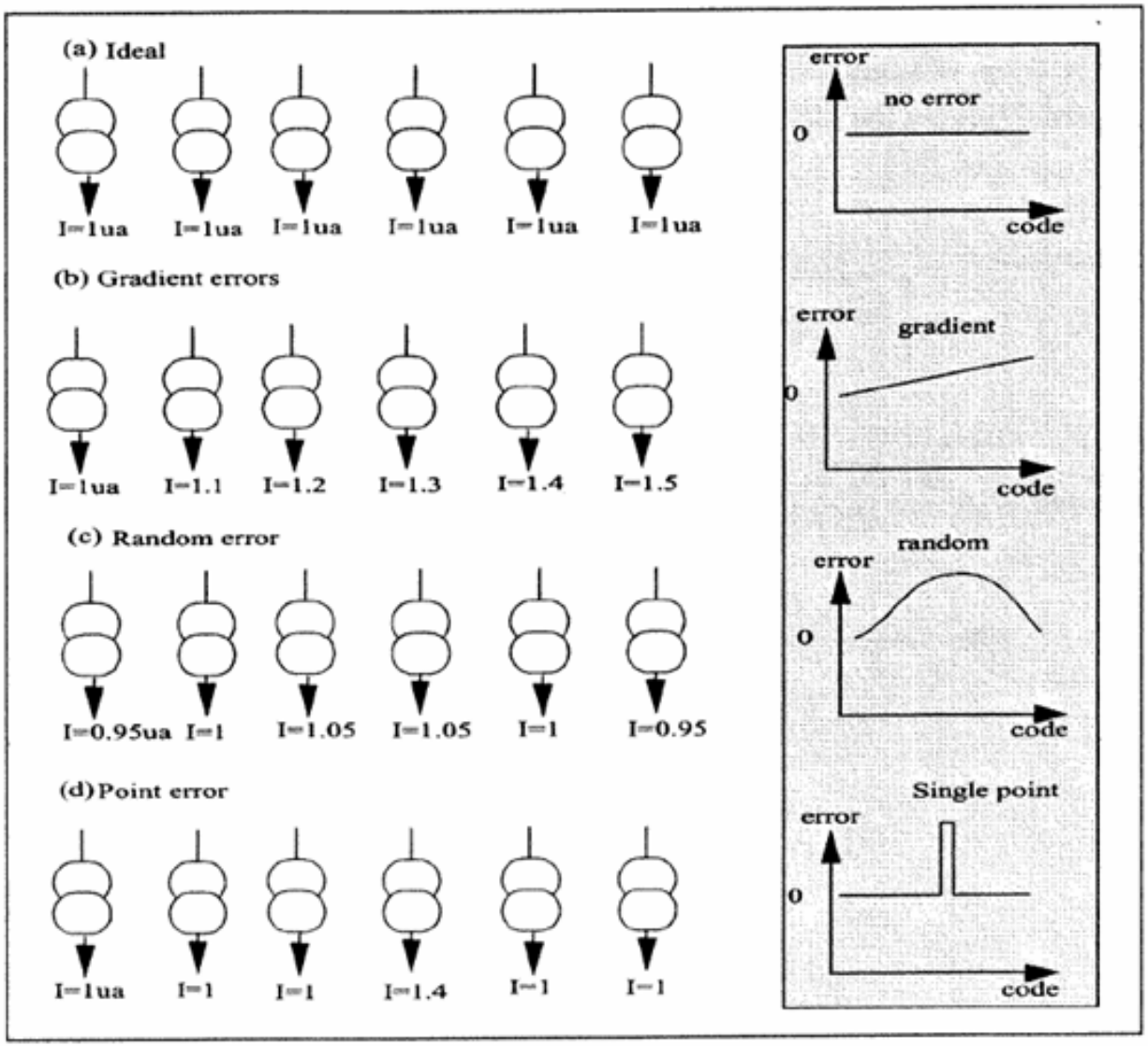
If fin lies at ¼ fs ! (fs=1MHz and fin=250KHz)

Pi x ¾ = 135 deg.

Sin(135) / 3.14x3/4 = 0.707/2.355=0.3

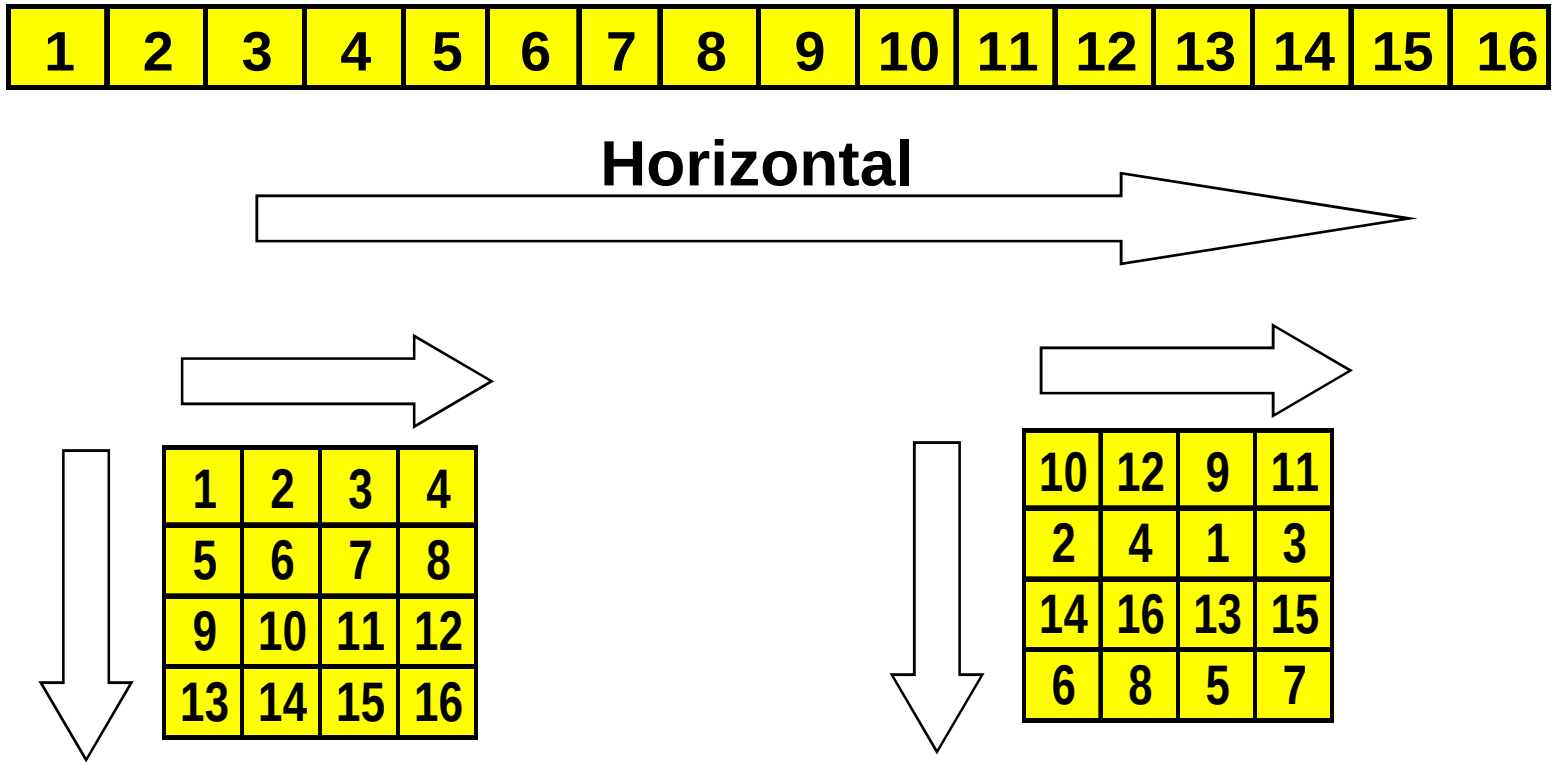


Type of mis-matches- I sources



a) No error b) Gradient c) Random d) Single point

Thermometer unit placement architecture: Gradient affect

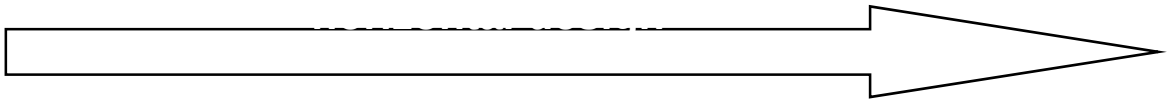


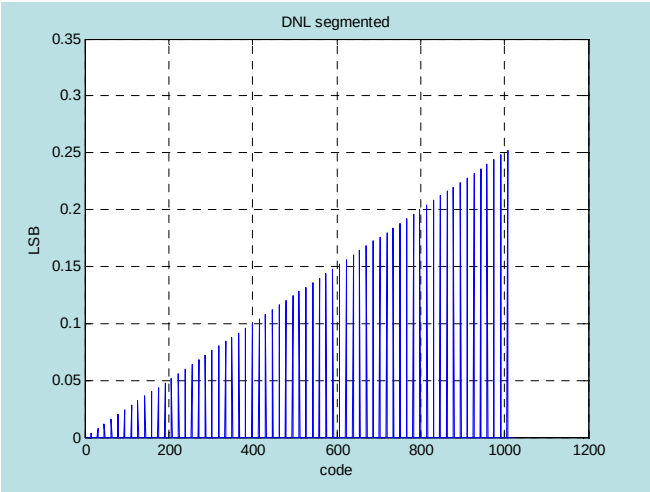
Horizontal/Vertical

Shufle design

horizontal unit placement

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

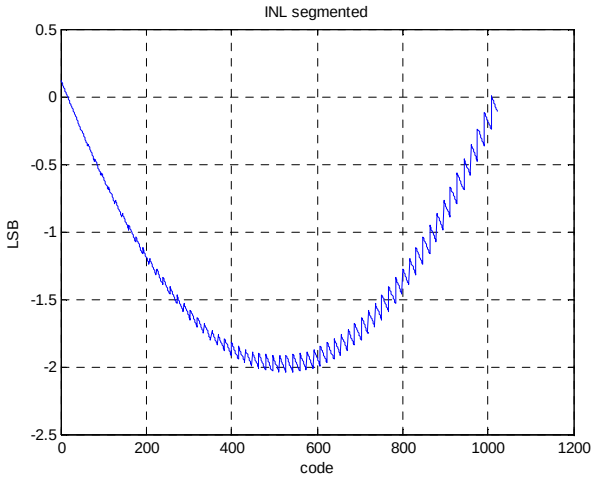




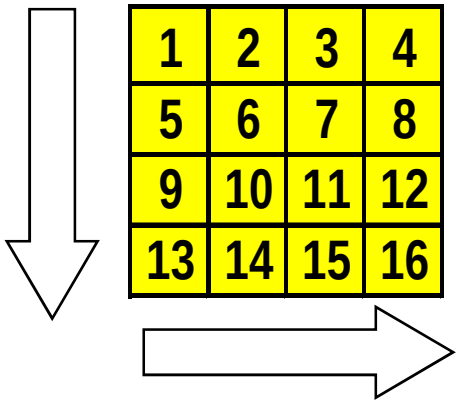
DNL

Min-max=large..

INL

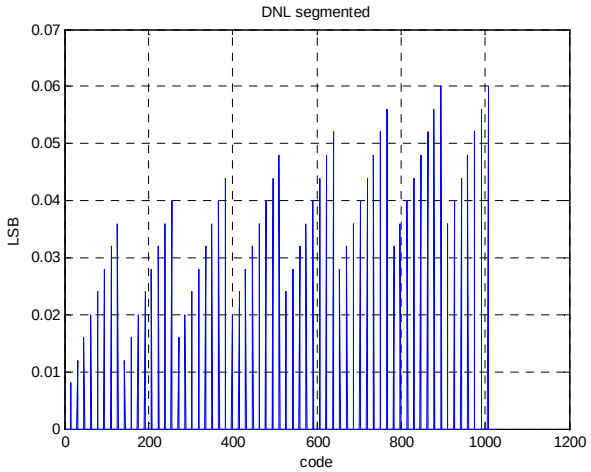


Horizontal/Vertical unit placement

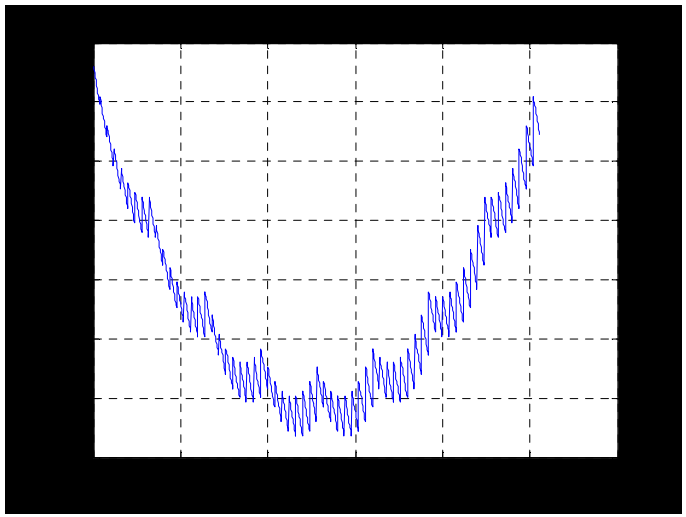


Min-max=~0.27lsb

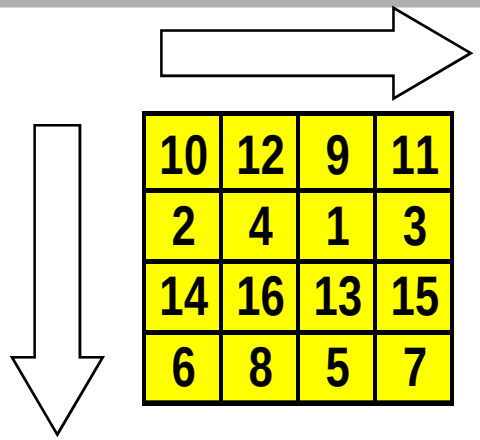
DNL



INL



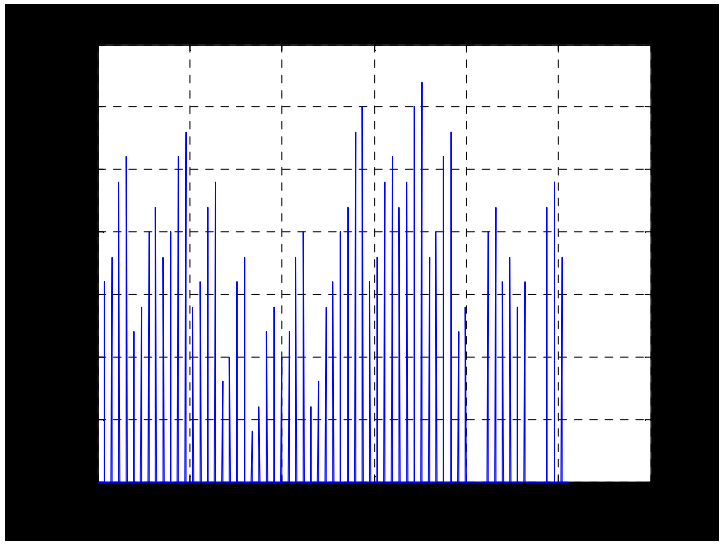
Shuffle unit placement



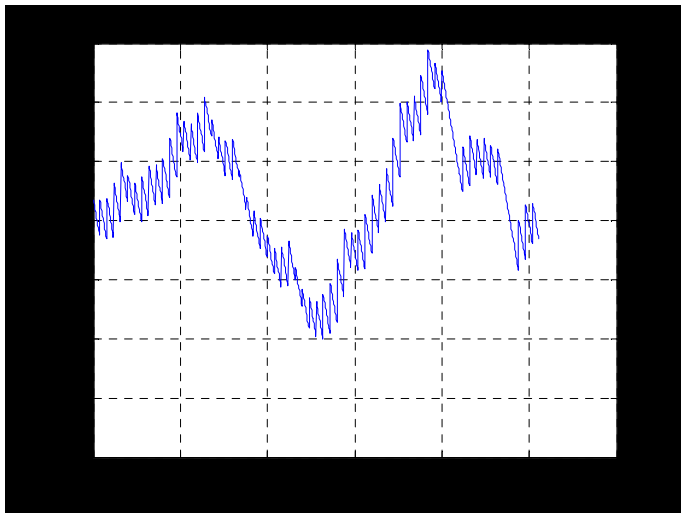
10	12	9	11
2	4	1	3
14	16	13	15
6	8	5	7

Min-max=~0.25lsb

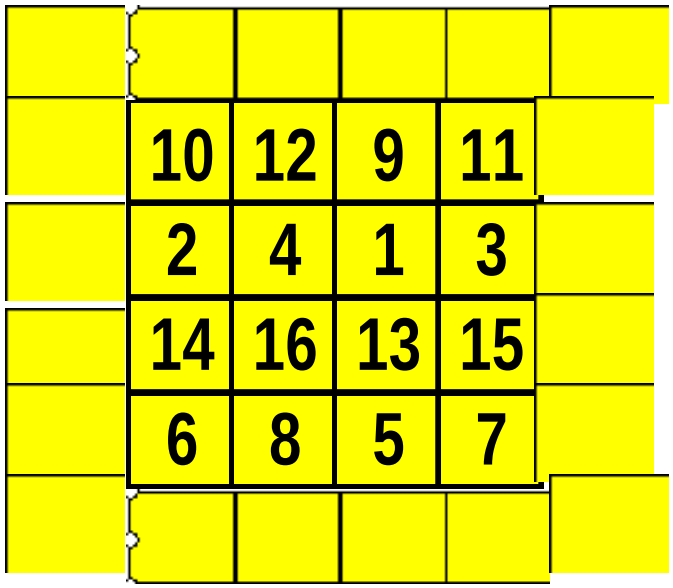
DNL



INL



dummies

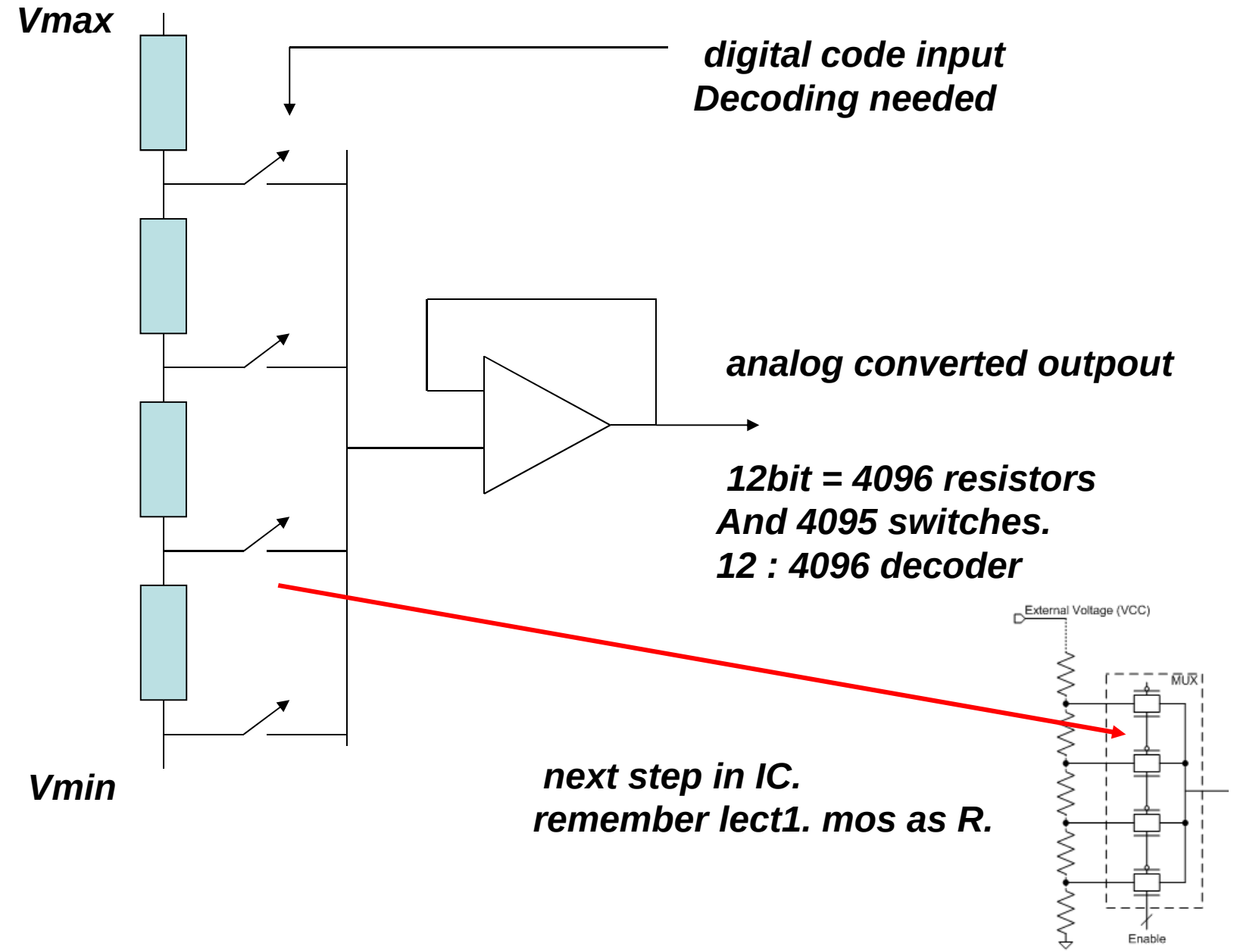


Keep background of edge unit identical
Some goes to the extreem of 2 rows

DACs Architectures

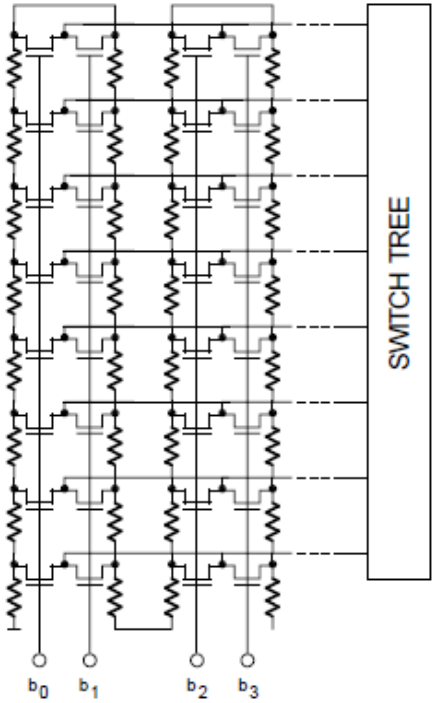
Voltage mode: R Ladder and R-String DAC
The Basic R-2R DAC
R and I DAC
C DAC
Current (steering) DAC

Resistor-String DAC- basics



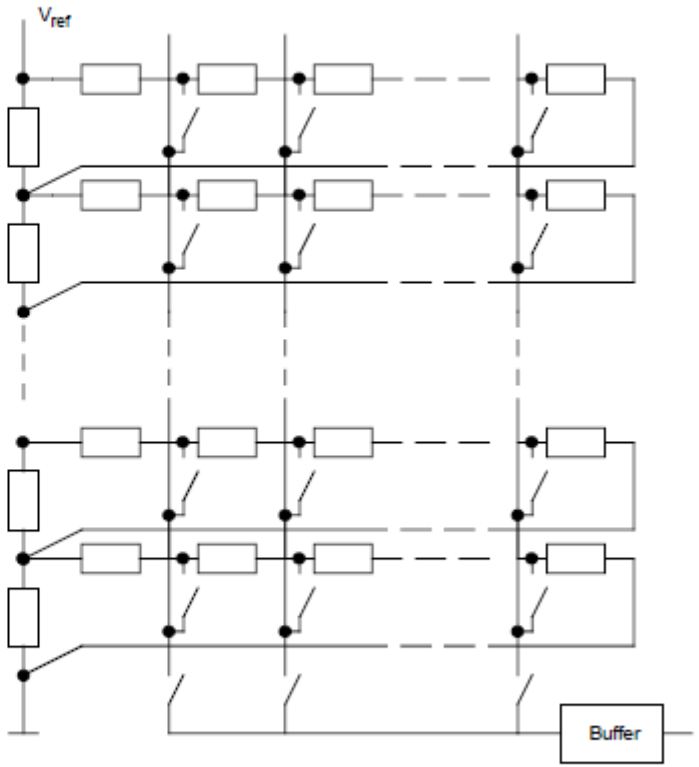
RESISTIVE DIVIDER D/A CONVERTERS

- Folded resistive string
- Parallel selection of 8 different voltage taps
- Tree of switches to select one of the 8 voltage taps
- Features
  - ☺ Intrinsically monotonic
  - ☹ Corner resistors difficult to implement
  - ☺ Compact layout

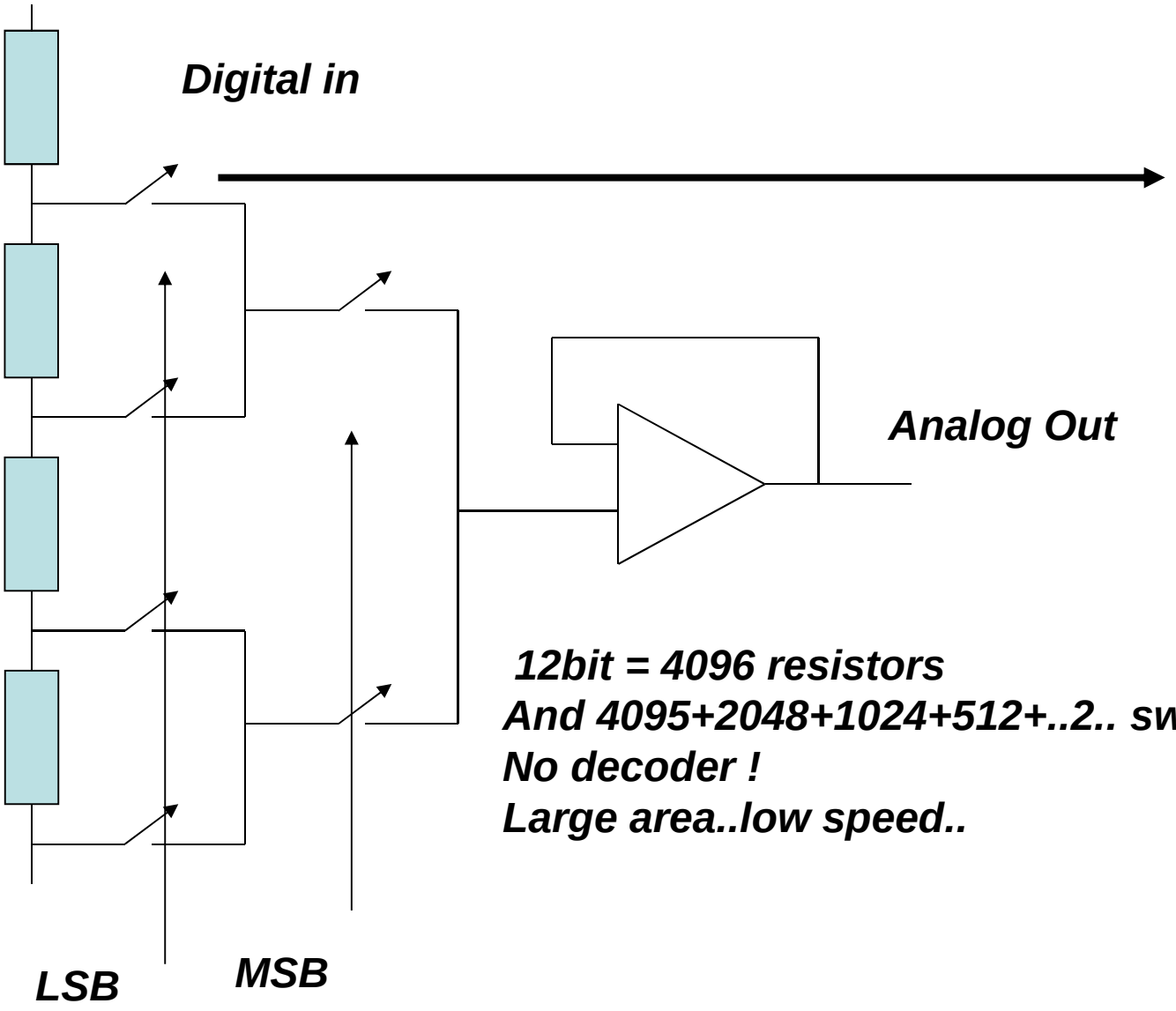


RESISTIVE DIVIDER D/A CONVERTERS

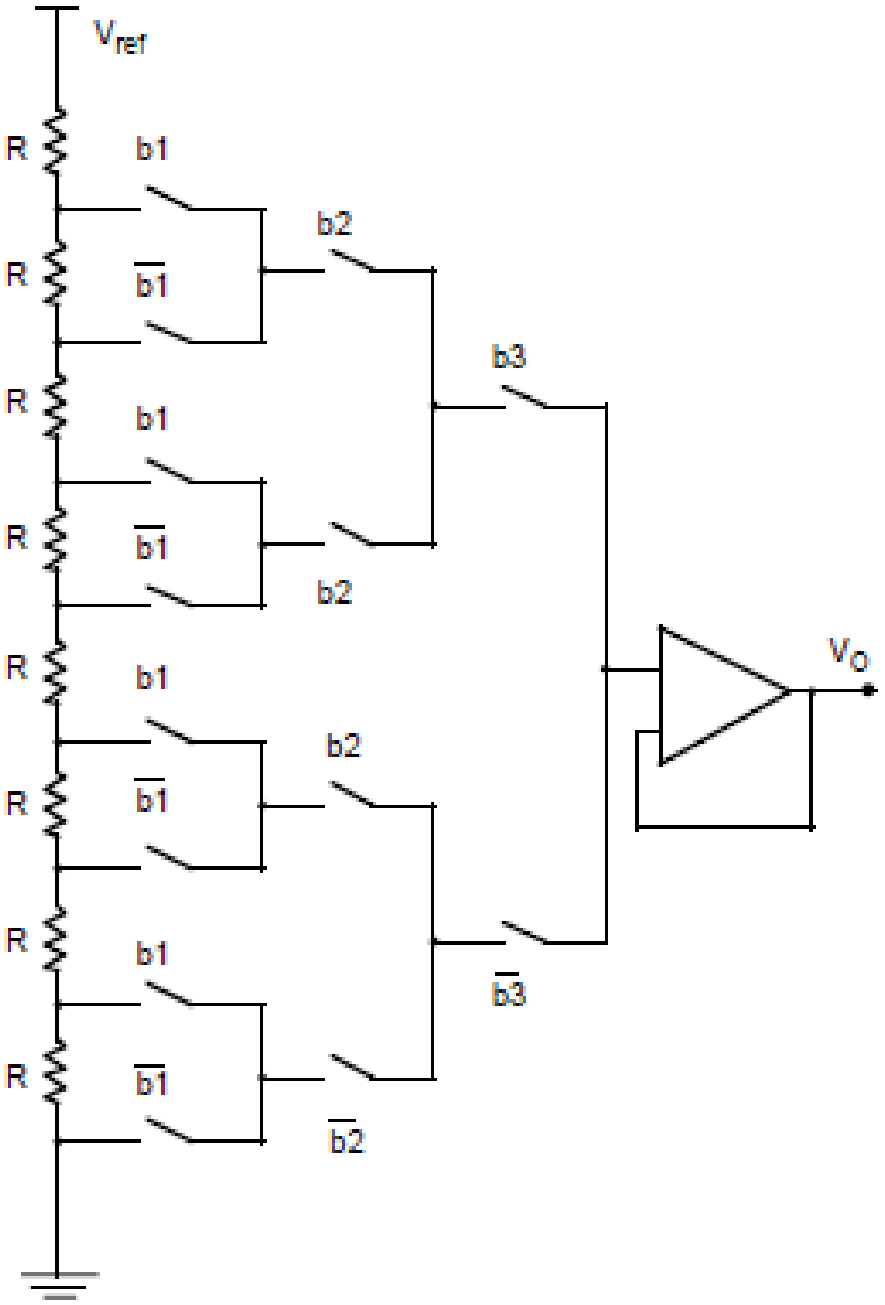
- Resistor matrix divides the reference voltage (XY selection)
- Output buffer required
- Features
  - ☺ High speed
  - ☺ Intrinsically monotonic
  - ☺ Up to 10 bits of resolution
  - ☹ Limitations due to the output buffer



Resistor DAC- basics decoder build in

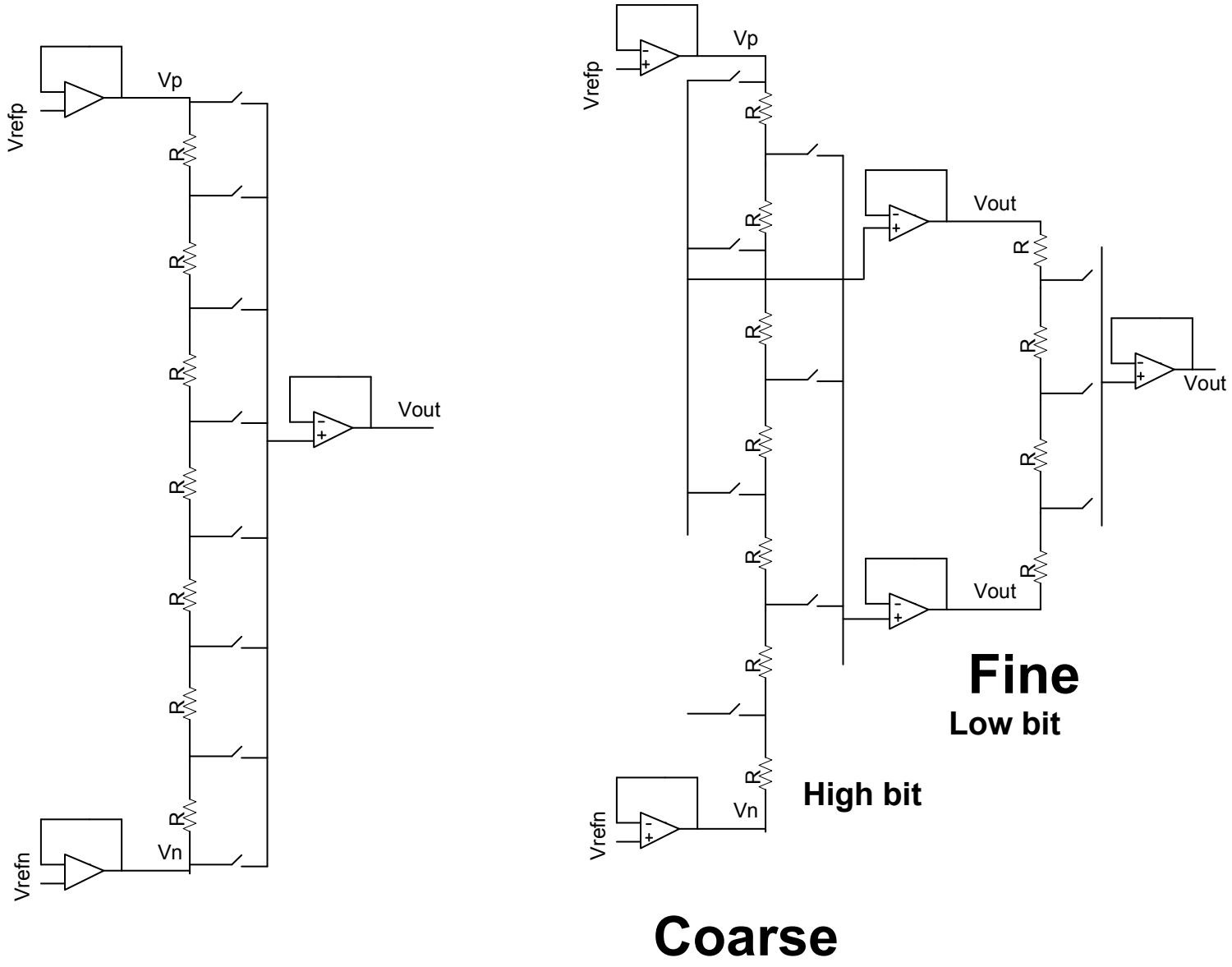


12bit = 4096 resistors
And 4095+2048+1024+512+..2.. switches.
No decoder !
Large area..low speed..



- The reference voltage is divided by a string of equal resistors
- A particular voltage tap is selected with a tree of switches
- The input impedance of the buffer is very high
- Features
  - ☺ Intrinsically monotonic
  - ☹ Sensitive to the buffer offset
  - ☹ Delay due to several switches in series

Voltage mode: R Ladder and R-String DAC



Voltage mode: R Ladder and R-String DAC- Equations

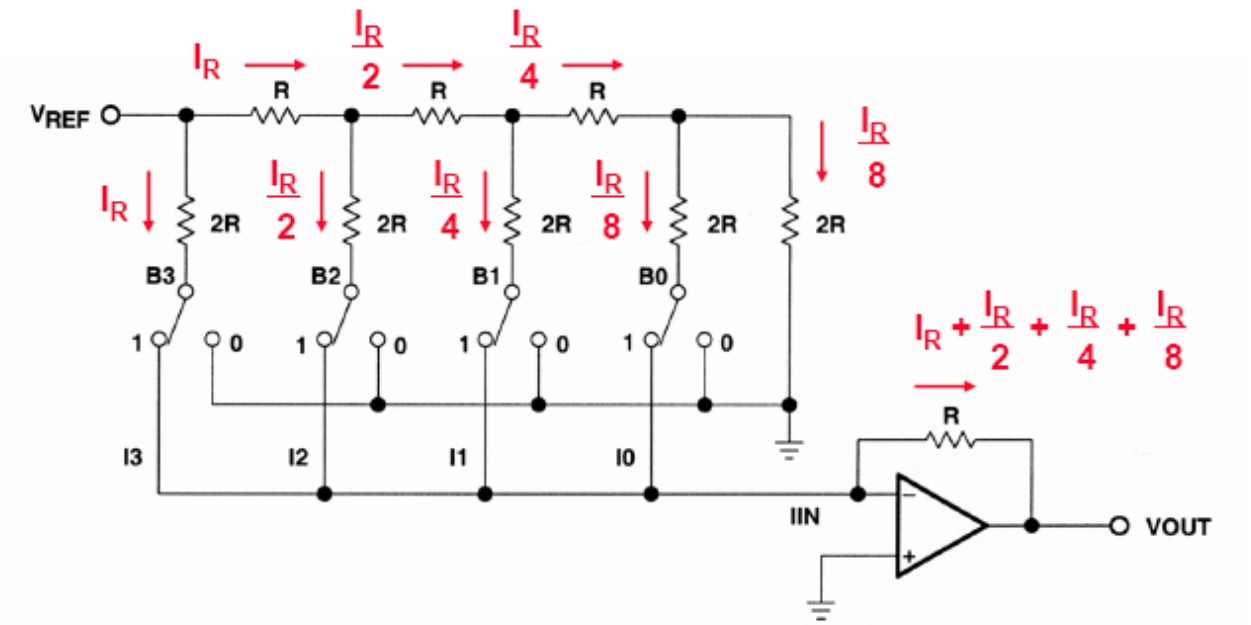
R string - Easy to implement in CMOS, “large” die size (In use up 8-10b)
A switch and resistor, digital selection, decoding, can be done with switch tree.

Multiple R-String allow increase in resolution (**keeping monotonic**)
With only doubling the R string. (Holloway 84)
Need only 2N+1 resistors not 2 to the power of N.

Speed is limited by amplifier input capacitance switch resistance and opamp BW
Op1 op2, and op3 offset is a draw back

THE BASIC R-2R DAC

R-2R DAC

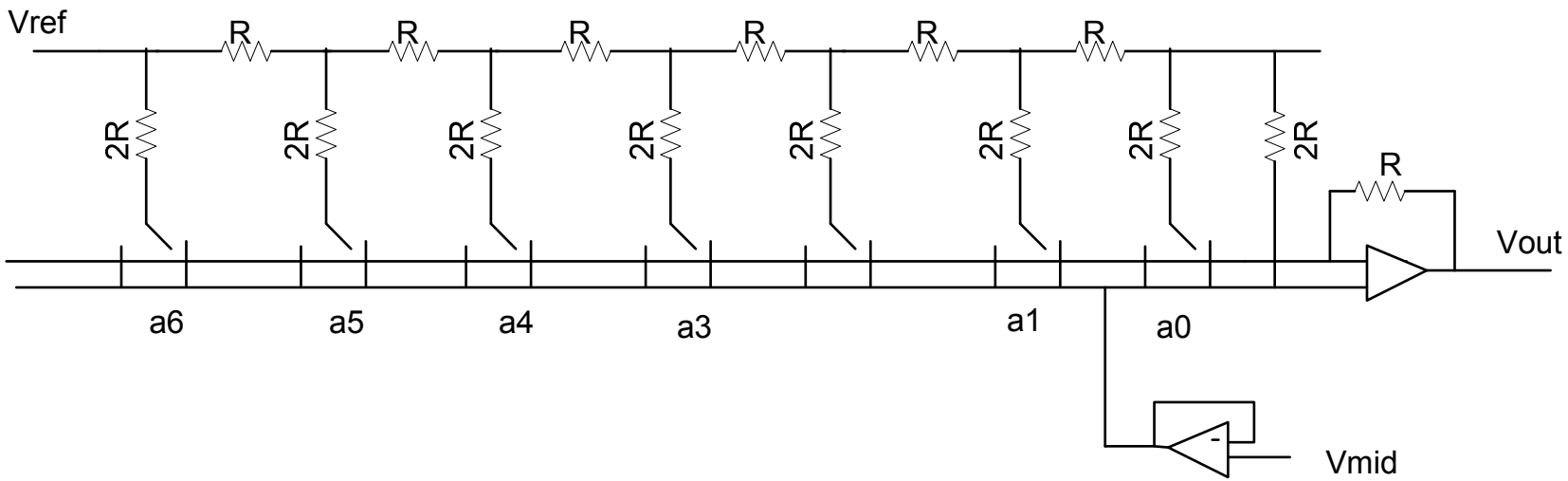


Smaller area in Resistors !

Willy Sansen 10-05 2013

Motivation: lower area, 12b=25 resistors

No guaranteed monotonic, bad offset sensitivity



Operation- unipolar output:

msb I(a6=H)= -Vref/2R only a6 goes H
I(a5=H)= -Vref/4R
lsb I(a0=H)= -Vref/128R only a0=H
I total = -Vref/R – Vref/128R all switches to out=H

Bipolar output possible with an extra amplifier and the use of Vmid

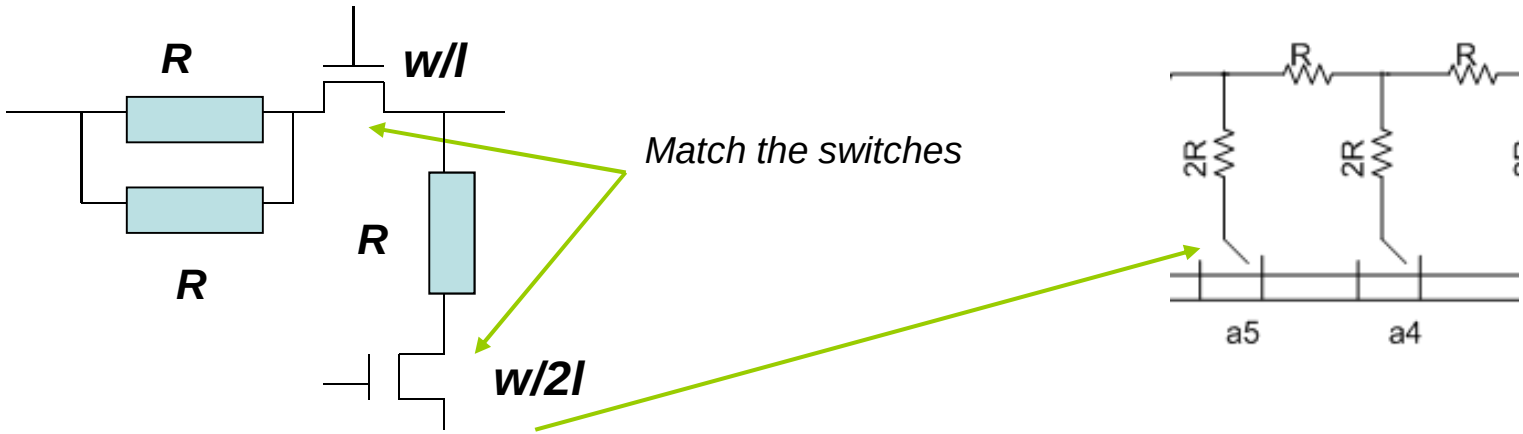
R-2R key issues

Very common architecture if thin film resistors are used (Cecil 74)
Area efficient- Easy to increase resolution R-2R per bit
Monotonic is not granted
INL and DNL are closely coupled
Relatively Slow

“rule of thumb” : Matching requirement for the n th bit in the i th bit

$$\Delta R < \frac{R}{2^{n-i}}$$

1) Switch resistance, Vgs voltage changes will effect mismatches



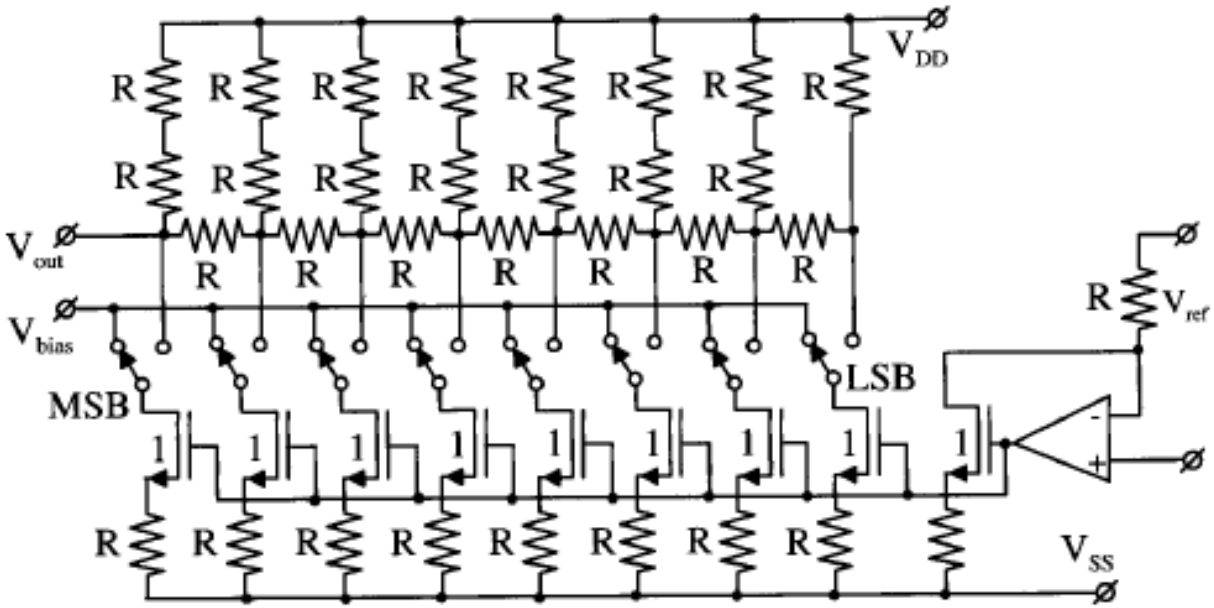
2) Problem: Output impedance changes and get multiplied by amplifier offset
Looking from the other side (opamp side) R looking back form
the amplifier vary with code.

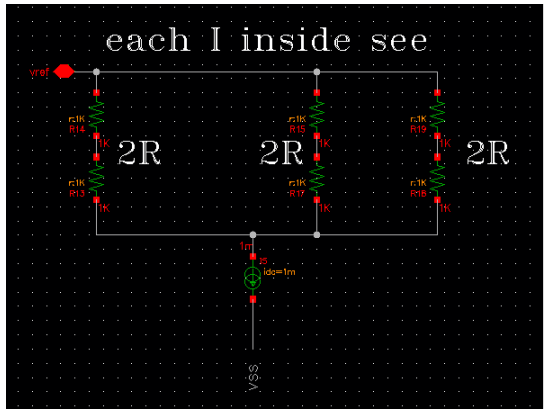
can we Fix the impedance issue

R-2R and I

Architectures for Nyquist High-Speed D/A converters:

- **R-2R ladder:**
  - Area is reduced compared with resistor string
  - Simple design: equal resistor R-2R blocks, switches and current sources
  - Fixed output impedance
  - Accuracy is limited by matching of resistors and current sources
  - Poor power efficiency

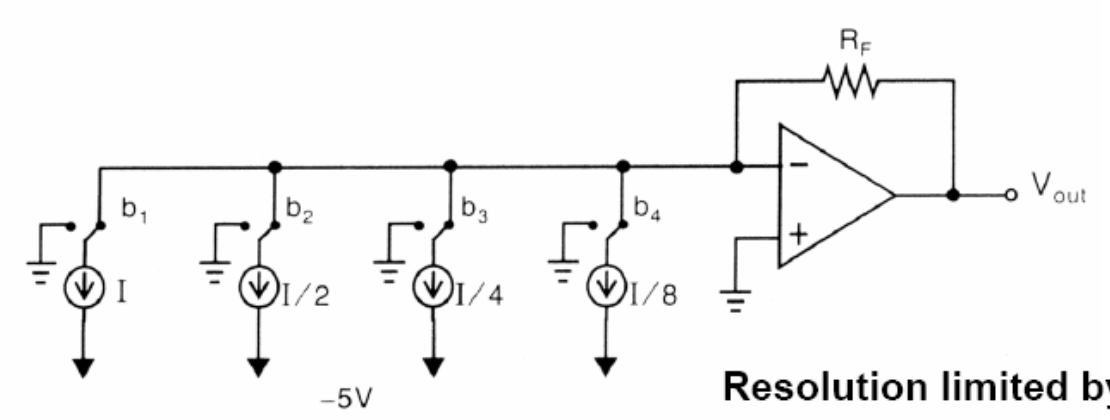




Source: R V Plasshe

Current DAC

4-bit Current steering DAC



Resolution limited by Mismatch in the Current sources !

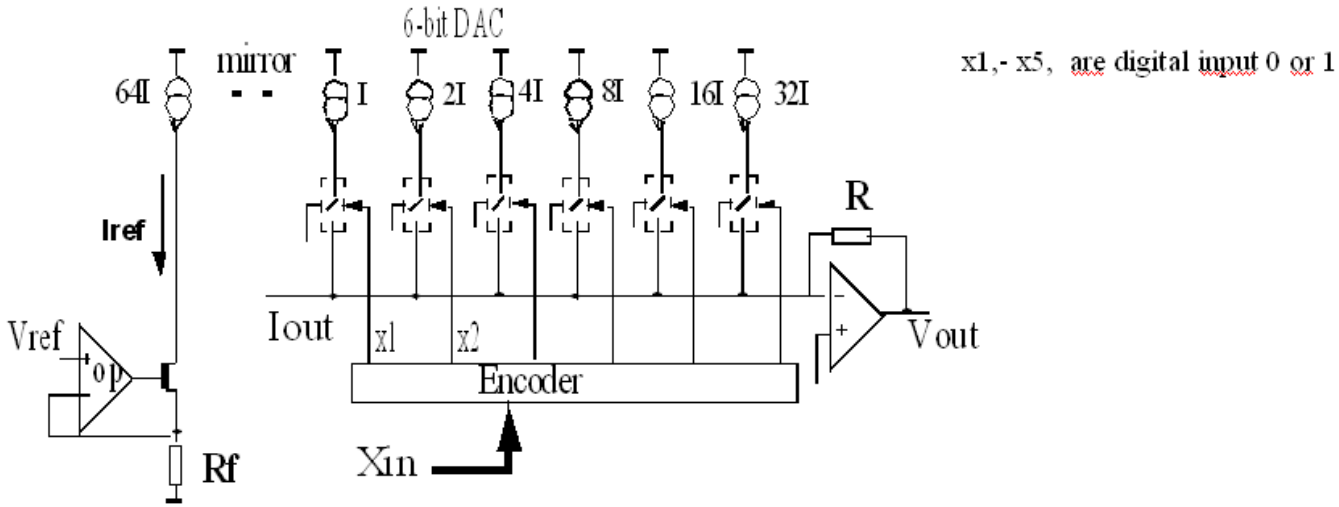
Glitches !

Willy Sansen 10-05 2015

Limit: Thermal/1/f Noise of Idac, opamp (gmin), and Rf.
Speed: Fast-- as opamp unity gain Band width.

I dac with reference

DAC Implementation



Vout = -Vref * (R / Rf*64)* (1x1+2x2+4x3+8x4+16x5+32x6)

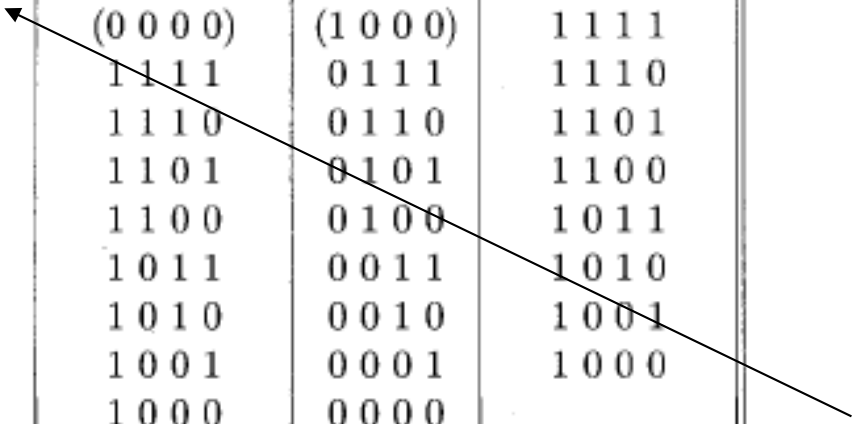
Iref is generated using op

Vout is only a function of code and Vref

Additonal objective (for future technology generations): Low operating voltage 1.8 V

Glitch control Coding schemes..:

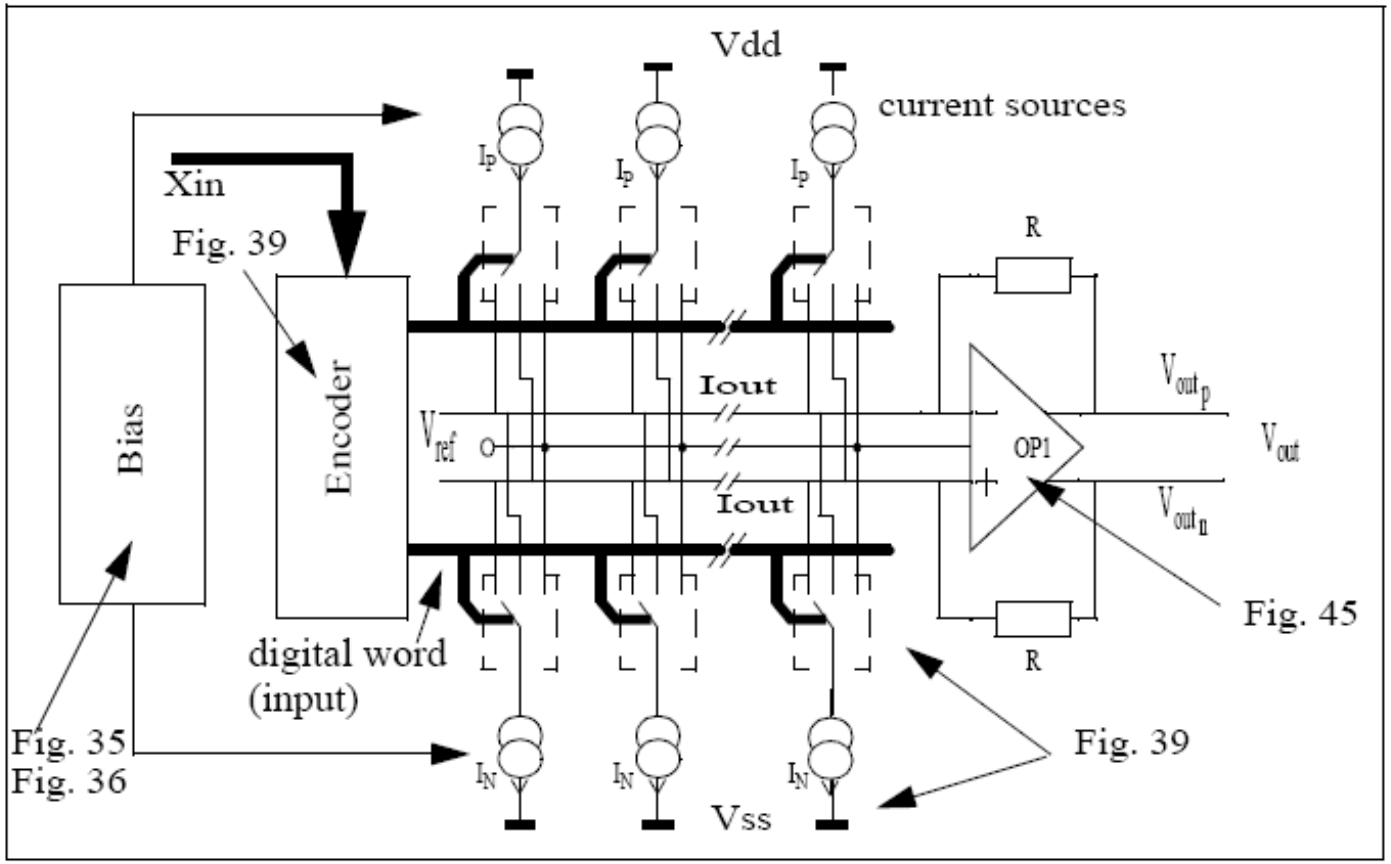
Number	Sign + Magnitude	Twos Complement	Offset Binary	Ones Complement
+7	0 1 1 1	0 1 1 1	1 1 1 1	0 1 1 1
+6	0 1 1 0	0 1 1 0	1 1 1 0	0 1 1 0
+5	0 1 0 1	0 1 0 1	1 1 0 1	0 1 0 1
+4	0 1 0 0	0 1 0 0	1 1 0 0	0 1 0 0
+3	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1
+2	0 0 1 0	0 0 1 0	1 0 1 0	0 0 1 0
+1	0 0 0 1	0 0 0 1	1 0 0 1	0 0 0 1
+0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
−0	1 0 0 0	(0 0 0 0)	(1 0 0 0)	1 1 1 1
−1	1 0 0 1	1 1 1 1	0 1 1 1	1 1 1 0
−2	1 0 1 0	1 1 1 0	0 1 1 0	1 1 0 1
−3	1 0 1 1	1 1 0 1	0 1 0 1	1 1 0 0
−4	1 1 0 0	1 1 0 0	0 1 0 0	1 0 1 1
−5	1 1 0 1	1 0 1 1	0 0 1 1	1 0 1 0
−6	1 1 1 0	1 0 1 0	0 0 1 0	1 0 0 1
−7	1 1 1 1	1 0 0 1	0 0 0 1	1 0 0 0
−8		1 0 0 0	0 0 0 0	



Good around +/-0

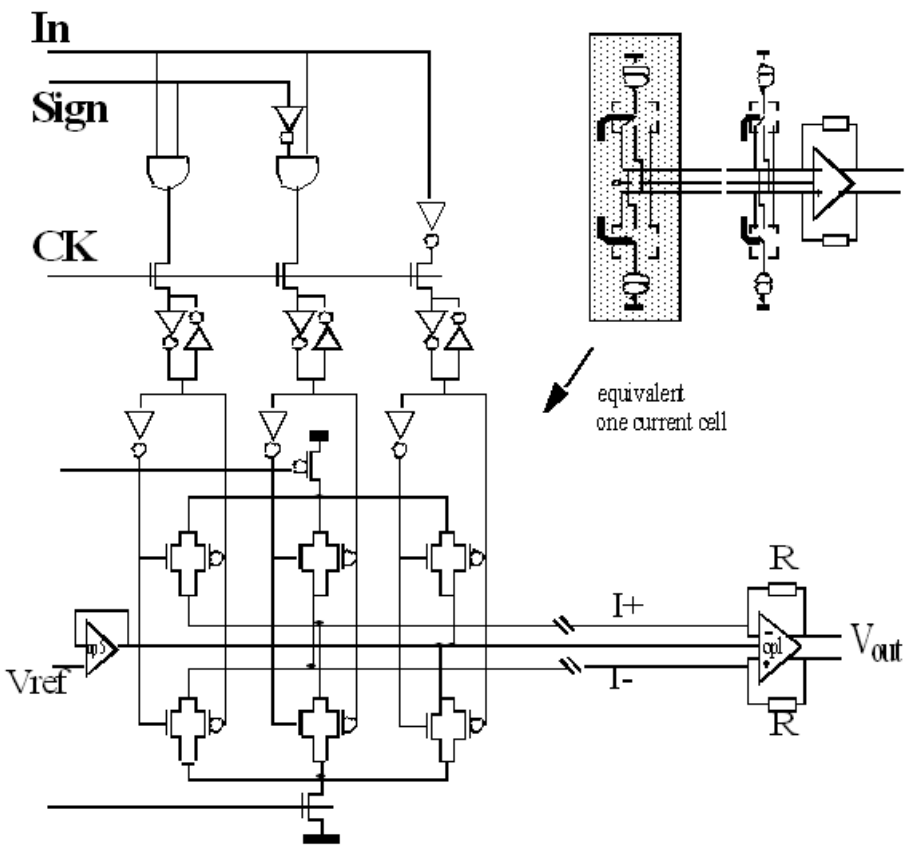
- **Offset Binary.** Obtained starting to encode from the most negative number.
- **Sign Magnitude.** The MSB represents the sign, the others the absolute value.
- **1's Complement.** Negative numbers are obtained complementing positive numbers.
- **2's Complement.** Obtained from the offset binary complementing the MSB; negative numbers equal to 1's complement plus one.

DAC Differential Architecture



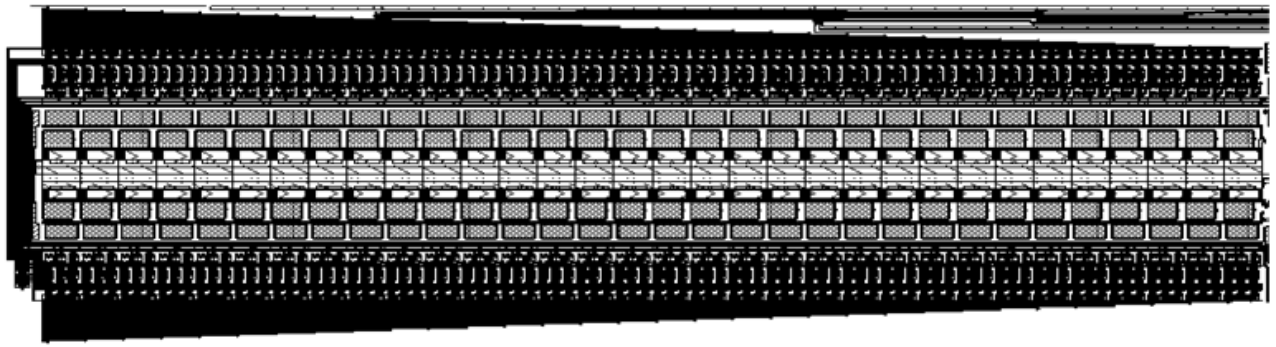
LSB Implementation

- 64 units
- **Sign** input is for current direction
- **CK** is to latch the data
- Example:
- if **In** = 0 , Vout=0



DAC Layout

- Hand layout to allow "shielding" of analog from digital
- Iout lines are in the middle
- Digital on the outside
- Area: Core < 0.6 mm^2 (total <1)



Measured Results

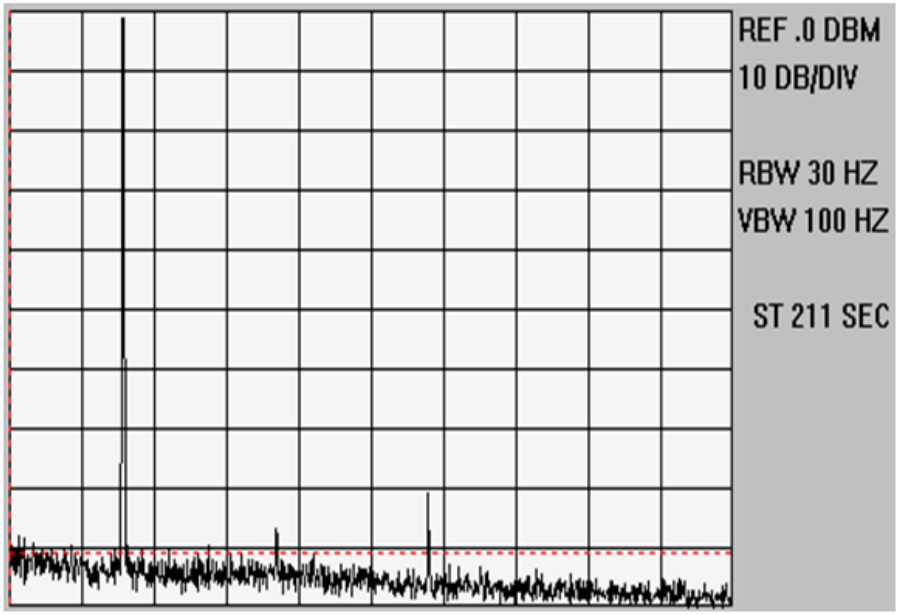
Transmitter Harmonic

WITHOUT DYNAMIC AVERAGING

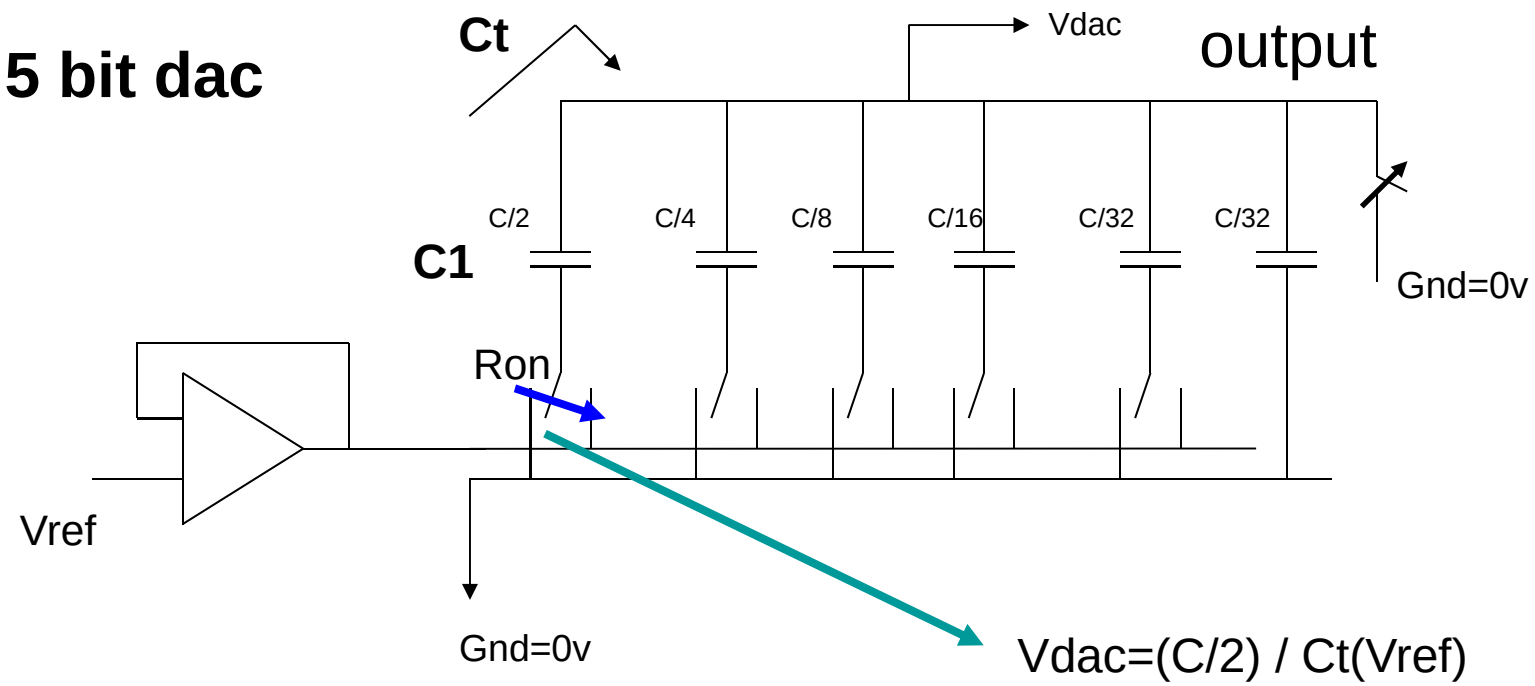
2rd Harmonic at - 87dB

3nd Harmonic at - 78dB

5th Harmonic at - 87dB



C DAC



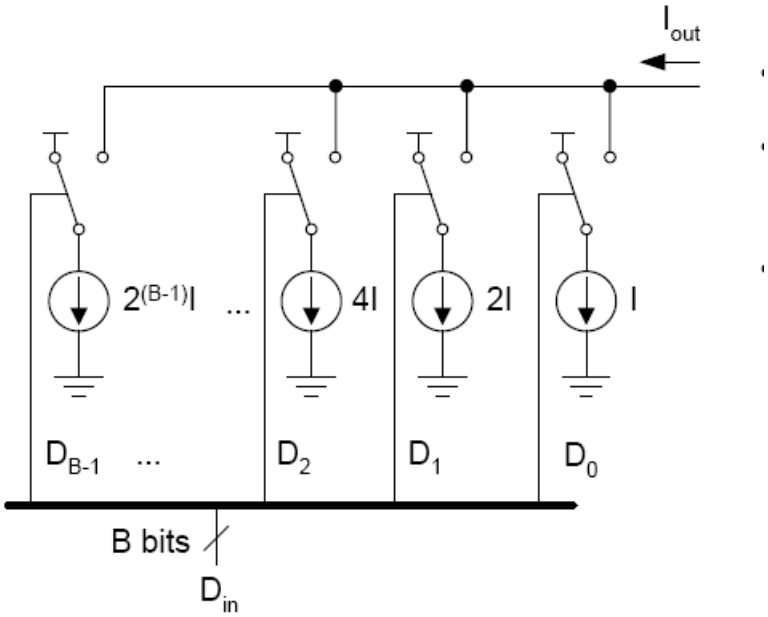
Switch every ½ cycle to 0 and re strart..

Output is valid only part of the time (switched) may need Hold switch
Matching of capacitors set the INL / DNL

Limit: Noise KT/C, glitches
Speed: Fast-- as Ron of switch, vref settling, and and C/2 n time constant.

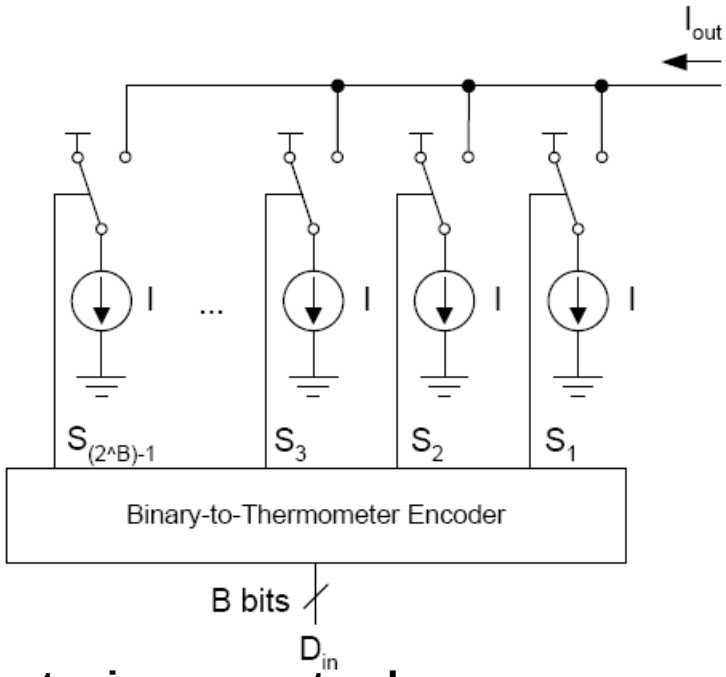
I dac - binary

I dac - thermometer



Could be non Monotonic- in transitions
Simple decoder

“best” for speed => Iout time constant



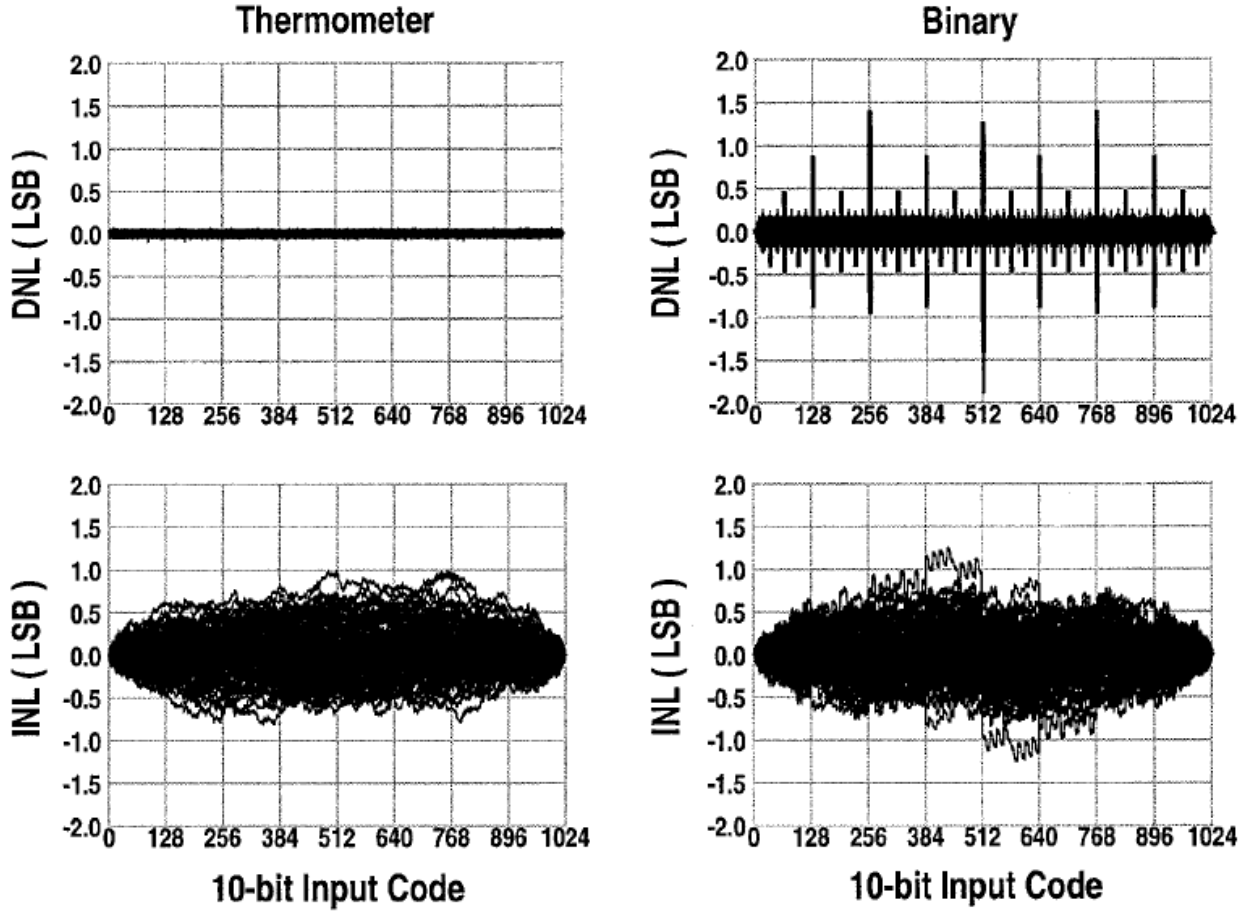
Monotonic- guaranteed

decoder complex
001 000000001
010 000000011
011 000000111 always one change
100 000001111

Source: B. Murmann Stanford

Binary Vs. Thermometer - mismatch

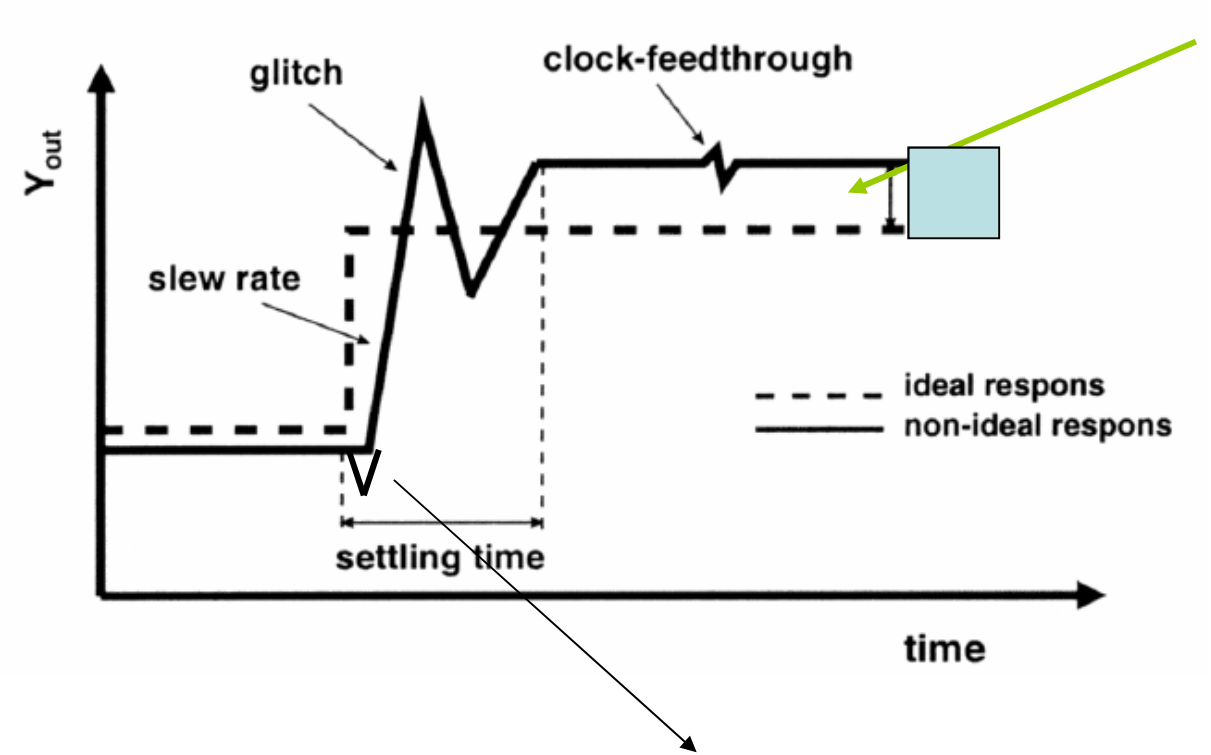
Source : JSCC IEEE 1998 Chi-Hung 10b 500Mhz



Matlab 1000 simulations
FOR THE SAME AREA
INL – THE SAME DNL – BIG DIFFERENE
Figure out the optimum place: how many binary bits and how many segmented bit

DAC Response

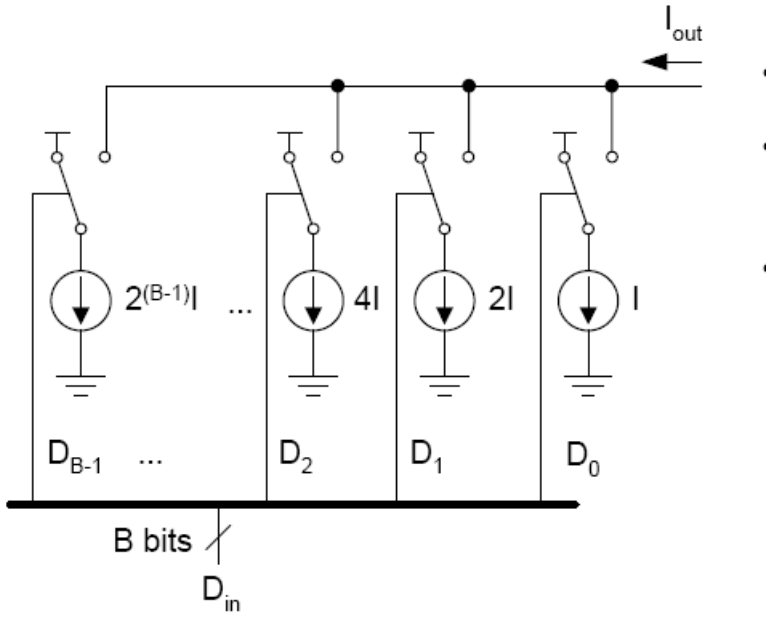
Inaccuracy/offset

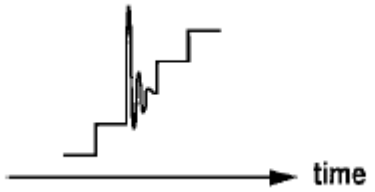


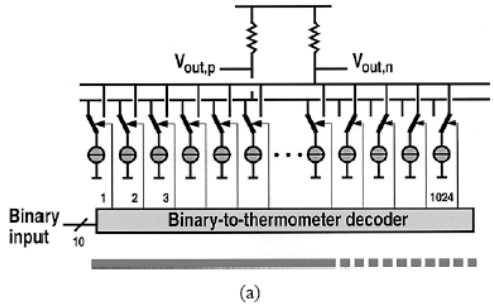
Capacitive charge

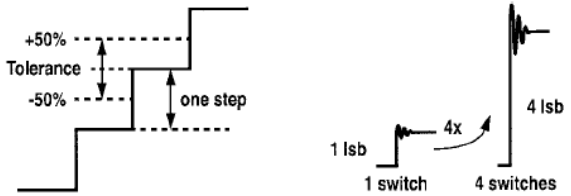
Partly Source: WilleSansen 2007

Glitches and INL in Binary dac



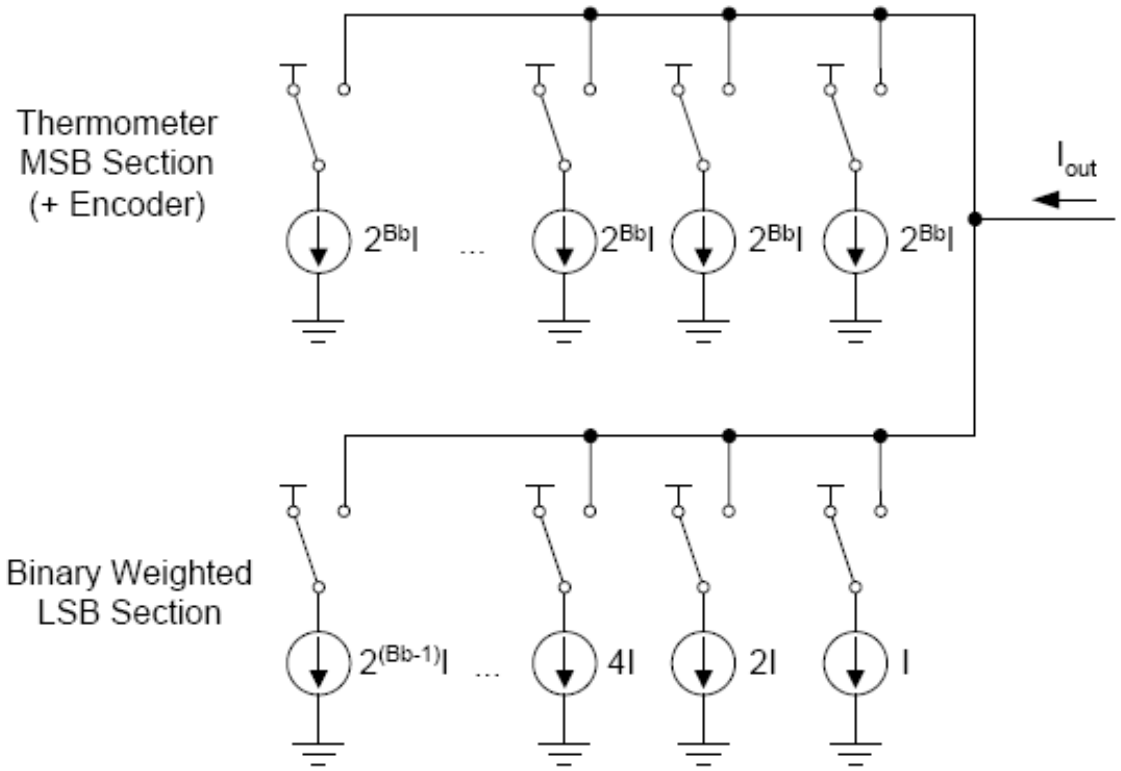






If the glitches scale with code (and capacitance is linear) – Linearity is good

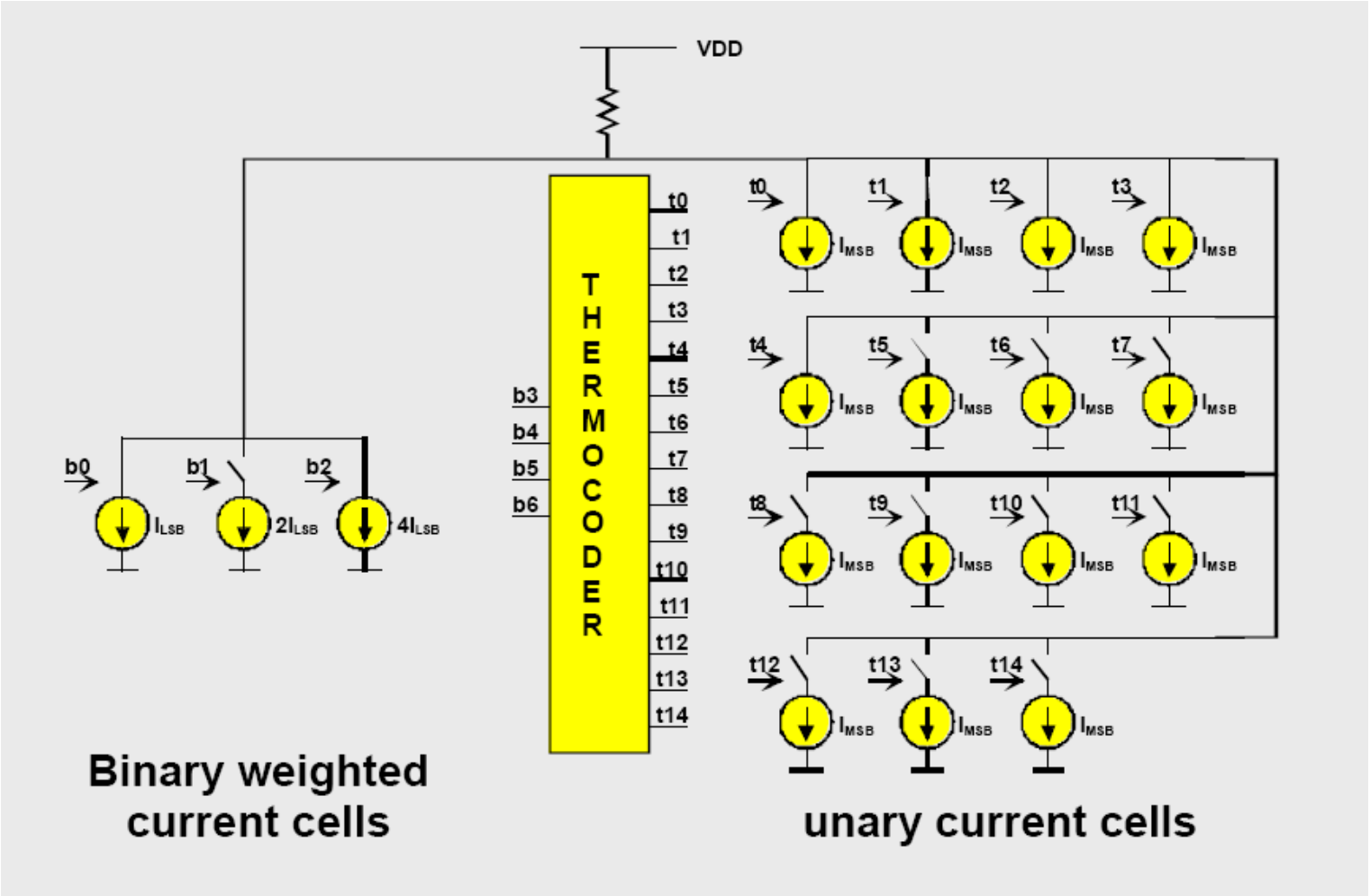
Combined I dac - segmented



- Binary weighted section with B_b bits
- Thermometer sectior with $B_t = B-B_b$ bits
- Typically $B_t \sim 4\ldots8$
- Reasonably small encoder
- Easier to achieve monotonicity

Source: B. Murmann Stanford

Current (steering) DAC- removed opamp

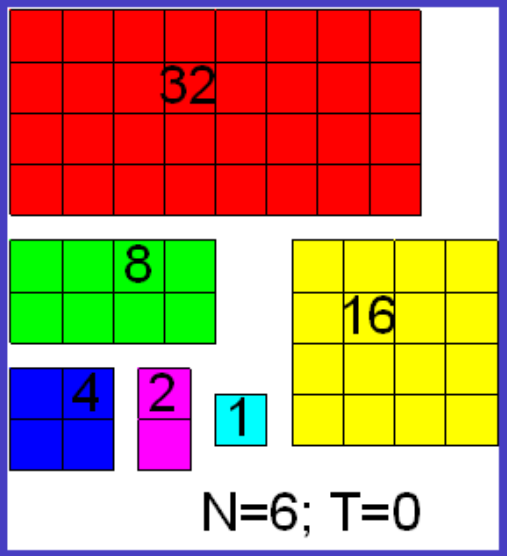


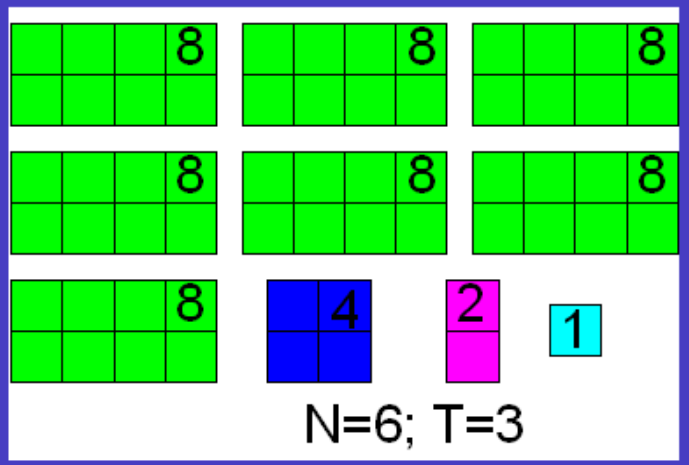
Source : G. Gielen, K.U.L Leuven

2 option of DAC arrangements

Prove DNL eq...

Segmented DAC INL DNL





$$\sigma_{INL} \approx \sqrt{2^{N-2}} \cdot \sigma_I < 0.5 \cdot LSB$$

$$\sigma_{DNL} \approx \sqrt{2^{N-T}} \cdot \sigma_I < 0.5 \cdot LSB$$

- DAC architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision

STATIC PERFORMANCE
In Current-Steering D/A Converters

DNL in binary D/A converters:

Worst case DNL for the midcode transition (MSB):

$$\sigma^2(\Delta I) = \sigma^2\left(2^{N-1}i_0 - \left(2^{N-1}-1\right)i_0\right) = \left(2^N - 1\right)\sigma^2(i_0) \Rightarrow$$

$$DNL^{\max} = \frac{\sigma(\Delta I)}{i_0} = \sqrt{2^N - 1}\,\frac{\sigma(i_0)}{i_0} \text{ in LSB units}$$

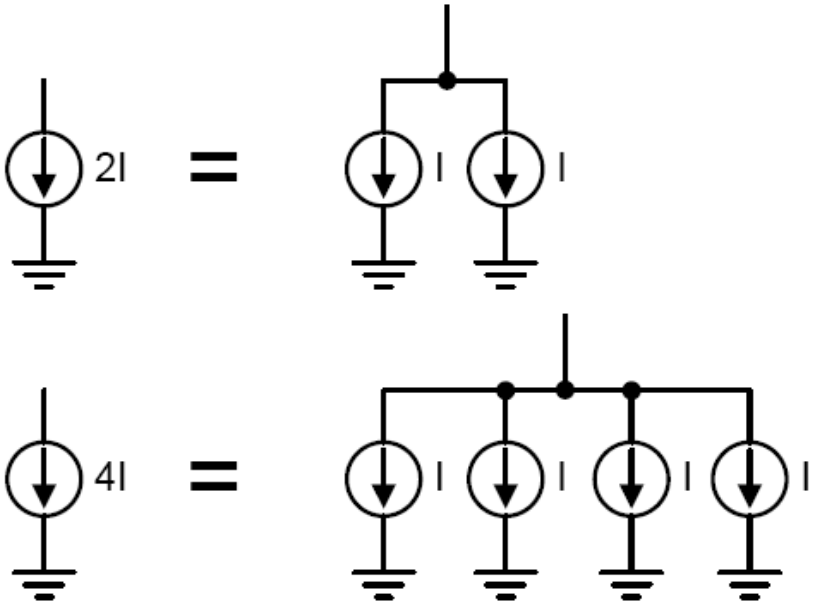
DNL in thermometric D/A converters:

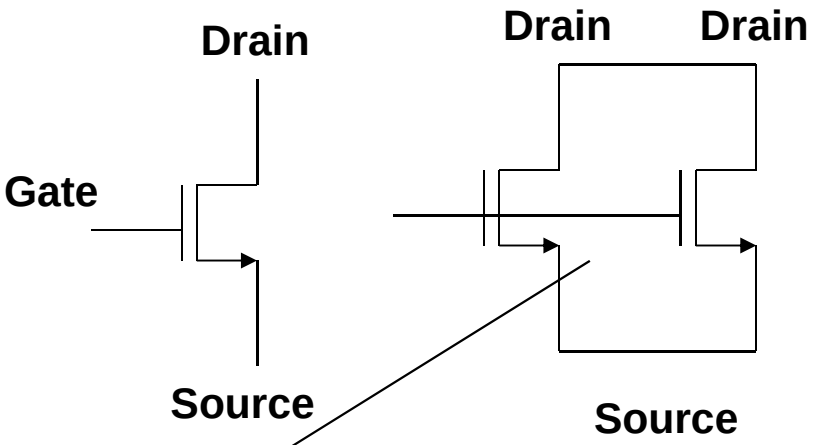
DNL limited by the LSB a single i_0 source is connoted or disconnected from adjacent code to code transitions:

$$DNL^{\max} = \frac{\sigma(\Delta I)}{i_0} = \frac{\sigma(i_0)}{i_0} \text{ in LSB units}$$

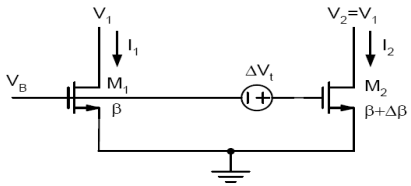
DNL < 0.5 LSB is guaranteed for as much as a 50% precision in the i_0 sources

Current source implementation





Mismatch in MOS Current Sources



$$\Delta I = I_1 - I_2 \cong -g_m \Delta V_t + I_1 \frac{\Delta\beta}{\beta}$$

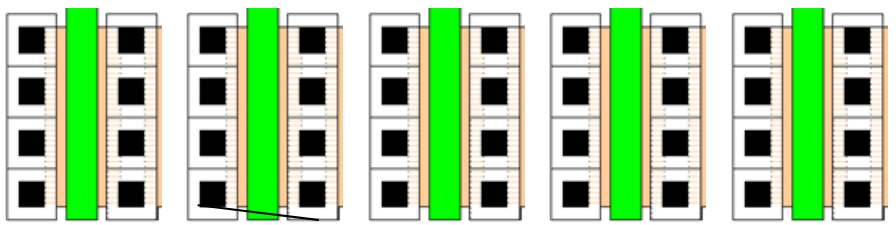
$$\frac{\Delta I}{I_1} \cong -\frac{g_m}{I_1}\Delta V_t + \frac{\Delta\beta}{\beta}$$

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} \qquad \sigma_{\frac{\Delta\beta}{\beta}} = \frac{A_\beta}{\sqrt{WL}}$$

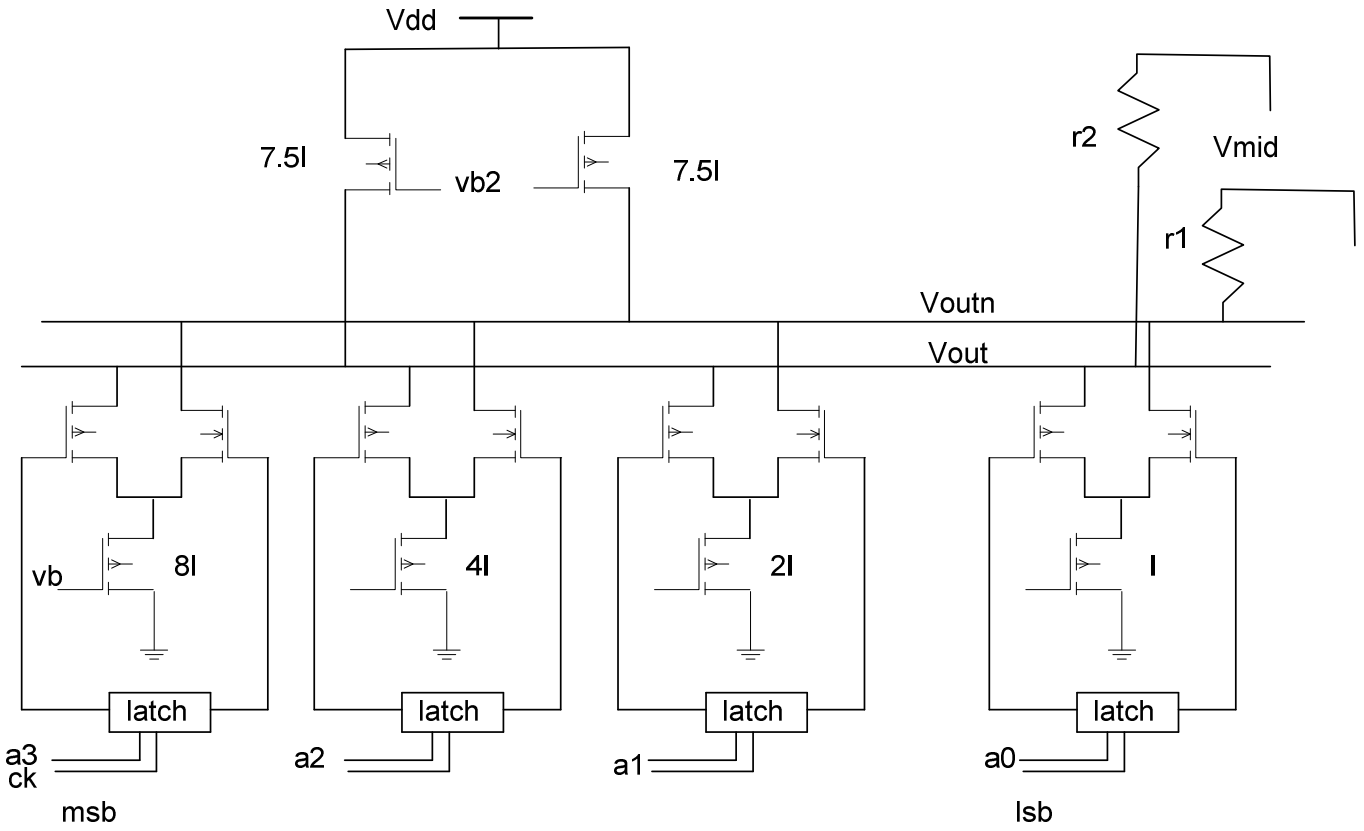
- Example
  - W=500μm, L=0.2μm, g_m/I_D=10S/A, A_{Vt}=5mV-μm, A_β=1%-μm

$$\sigma_{\frac{\Delta I}{I_1}} = \sqrt{\left(10\frac{S}{A}\cdot\frac{5mV}{10}\right)^2 + \left(\frac{1\%}{10}\right)^2} = \sqrt{(0.5\%)^2 + (0.1\%)^2} = 0.51\%$$

Layout



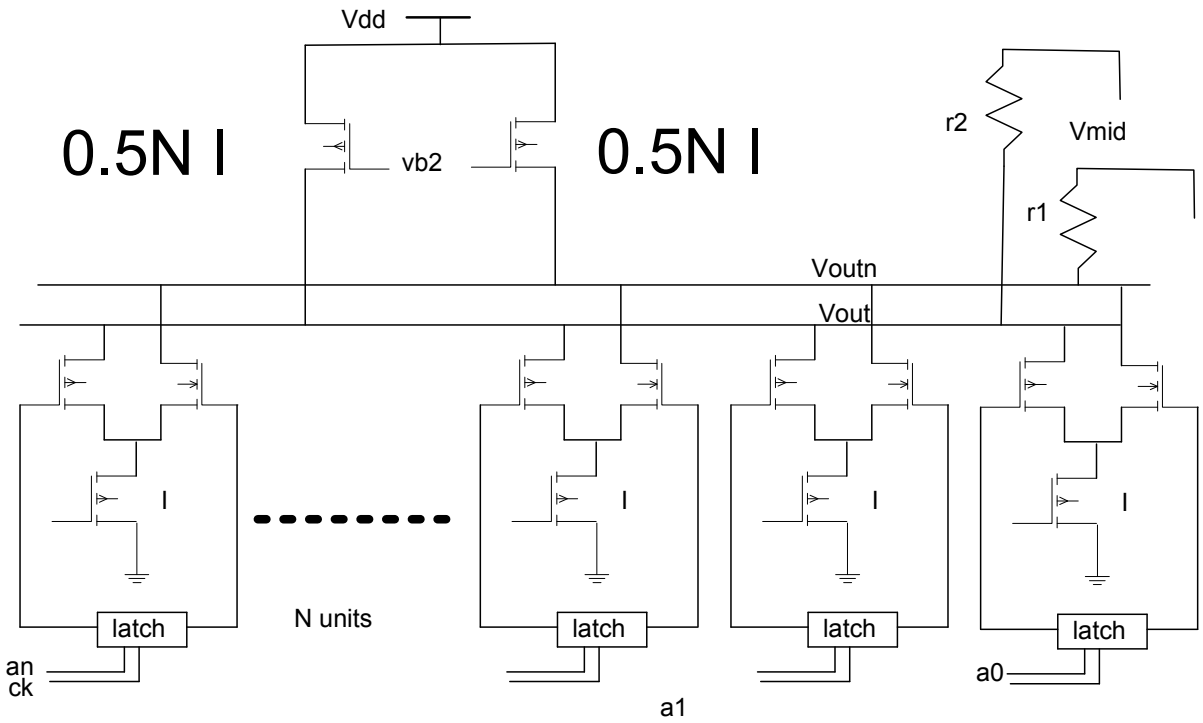
Binary Weighted



Use twice the current on the bottom
But only N channel switches (CML

Very Fast
Compact N latches (but need to be sized up)
Linearity limited by MSB
DNL spikes: in some code transitions

Thermometer

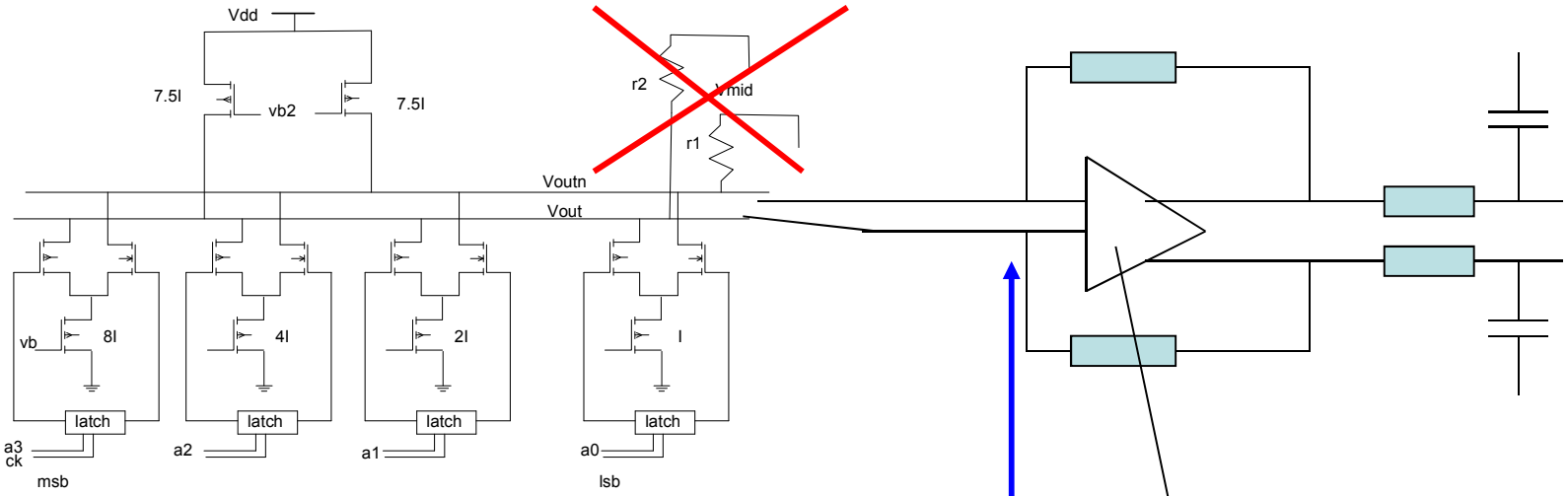


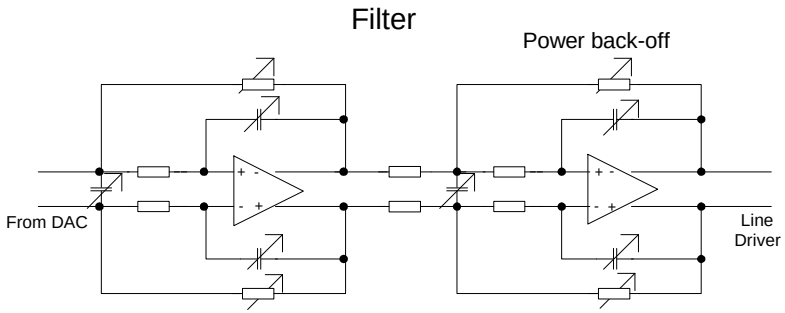
N I

Current source matching relaxed (DNL)
Each stage is LSB equivalent in contribution
For N bit, 2 to power of N latches, unit cells, wires
Silicon area is large, depend on marching and routing
Power supply grounding is important
I deal: Can combine with Binary approach and leave some MSB as Segmented

DAC with reduced Rout effect and filter

Fix the output impedance variations
And add the « out of ban » noise reduction filter



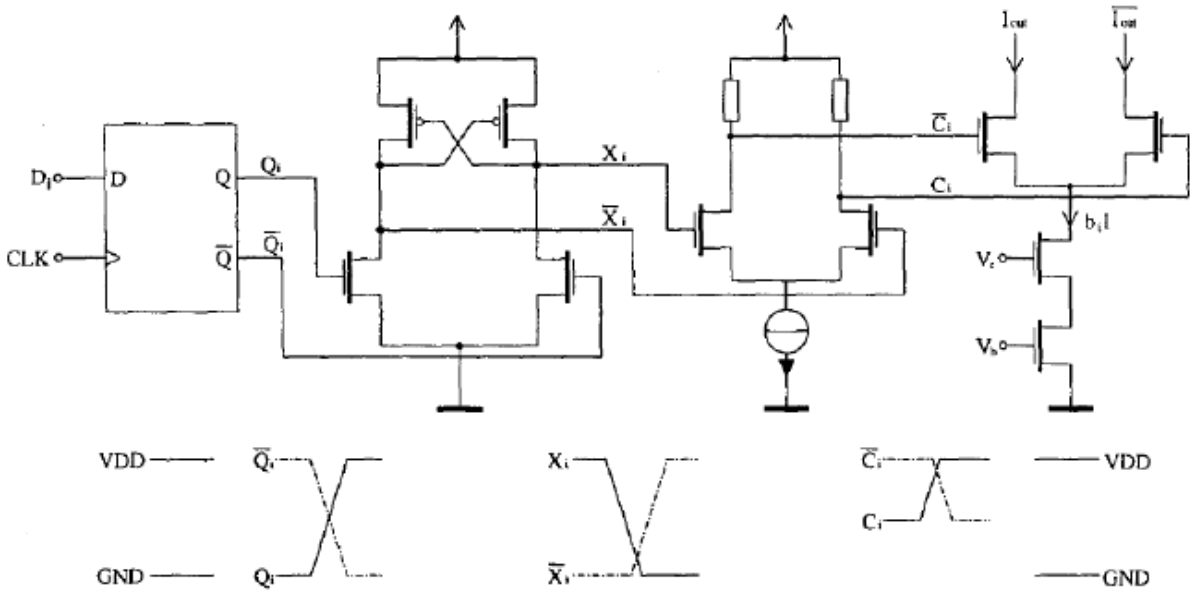


Virtual mid voltage
Non moving

Pre driver

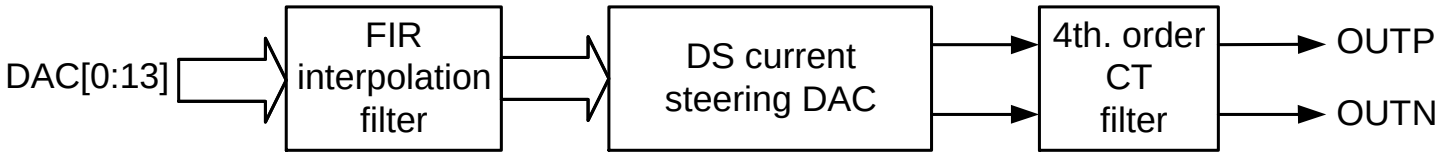
LATCH AND SWITCH
Minimization of glitches

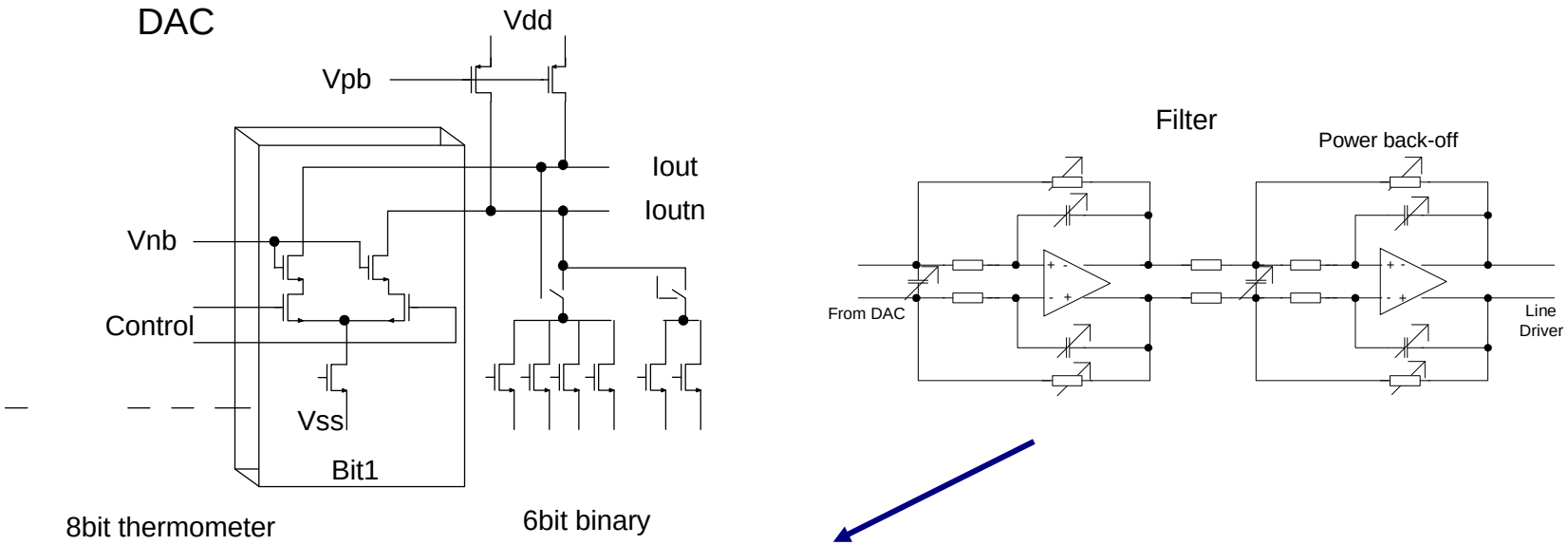
- **Non symmetrical crossing point**: reduces current source drain spike
- **Reduced clock swing**: sets on-voltage for cascoding bias and reduces clock feed-through



L. Sumanen, *et al*, "A 10-bit High-Speed Low-Power CMOS D/A Converter in 0.2mm^2", *Proc. of ICECS*, 1998

Dac to output path



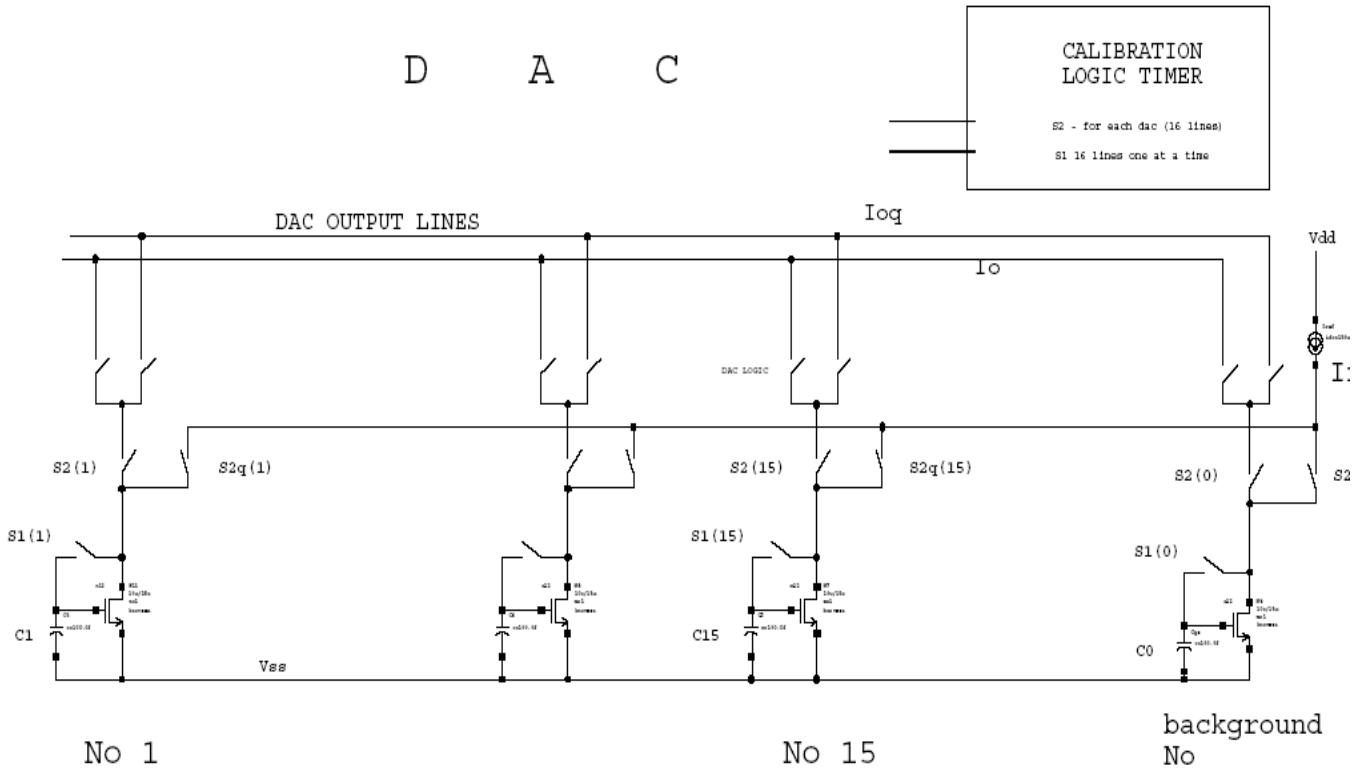


Deglitcher & Filter to reduce out of band noise
Set poles above maximum input BW

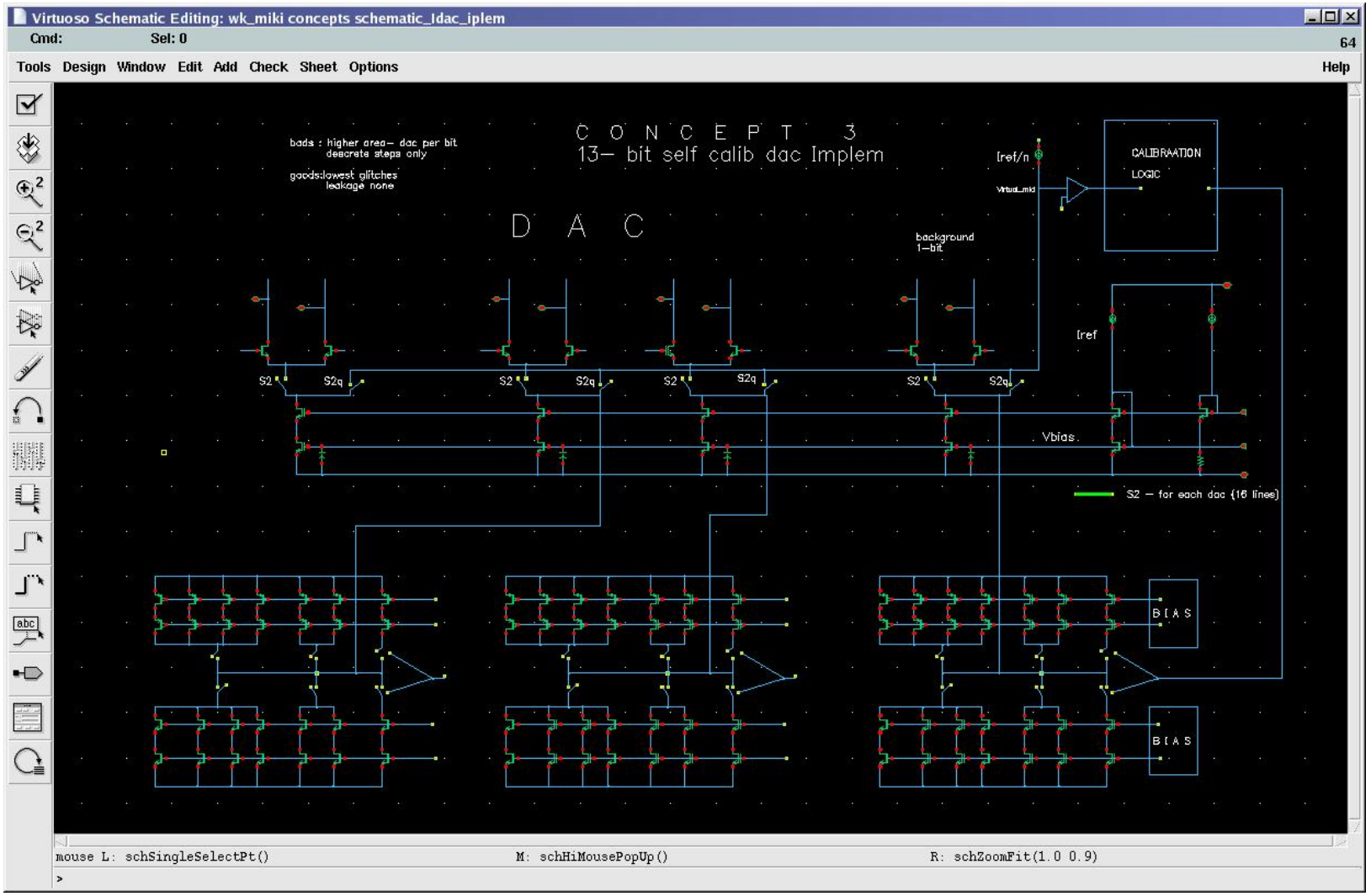
Calibration Methods

1) Make all I the same
2) Add error I
3) Dynamic Averaging

Calibration Method 1



Calibration Method 1



End lecture 06

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