Welcome to

0510.7720.01 Winter semester 2021

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 6 and 7- recorded for: may 13th and 20 2021..

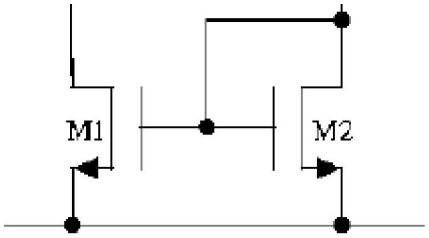
Comparator: Operation and Design

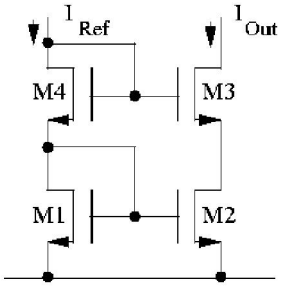
Agenda

Quick review on analog circuits basics

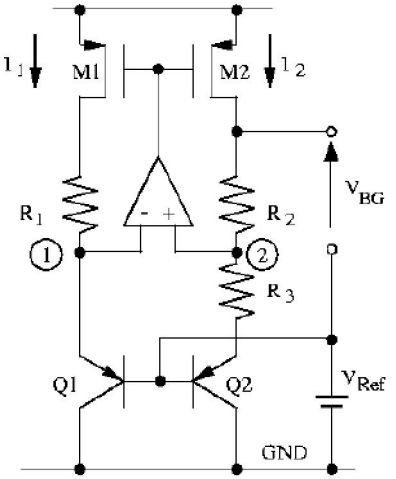
- Comparator Basics
- Architectures
- Error Sources
- Comparator Examples

Current sources- the heart of Analog Ics..-Video discussions..

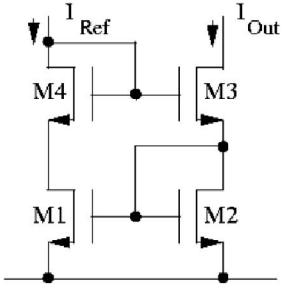


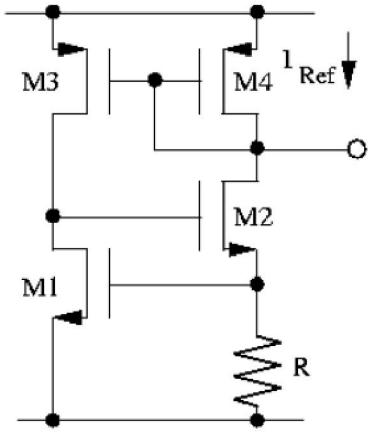


Cascode/cascade



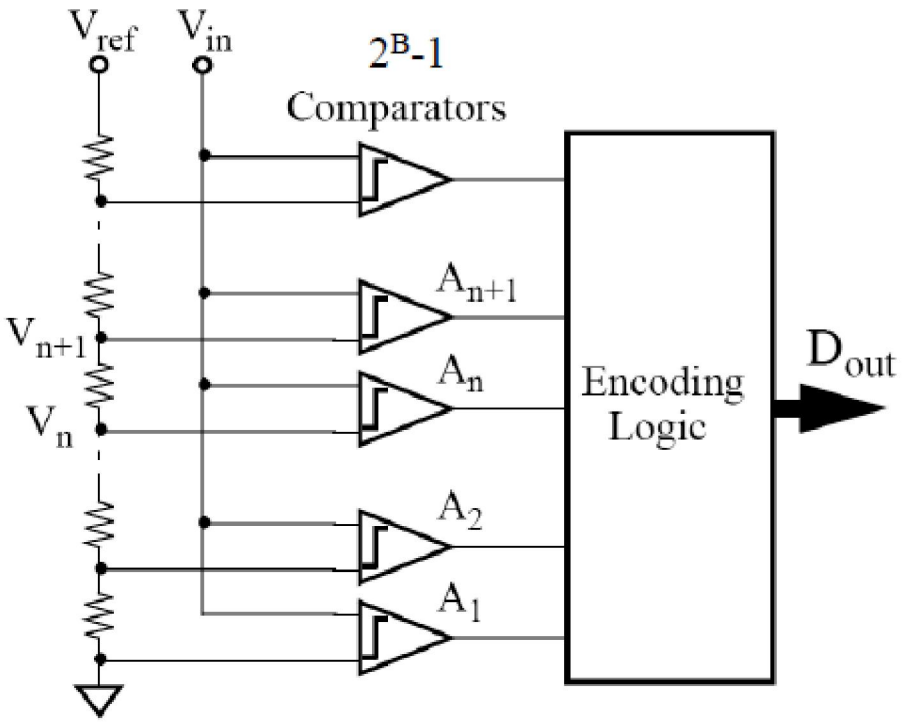
Improved Wilson Current Mirror

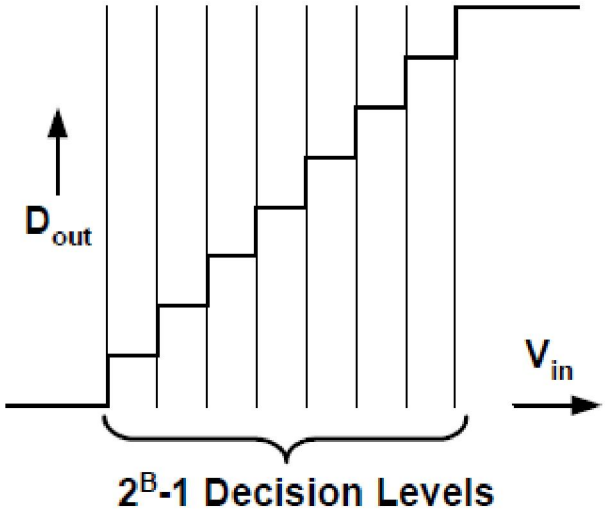




For the project assignment---convert the digital back to numbers..

Flash ADC

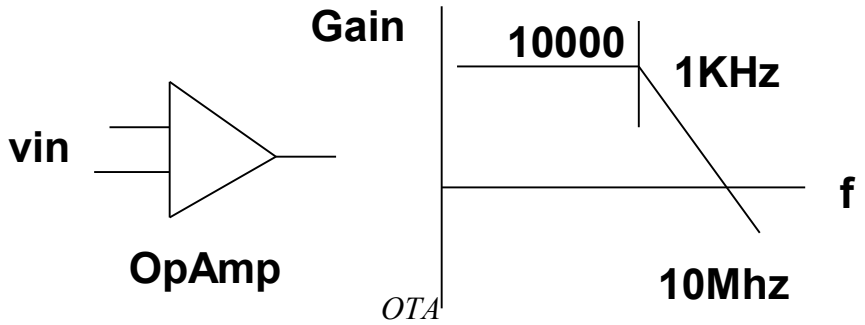




Comparator Basics – Design Methods

- Comparator:
  - Non Sampled
  - Sampled
- Error in Comparators
- Basic Analysis
- Architectures
- Special topics – Calibrated and differential

Speed and Feedback Basics

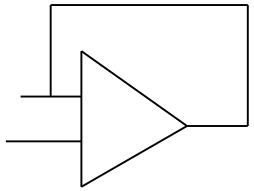


Speed

$\tau = 1ms$

Gain(dc)

80dB

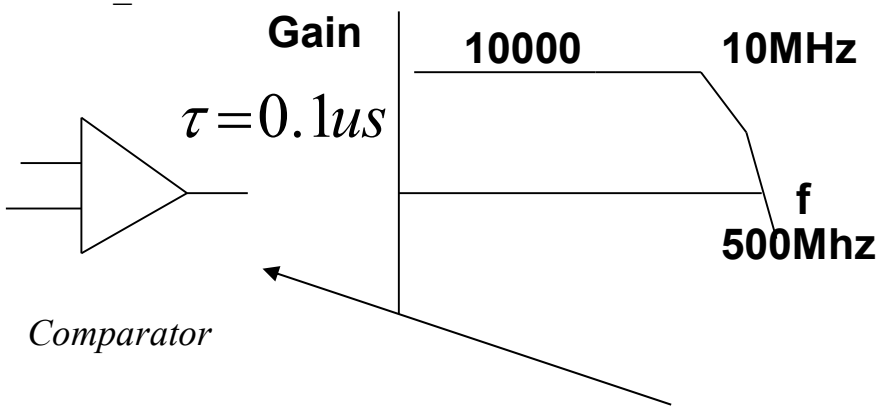


Gain=1

And accurate

$\tau = 0.1us$

0dB



$\tau \sim 0.1us$

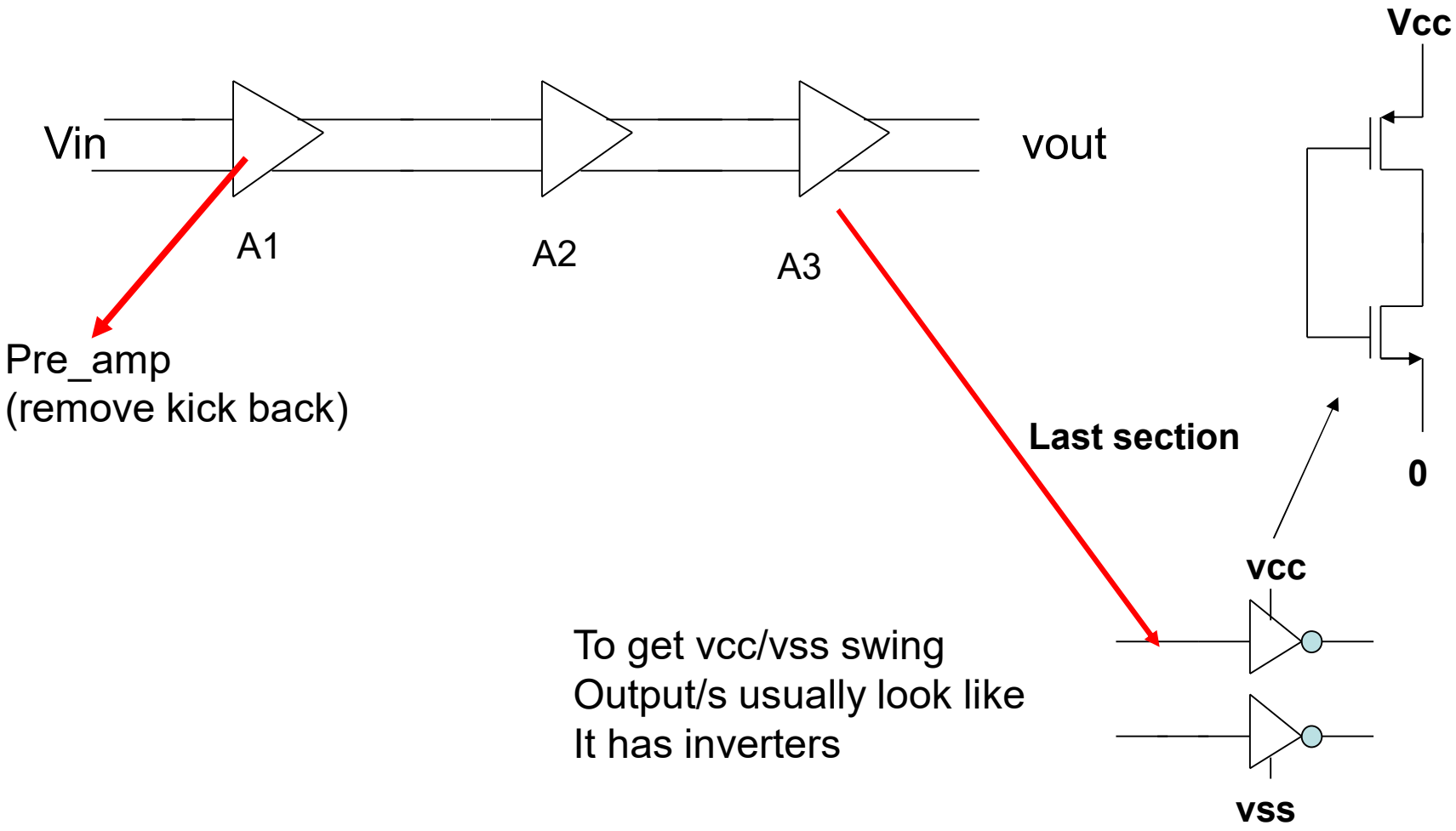
80dB

Removed all compensation

- **Comparator:**
  - A Link from Analog to Digital – Quantizer
- **Definition:**
  - Compares between 2 or more inputs and produce a digital value high or low- ***"Its a 1 bit ADC !"***
- **Structure:**
  - A chain of gain stages (no feed back-unlike amplifier)
- It is used in an "open Loop" configuration to achieve fast digital response (opamps are slow and big)

❑ Non Sampled: Continuous Time (CT)

- ❑ Output is gain time input differences:
  - ❑ slow because internal nodes need to be recovered

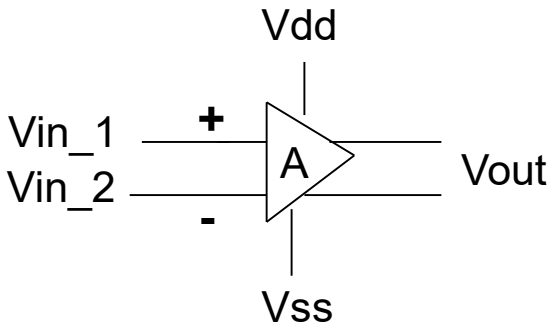


Mathematical Descriptions – Low Frequency

For small V_{in1}-V_{in2}

$$V_{out} = A(V_{in\_1} - V_{in\_2})$$

A = Gain of the combine structure



For all V_{in1}-V_{in2} V_{out}=clamp at either supply

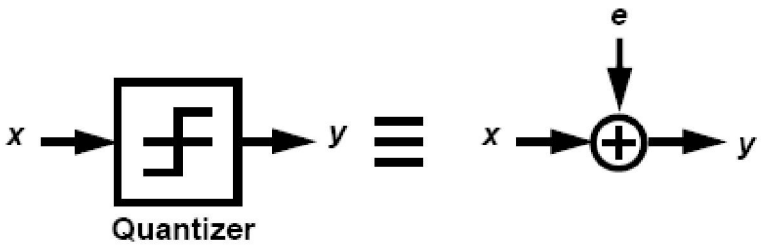
Ideal

$V_{out} = A(V_{in\_1} - V_{in\_2})$ → results fall between supplies (realistically its exponential)

$$V_{out} = V_{dd} \quad if\ A(V_{in\_1} - V_{in\_2}) > V_{dd} - V_{ss}$$

$$V_{out} = V_{ss} \quad if\ A(V_{in\_1} - V_{in\_2}) < V_{dd} - V_{ss}$$

Mathematical Descriptions with Noise



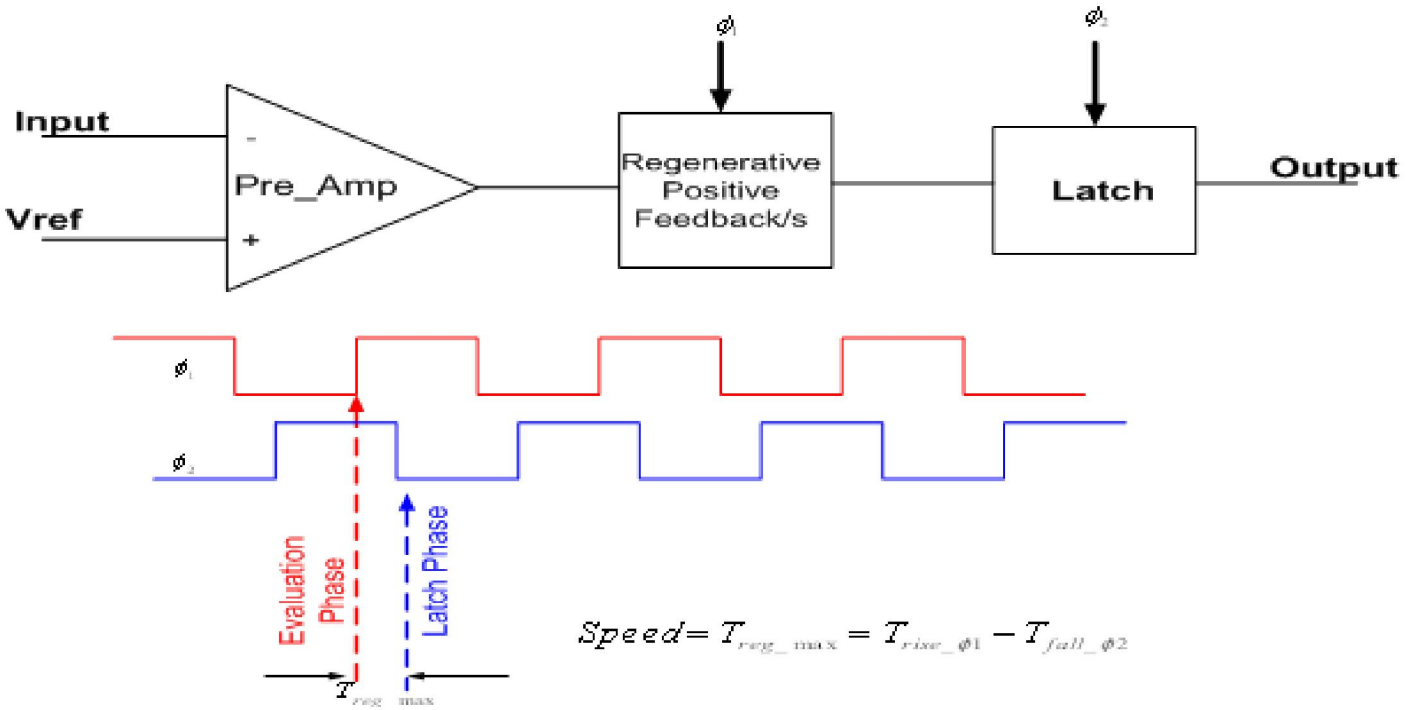
Important model in Sigma Delta ADCs

exact model if *e* is defined properly
ex. *y=sgn(x)*, then *e=y-x=sgn(x)-x*

becomes an approximation when we claim noise is independent

- **Sampled Comparator:**
  - Much faster
  - clamp high gain stages
  - Need clock or digital signal

Concept:



- **Errors in Comparators**:
  - Gain
  - Offset
  - Meta State
  - Speed
  - Kick Back
  - Noises and supply noise

Main Parameters Definitions

- Input Offset – It is the voltage that must be applied to the input to obtain the crossing point between low and high logic level
- Vout = A x Vindiff , vss<Vout<Vdd A=1000 , time is also a factor

- Sensitivity- It is the minimum voltage or current that produces a consistent output signal within the expected comparison time- Meta state

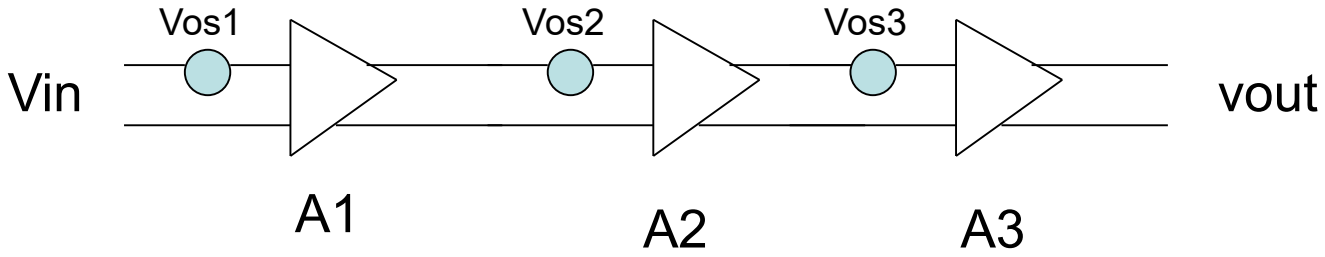
- Comparator response time – It is minimum time interval required to achieve the proper logic output as a response to the minimum input step

- Overdrive recovery time – When the input signal is pretty large the gain stage saturates to the positive or negative rails quickly. If the input stage become small, the gain stage takes some time to react and generates the voltage required to produce the output voltage

- Kick back input noise – Caused in evaluation state due to transition response: Switching noise

Offset and Gain – Basics in Comparator

V_{os}(total)



$$V_{os\,(total)} = \sqrt{V_{os1}^2 + \frac{V_{os2}^2}{A_1^2} + \frac{V_{os3}^2}{A_1^2 A_2^2}}$$

Key:

- **V_{os} is a statistic parameter**
- **Further stages (A2 and A3) have larger offset using minimum sizes..**

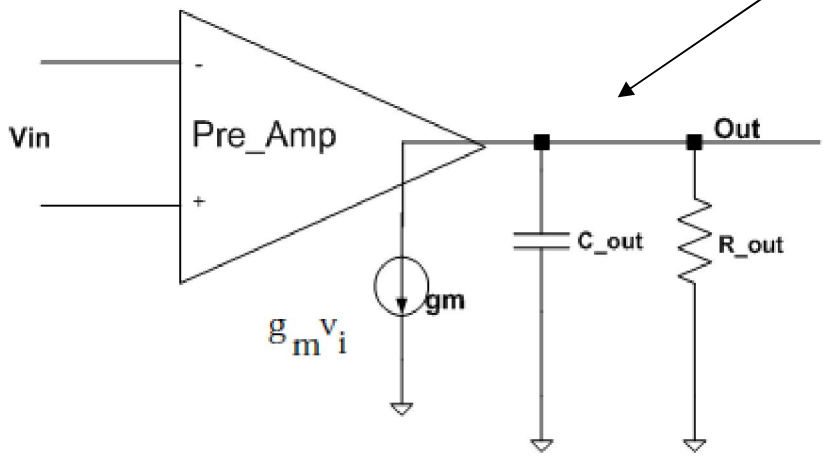
Example: 8 bit ADC

for 8 bit with V_{fs}=0.5v , V_{dd}=1v at 1/10LSB =
A1 x A2 x A3 required ~ 5000 ➔ (1v/(0.5/255 x 10)
If:
Vos1=2mv, vos2=10mv, vos3=20mv
If we take: A1=10mv A2=25mv A3=20mv

$$V_{os\,(total)} = \sqrt{2^2 + \frac{10^2}{10^2} + \frac{20^2}{10^2 25^2}} = 2.23mV$$

Gm Rout … diff stage..

Model (vi is Vin)

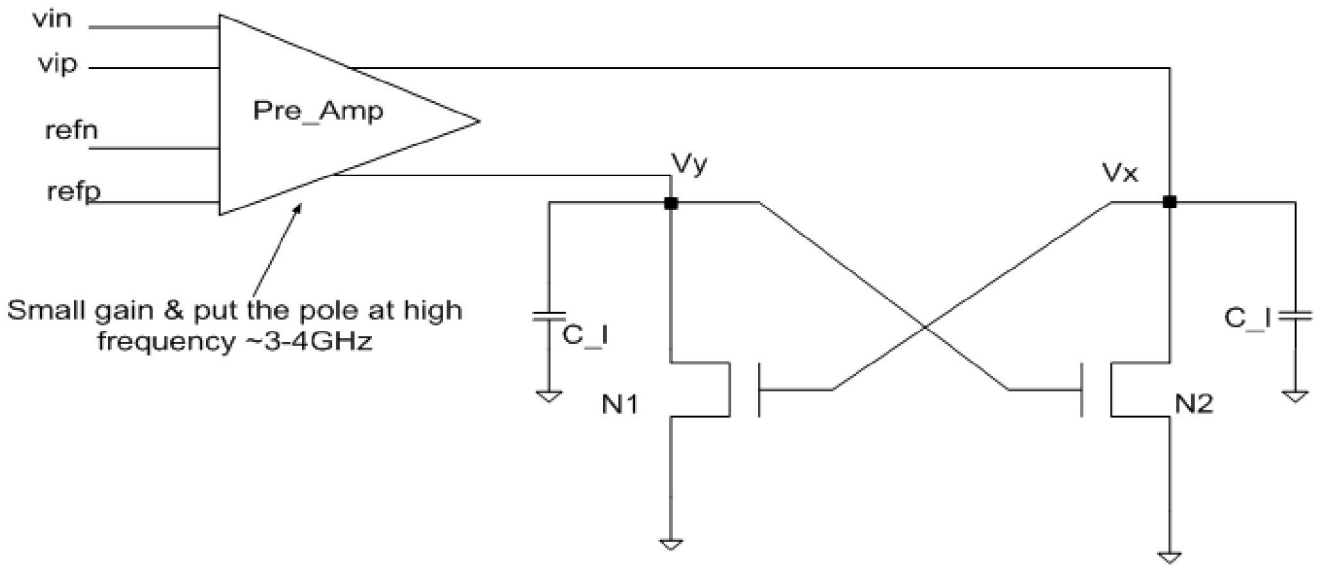


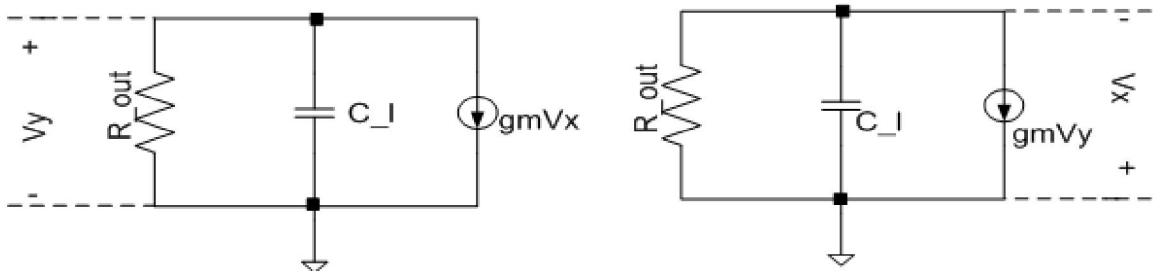
$$V_{out}(t) = V_{in} \cdot g_m \cdot R_{\_out} \cdot (1 - e^{-t_{reg}/\tau})$$

$$Where: \tau = R_{out} \cdot C_{out}$$

$$g_m = \frac{I}{V_{in}}$$

With Positive Feedback – Sampled





Small signal representation

Math – Positive Feedback Comparator Latch

$$g_m \cdot V_y = -C_L \cdot \frac{dV_x}{dt} - \frac{V_x}{R_{out}} \qquad g_m \cdot V_x = -C_L \cdot \frac{dV_y}{dt} - \frac{V_y}{R_{out}}$$

$$\begin{cases} \tau \cdot \dfrac{dV_x}{dt} + V_x = -A \cdot V_y \\ \tau \cdot \dfrac{dV_y}{dt} + V_y = -A \cdot V_x \end{cases} \rightarrow \text{where} \quad \tau = R_{out} \cdot C_L, \quad A = g_m \cdot R_{out}$$

Look not R but gm–
Great speed improvement

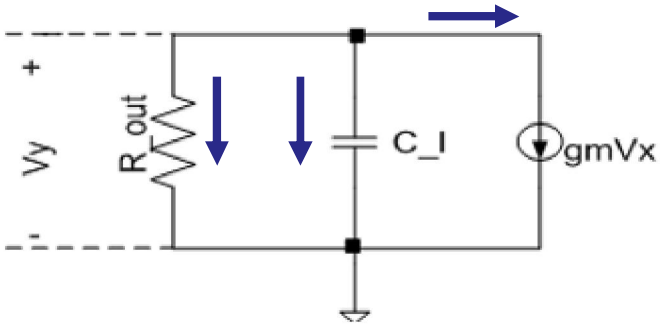
$$\tau \cdot \frac{d(\Delta V)}{dt} = \Delta V(A-1)$$

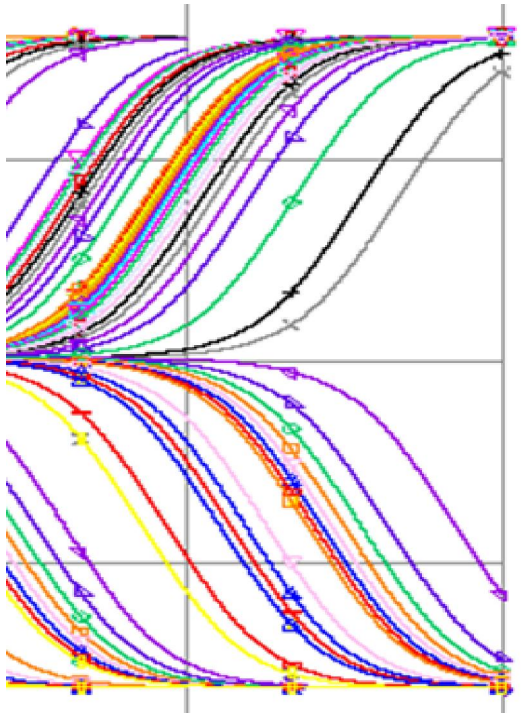
Solution →

$$\frac{\tau}{A-1} \cdot \frac{d(\Delta V)}{dt} = \Delta V$$

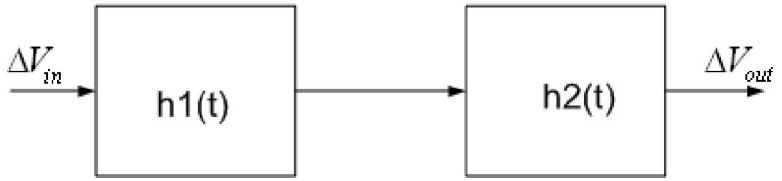
$$\Delta V = \Delta V_0 \cdot e^{\frac{A-1}{\tau}t} \approx \Delta V_0 \cdot e^{\frac{g_m}{C_L}t}$$

$$\frac{A-1}{\tau} = \frac{g_m \cdot R_{out} - 1}{R_{out} \cdot C_L} \approx \frac{g_m}{C_L}$$



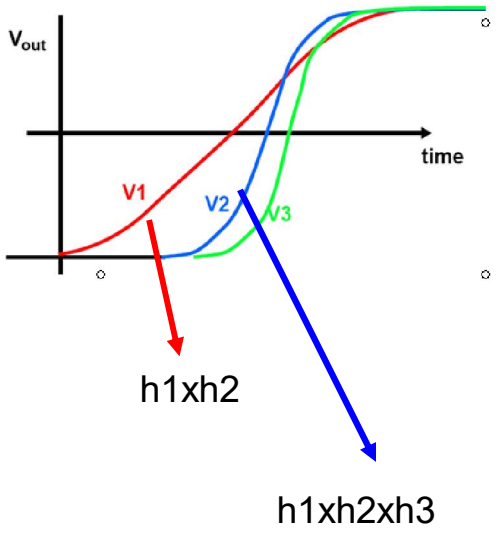


Band width reduction



$$h(t) = h_1(t) * h_2(t) = \left(e^{\frac{g_m}{C_L}\cdot t} * e^{\frac{g_m}{C_L}\cdot t} \right) = t \cdot e^{\frac{g_m}{C_L}\cdot t}$$

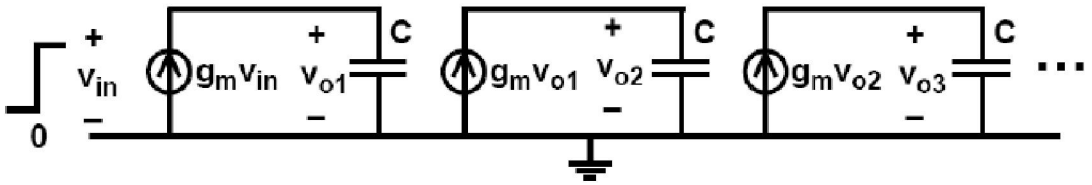
$$\Delta V_{out}(t) \approx \Delta V_{in} \cdot K \cdot t \cdot e^{\frac{g_m}{C_L}\cdot t}$$



Note: if we have n-stages of the regenerative feedbacks then

$$h_n(t) = h_1(t) * h_2(t) \cdots * h_{n-1} * h_n = \left(e^{\frac{g_m}{C_L}\cdot t} * e^{\frac{g_m}{C_L}\cdot t} \ldots * e^{\frac{g_m}{C_L}\cdot t} * e^{\frac{g_m}{C_L}\cdot t} \right) = \frac{t^{n-1} \cdot e^{\frac{g_m}{C_L}\cdot t}}{(n-1)!}$$

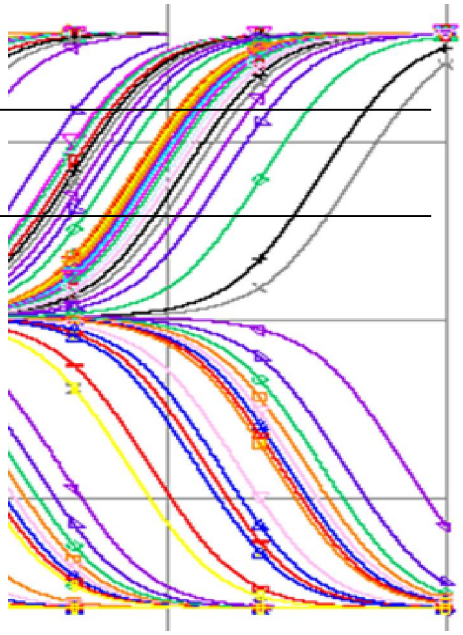
$$v_{oN} = \frac{\omega_u^N}{s^N} v_{in}$$



Meta Stability in Comparator

- Meta-stability is a potentially catastrophic event that can occur when asynchronous inputs and regenerative/flip-flops are used
- Meta-stable outputs are not logic high or logic low and cause delays and system failures
- Meta-Stability is a probabilistic event, because the difference between the input signal and the reference voltage is a random variable
- The smaller the difference between the input signal and reference voltage, the longer the decision time required. On the limit the decision time can approach infinity

Not defined place



Analytical Derivation of Meta-Stability & Mean Time To Failure (MTF)

- The probability event given following: where t is the actual comparison time, T is the allowed time

$$\Pr(t>T)=e^{\left(-\frac{A}{\tau}\cdot T\right)}=e^{-\frac{g_m}{C_{out}}\cdot T}$$

- If one can have a collection of N such comparators all clocking at a frequency fs, then one can found MTF following

$$MTF\approx\frac{e^{\frac{A}{\tau}\cdot T}}{N\cdot f_s}=\frac{e^{\frac{g_m}{C_{out}}\cdot T}}{N\cdot f_s}$$

~ Set it for > month

Example

- Example: 6-bit, 500MHz Flash ADC, $T_{max}=T_s/2=1ns$, $\tau_u=1/(2\pi\cdot 5GHz)=32ps$, $A_v=3$, $V_{FS}=0.5V_{DD}$

$$P(Error)=\frac{2}{3}\left(2^6-1\right)\cdot e^{-1000/32}\cong 10^{-12}$$

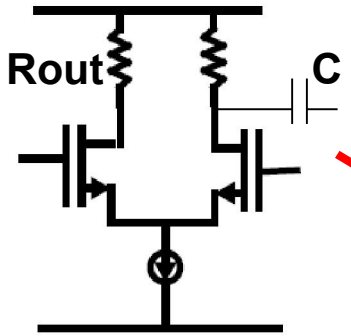
- Mean time to failure (MTF)

$$MTF=\frac{1}{P(Error)\cdot f_s}=\frac{1}{10^{-12}\cdot 0.5\cdot 10^9}s=2000s\cong 33\text{minutes}$$

source: Prof. Murmann stanford

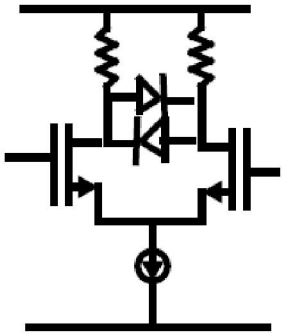
Front Stage Architectures- with Resistors

1. Use small values of R_l
   - Minimizes swing
   - Shortens time constant



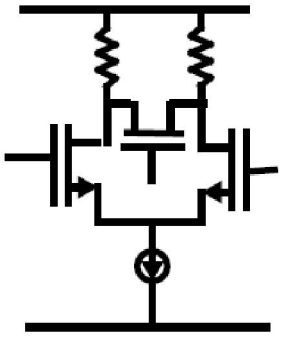
$$V_{out}(t) = V_{in} \cdot g_m \cdot R_{\_out} \cdot (1 - e^{-t_{reg}/\tau})$$
$$Where: \tau = R_{out} \cdot C_{out}$$

2. Use Passive Clamps
   - Limits Swing
   - Adds parasitics



BW = 1 / 2pi(RoutC)

3. Use active nulling clamps
   - Good in principle
   - Tough clock generation problem

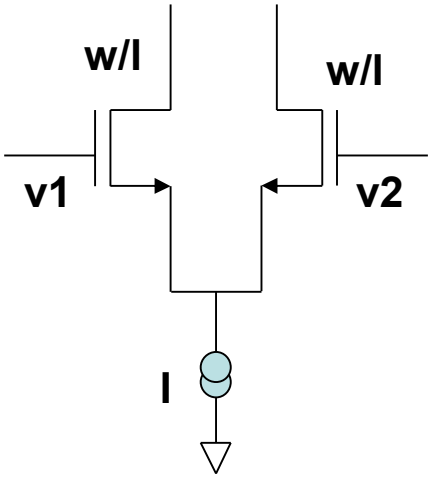


Source: P Gray

Summary:
Number of stages and gain needed
is process and project dependent no fixed analytical solution.

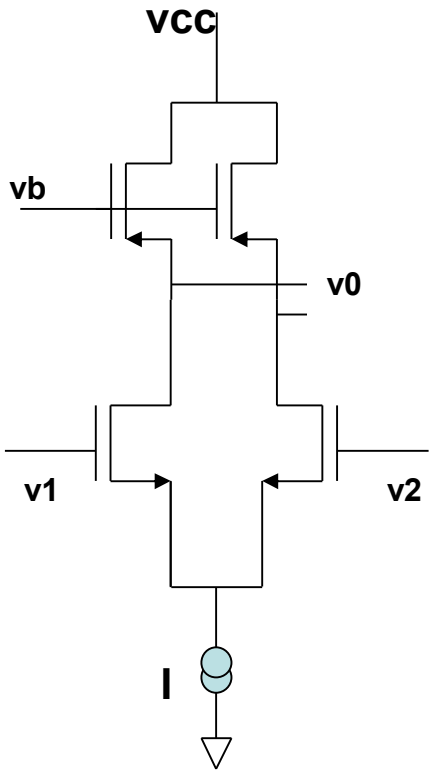
Best empirical gmR=4-8 number of stages ~ 2-4

Input Stage: Architectures Options - Using PMOS



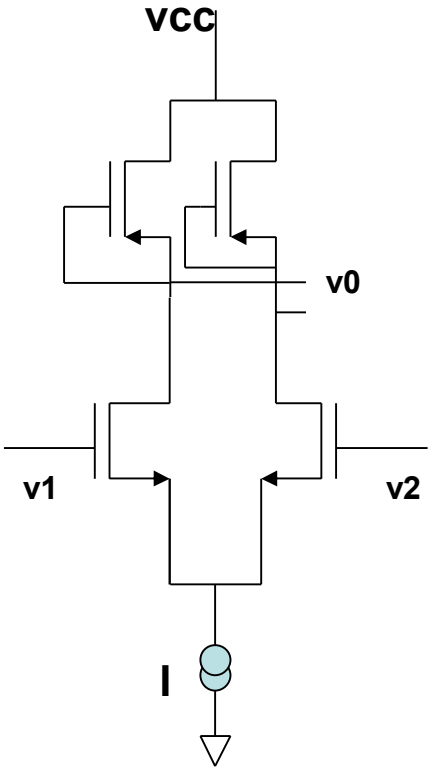
gm x what

A



gm x Rop/Ron
Kickback
Large gain

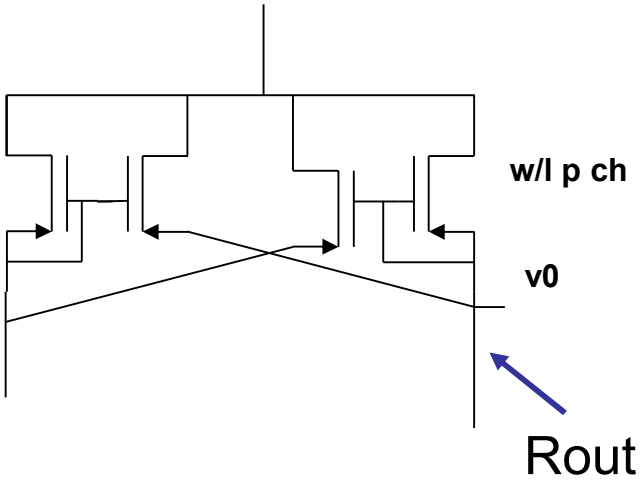
B

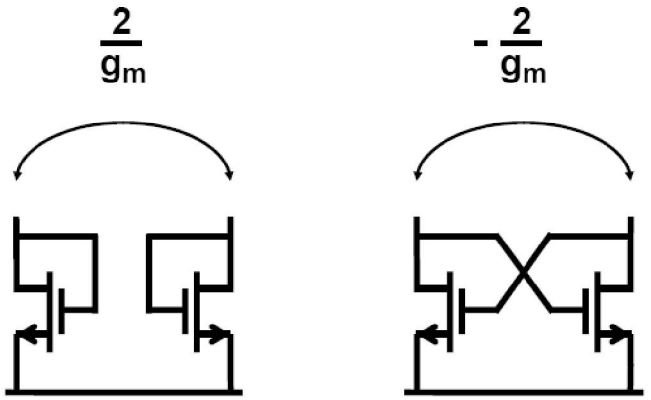


gm x 1/gmp
Low gain

C

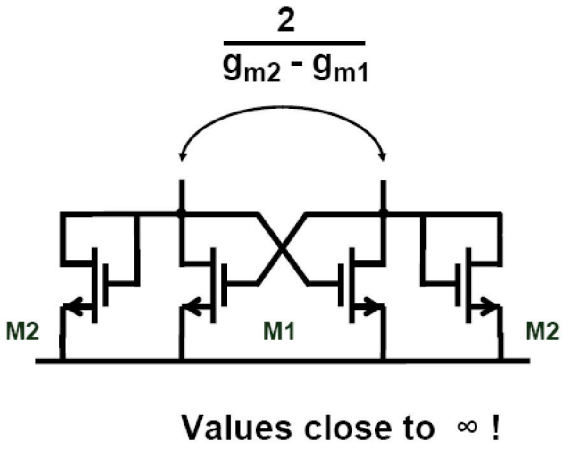
Added Feedback to Load





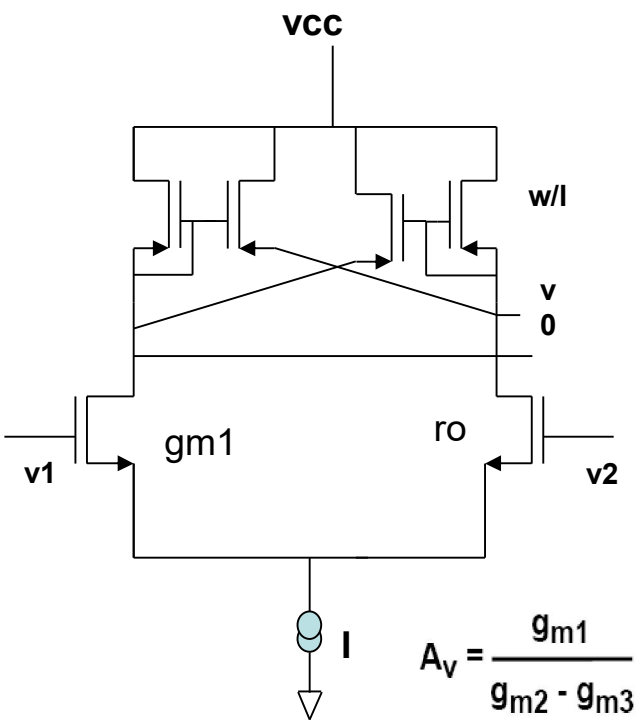
positive feedback to raise Rout

Effective rout =infinite



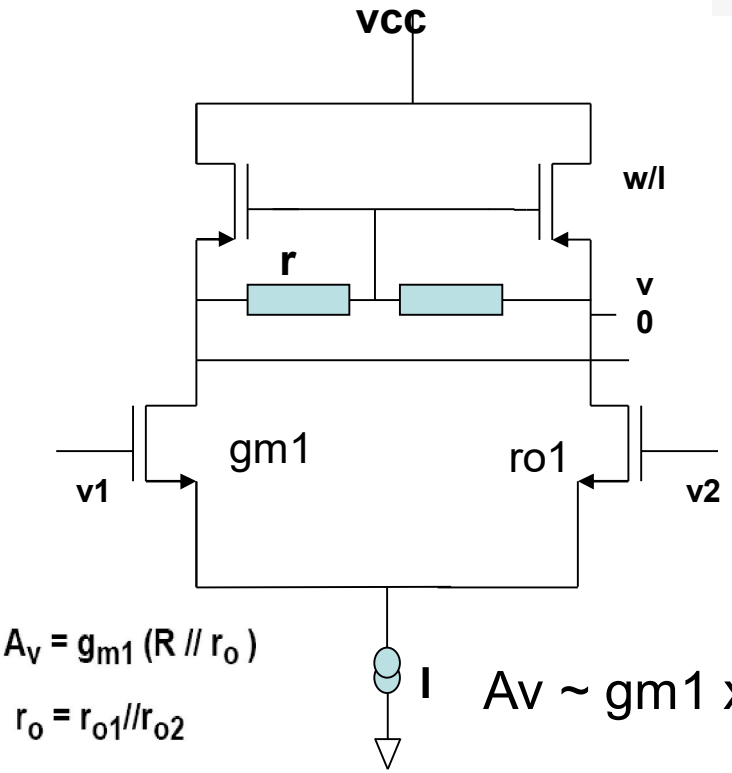
Source: Willy Snasen 2005

Input Stage: Architectures Options



$$A_V = \frac{g_{m1}}{g_{m2} - g_{m3}}$$

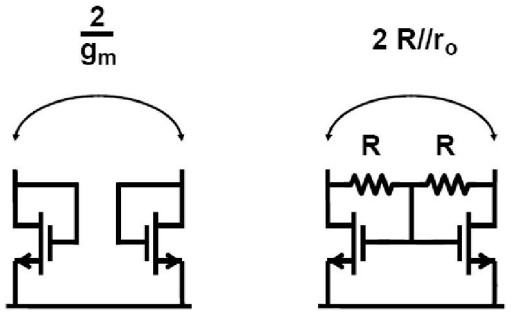
AV ~ gm1 x ro



$A_v = g_{m1} (R \,//\, r_o)$

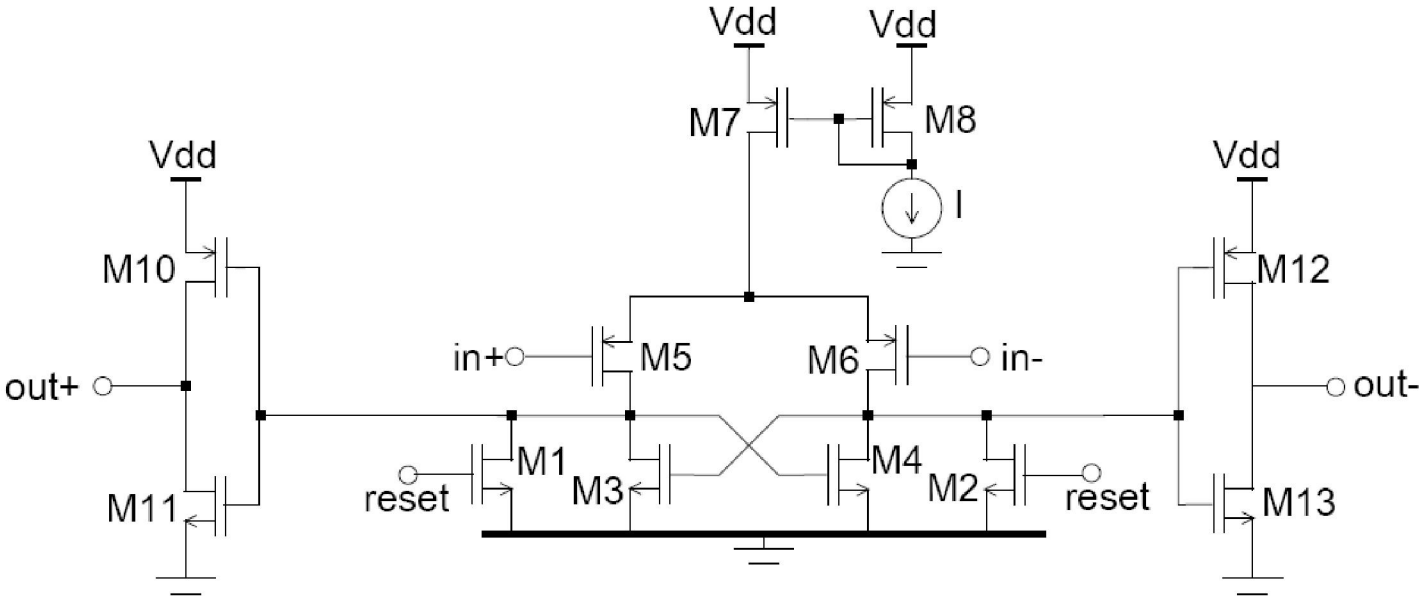
$r_o = r_{o1} // r_{o2}$

Av ~ gm1 x r



Source: Willy Snasen 2005

Comparator Examples

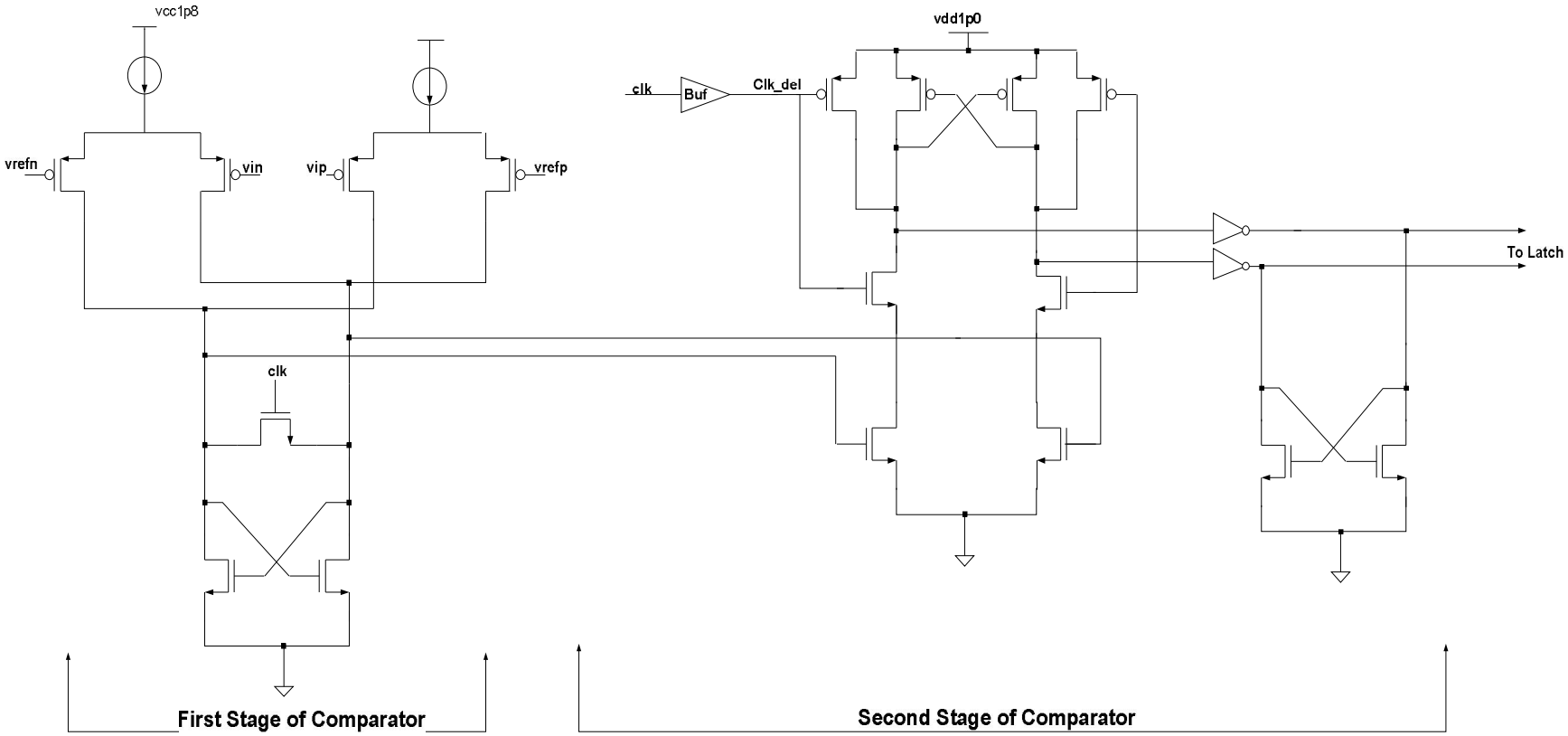


Simple

Good for low supply
Reset switch to ground
Kick back

Question can the outputs (inverter) swing to Vss ?

Differential Input Two Stage Comparator Option (no pre_amp)



More Example of comparators

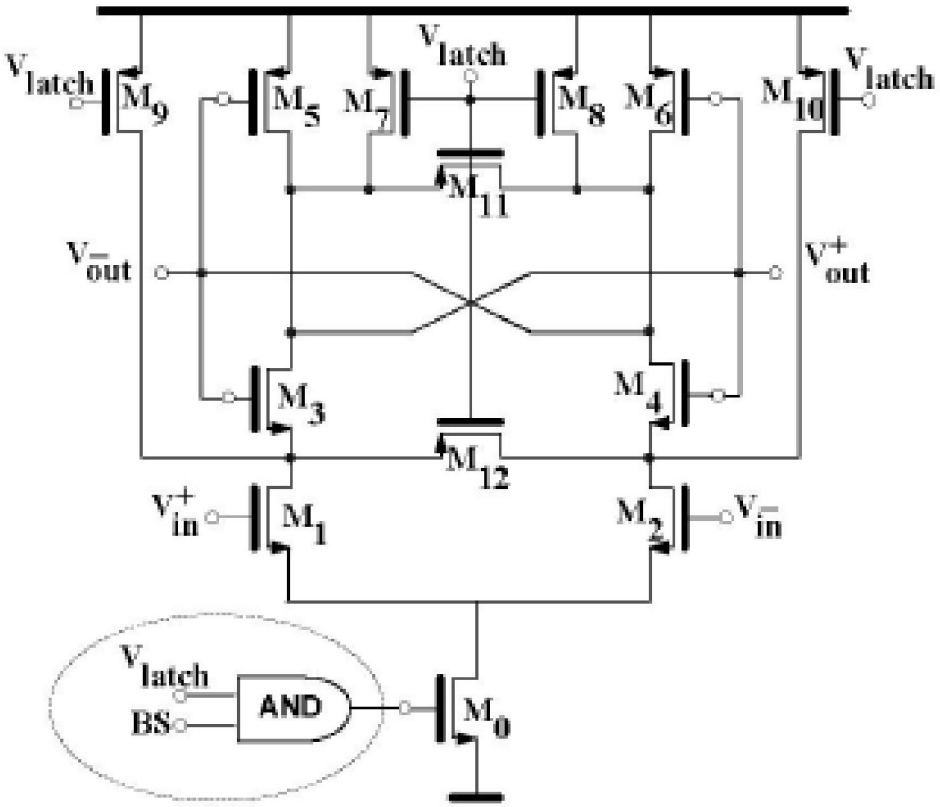
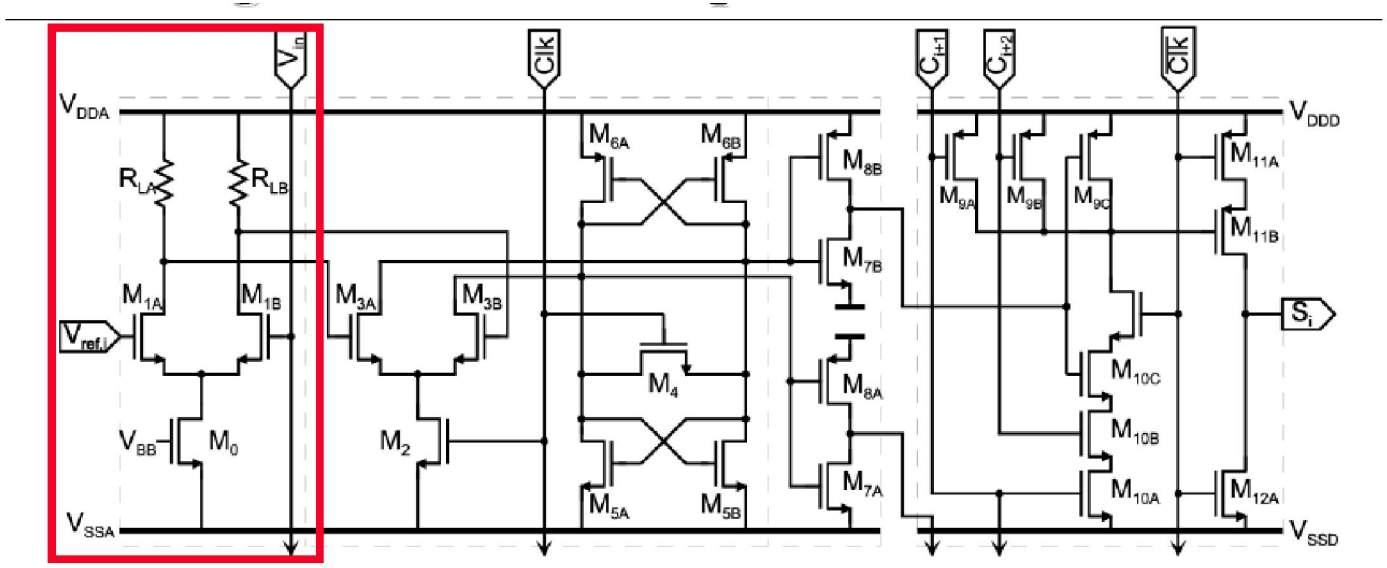


Fig. 5: High speed comparator and its switching circuit

A Power-Efficient 1.056 GS/s Resolution-Switchable
5-bit/6-bit Flash ADC for UWB Applications

Jun-Xia Ma, Sai-Weng Sin, Seng-Pan U [1], R.P.Martins [2]

Special Topics – Calibrated and differential
Architectures examples



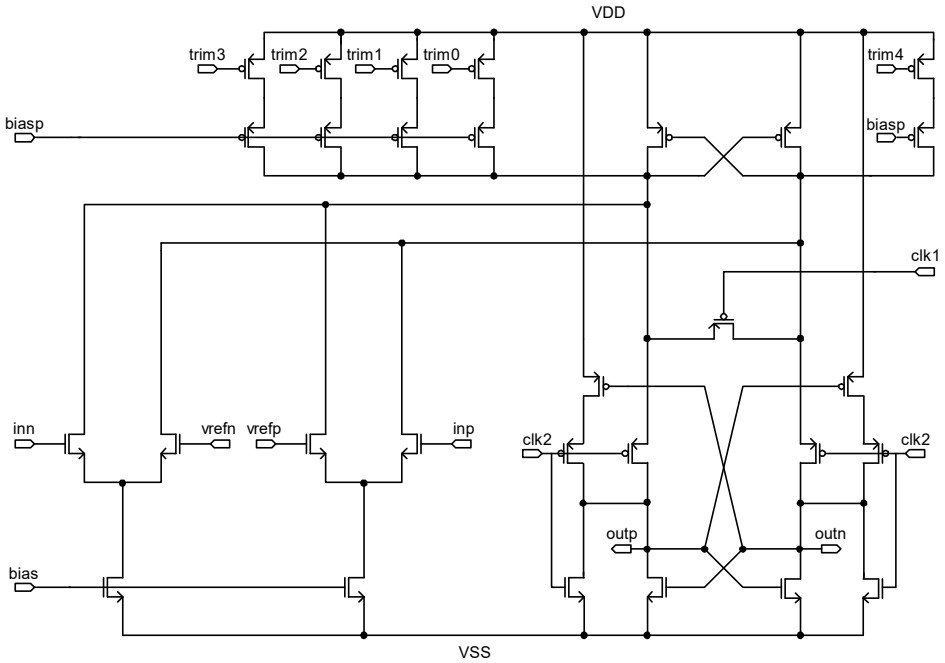
- ***Pre-amplifier [M1a,M1b]***
  - **Differential Pair with resistive load**
  - **Reduce Kick-back noise**
  - **Reduce Input Referred Offset Comparator**

Source: Esat-Micas esscirc00

Offset Calibration of Comparators:

Why? → Main reason lower input capacitance

Differential – Latched with Calibration Differential



A 10.3GS/s 6bit (5.1 ENOB at Nyquist) Time-Interleaved/Pipelined ADC Using Open-Loop Amplifiers and Digital Calibration in 90nm CMOS

Ali Nazemi[1], Carl Grace[1], Lanny Lewyn[1], Bilal Kobeissy[1], Oscar Agazzi[1,2], Paul Voois[1], Cindra Abidin[1], George Eaton[1], Mahyar Kargar[1], Cesar Marquez[1], Sumant Ramprasad[1], Federico Bollo[2], Vladimir A. Posse[1], Stephen Wang[1], Georgios Asmanis[1]
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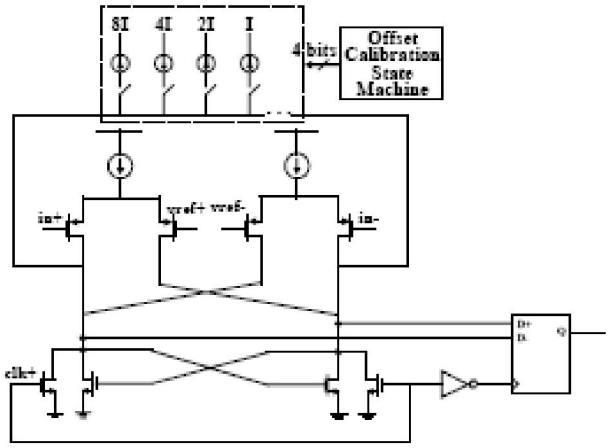


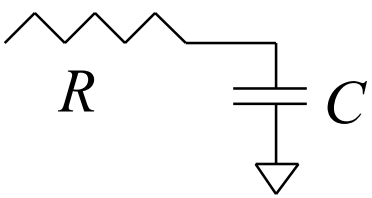
Comparator schematic with digital offset calibration.

End Lecture 8

Additions

Basic Feedback to Boost BW

"SLOW"

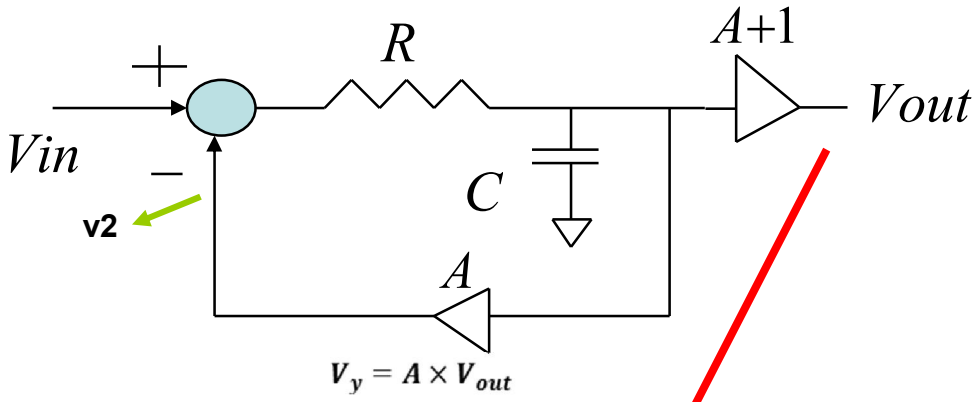


$$V_{out}(t) = V_{in}\left[1 - e^{-t/\tau}\right]$$

$$\tau = RC$$

$$Gain_{DC} = 1$$

"FAST"



$$V_{out}(t) = V_{in}\left[1 - e^{-t(A+1)/\tau}\right]$$

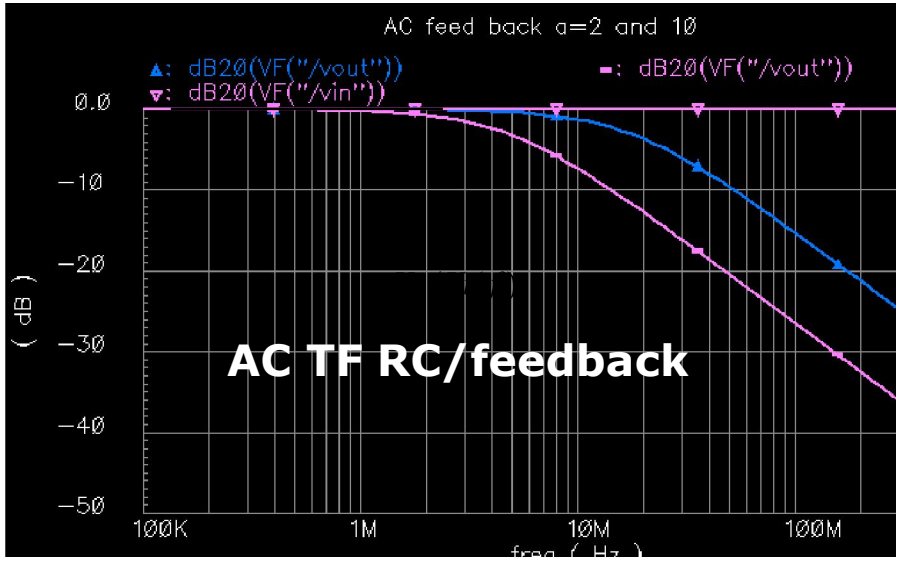
$$\tau(new) = RC/(A+1)$$

$$Gain_{DC} = 1/(1+A)$$

But at V_2:

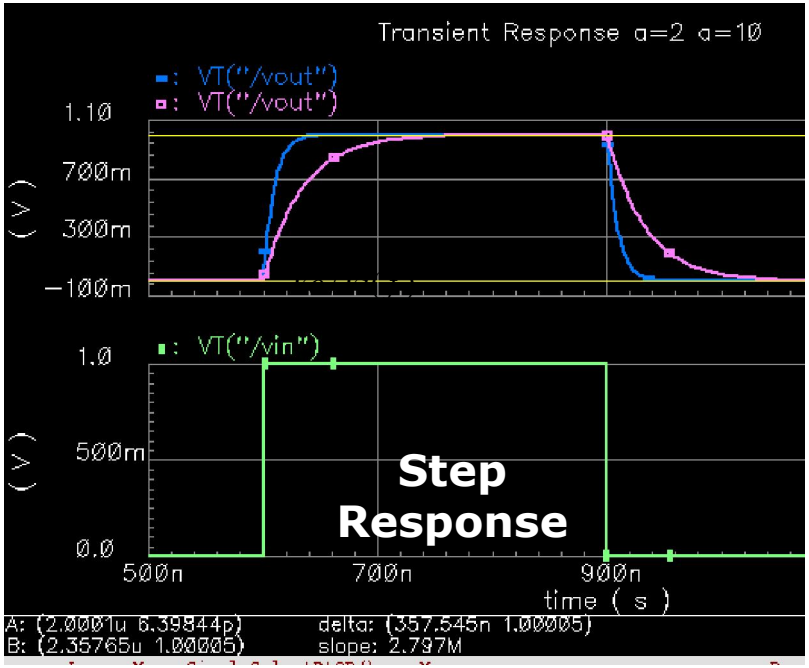
$$Gain_{DC} = \frac{A}{1+A} \approx 1$$

Simulation: A=2 and A=10



Frequency

$$Vo/Vi(f)$$



Time

AC Response

Time Domain