Welcome to
046188 Winter semester 2012
Mixed Signal Electronic Circuits
Instructor: Dr. M. Moyal

Lecture 5a

Cont. Mismatches in Mixed Signal Circuits

Mismatches in CMOS devices.

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Summary lect. 2-4

Eq. and definitions

$$SNR = \frac{Signal\ Power}{Total\ Noise\ Power}$$

$$SNDR = \frac{Signal\ Power}{Noise\ and\ Distortion\ Power}$$

$$ENOB = \frac{SNDR(dB) - 1.76dB}{6.02dB}$$

$$SFDR = \frac{Signal\ Power}{Largest\ Spurious\ Power}$$

$$THD = \frac{Total\ Distortion\ Power}{Signal\ Power}$$

$$V_{noise}^2 = 4 \cdot k \cdot T \cdot R \cdot \Delta f$$

$1K\Omega => 4.09 \cdot (\eta V / \sqrt{Hz})$

Noise in a resistor

$$V_{in\_noise}^2 = \frac{(2/3) \bullet 4 \cdot k \cdot T \cdot \gamma}{g_m} \cdot \Delta f$$

$$V_{in\_noise}^2 = \frac{Ko \bullet \cdot k \cdot T}{W \bullet L \bullet f} \cdot \Delta f$$

Noise in a transistor (CMOS)

$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

C= Ca x Area = Ca x W x L

MISMATCHES

One of the most critical parameters in Mixes signal design.

Mostly ignored with normal simulators

Mismatches- modelling-"Pelgrom rule"

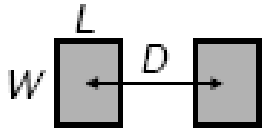
MISMATCHING
In Current-Steering D/A Converters

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 5, OCTOBER 1989

Matching Properties of MOS Transistors

MARCEL J. M. PELGROM, MEMBER, IEEE, AAD C. J. DUINMAIJER, AND ANTON P. G. WELBERS

/o equal



'Random' mismatch

Transistor sizing

'Systematic' mismatch

Layout techniques

$$\sigma_{V_T} = \frac{A_{V_T}}{\sqrt{WL}} + S_{V_T}^2 D^2$$

$$\frac{\sigma_\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}} + S_\beta^2 D^2$$

$$\frac{\sigma_\gamma}{\gamma} = \frac{A_\gamma}{\sqrt{WL}} + S_\gamma^2 D^2$$

First test:

Is it a current source mode ?
Is it a voltage mode device ?
Is it a switch ?

Mixed signal design must address:

Can we ignore/neglect the error ?

If not can we “calibrate” or fix the errors ?

Mismatches- Vth.

Process deviation: threshold voltage is highly process dependent:

$$Vth = VFB - Qss/Cox + Vsub + 2|\Phi p| + |Qd|/Cox$$

where:

VFB- flat band voltage,

Qss – surface charge per unit area,

Vsub – substrate voltage,

$2|\Phi p|$ - voltage required for strong inversion, doping gradients

Qd – depletion charge per unit area in the depletion region

Cox – oxide capacitance per um2, depends on oxide thickness

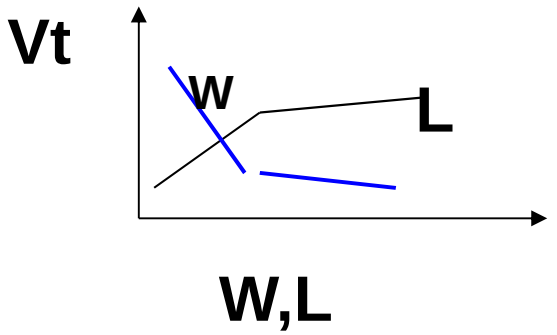
All of them except Vsub are process dependent and randomly or graded distributed

Layout mismatch: Voltage drop on along power line can cause graded error

Mismatches- History

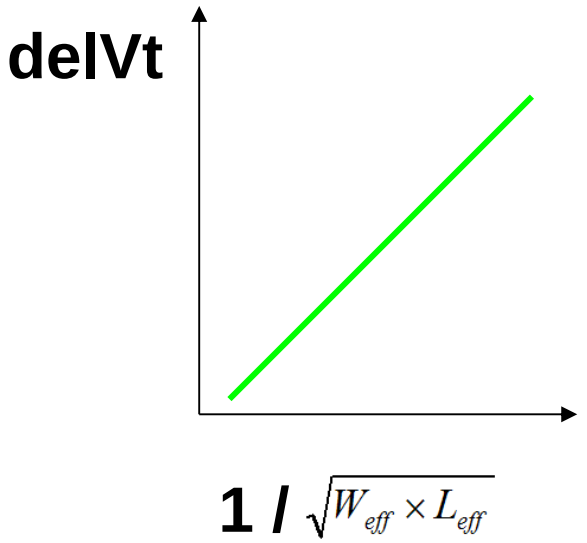
First belief was based on measured data :
Very L dependent and Very W dependent

Low L Vt. goes down – so variations is large
Low W Vt. goes up – so variation is large



Today Pelgrom law define most mismatches as function of area WxL

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}}$$



Note on C1

C1 is in today design ~ 2-10 mV for W x L =1 (u x u)

C1 has strong dependency on manufacturing – we do not have much control

C1 follow ~ 1.5 tox (in nm-> mv) as a “rule of thumb” – use thin oxide devices

C1 can be different for different layouts – we have control

Example for C1.

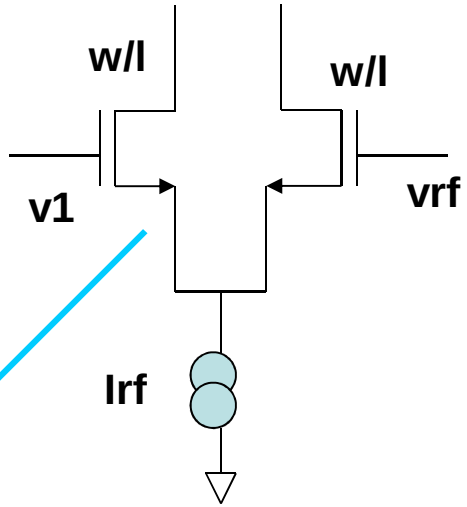
~ 3nm Tox --_ 90nm process ~ 4.5mv x um
0.18um process tox=4nm ~ 6mv x um
3.3v process, tox~7nm ~ 10mv x um

V Mismatches- Saturation

$$\sigma^2(I_D) = \frac{\beta^2}{2}(V_{GS} - V_T)^2 * \sigma^2(\Delta V_T) + I_D^2 * \sigma^2(\frac{\Delta L}{L})$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L}$$

“never mind” this.. Create a design model



amplifiers, comparators offset.

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}} \rightarrow \propto \frac{1}{\sqrt{W_{eff} \times L_{eff}}}$$

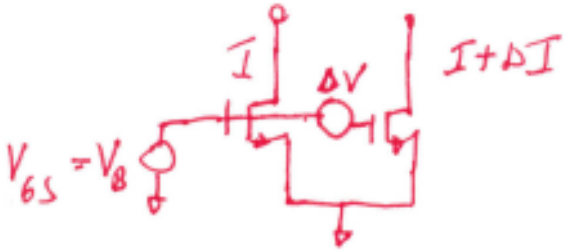
increase area for better results
What happen to input cap ?

I Mismatches- Saturation: method I

1

$$I = k\frac{W}{2L}(V_{GS}-V_T)^2 = \alpha(V_{GS}-V_T)^2$$

$$\Delta I + I = k\frac{W}{2L}(V_{GS}+\Delta V - V_T)^2 = \alpha(V_{GS}-\Delta V - V_T)^2$$



$$\Delta I = \alpha\left[(V_{GS}-\Delta V-V_T)^2-(V_{GS}-V_T)^2\right]$$

$$= \alpha\left[(V_{GS}-V_T)^2+\Delta V^2+2(V_{GS}-V_T)\Delta V-(V_{GS}-V_T)^2\right]$$

$$\Delta I \cong \alpha\, 2(V_{GS}-V_T)$$

$$\frac{\Delta I}{I} = \frac{\alpha\cdot 2(V_{GS}-V_T)\Delta V}{\alpha\,(V_{GS}-V_T)^2} = \frac{2}{V_{GS}-V_T}\cdot\Delta V = \left[\frac{2}{V_{GS}-V_T}\right]\frac{\sigma(V_T)}{\sqrt{W\times L}}$$

$$\left(\frac{\Delta I}{I}\right)^2 = \left[\frac{C_1}{\sqrt{W\times L}}\right]^2\frac{4}{(V_{GS}-V_T)^2}$$

One way.

$$\frac{\sigma^2(I_D)}{I_D^2} = \left\{\frac{\beta}{I_D}\sigma^2(\Delta V_T)+\sigma^2\left(\frac{\Delta L}{L}\right)\right\} = \left\{\frac{2}{(V_{GS}-V_T)^2}\sigma^2(\Delta V_T)+\sigma^2\left(\frac{\Delta L}{L}\right)\right\}$$

I Mismatches- Saturation- second method

$$\frac{\Delta I}{I} = \frac{g_m \cdot \Delta V}{I} = \frac{\sqrt{2k\frac{W}{L} \cdot I}}{I} \Delta V$$

$$= \frac{\left(2k\frac{W}{L}\right)}{\sqrt{I}} \cdot \Delta V = \frac{\sqrt{2k\frac{W}{L}}}{\sqrt{k\frac{W}{2L}}\,(V_{GS}-V_T)} \cdot \Delta V = \frac{2}{V_{GS}-V_T} \Delta V$$

$$\Delta I = g_m \cdot \Delta V$$

$$\boxed{\frac{\Delta I}{I} = \frac{2}{V_{GS}-V_T} \cdot \frac{C_1}{\sqrt{W \times L}}}$$

Second way.

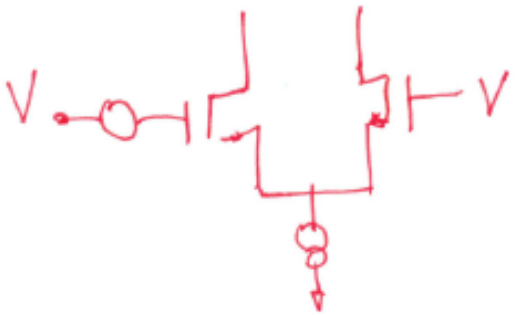
LARGE V_{GS}

In spice- monte-carlo can
Add also w and L mismatches

$$\frac{\Delta I_D}{I_D} = \left[\left(\frac{\Delta\frac{W}{L}}{\frac{W}{L}}\right) + \left(\frac{2\Delta V_T}{V_{GS}-V_T}\right)\right]$$

Mismatches/offset Vs. L, W,

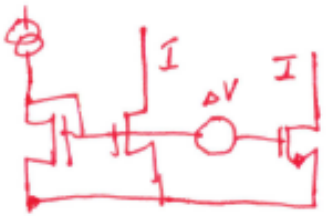
Amplifiers comparators minimize offset (mismatches)



$$\Delta V = \frac{C}{\sqrt{W \times L}} \Rightarrow \text{INCREASE } W \times L \text{ AREA}$$

$$\sim \boxed{\frac{1}{\sqrt{W \times L}}}$$

CURRENT SOURCES MINIMIZE I offset, MISMATCH.



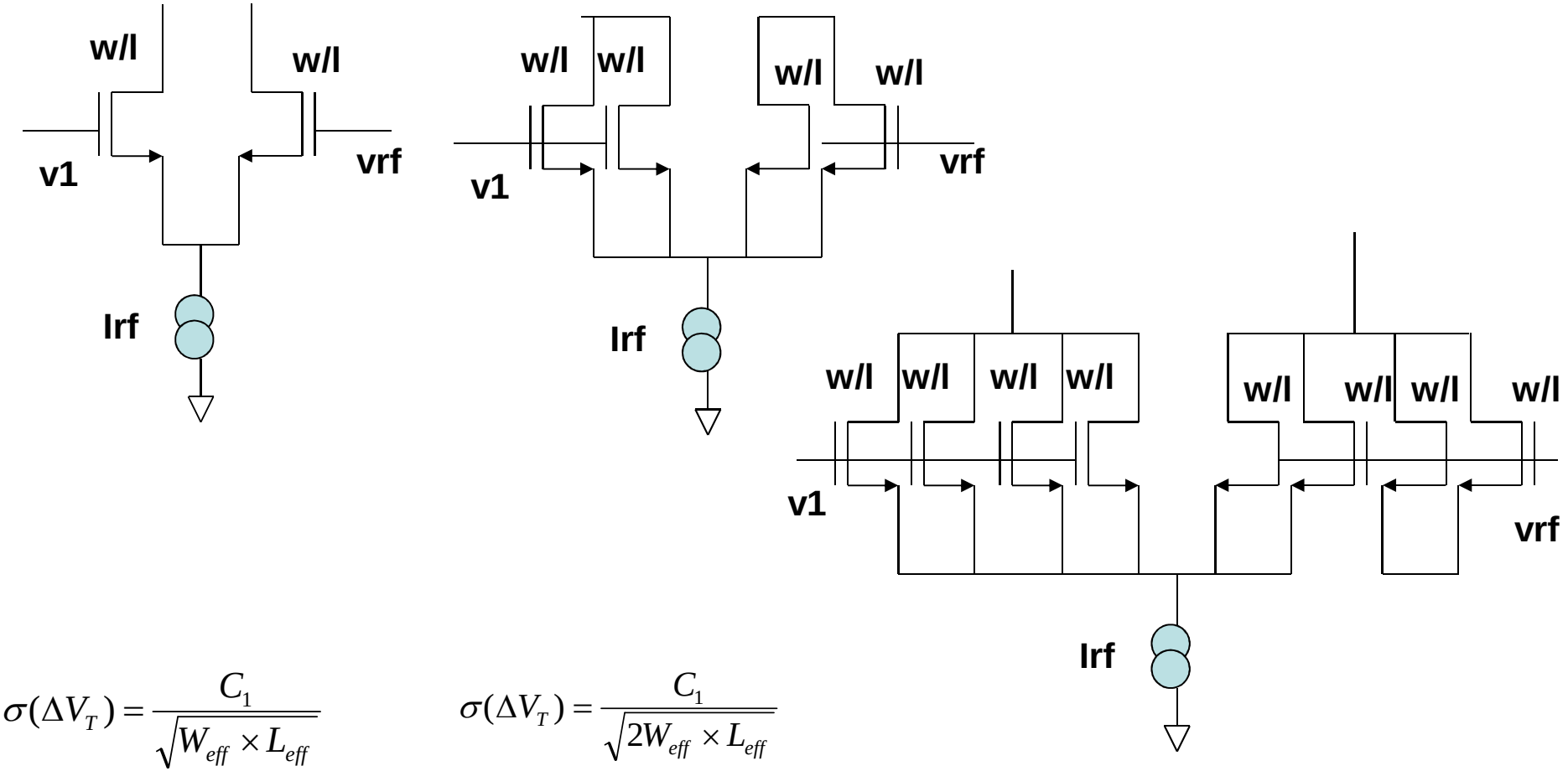
no $\Delta V \Rightarrow I + \Delta I$.

$$\Delta I = g_m \cdot \Delta V = \frac{g_m C_1}{\sqrt{W \times L}} = \frac{\sqrt{\left(k \frac{W}{L} 2I\right)} C_1}{\sqrt{W \times L}}$$

$$\Delta I = \frac{C \sqrt{2 I \mu_0 C_{ox}}}{L} \sim \boxed{\frac{1}{L}}$$

LARGER L

Example: Mismatches/offset



$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}}$$

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{2W_{eff} \times L_{eff}}}$$

$$\sigma(\Delta V_T) = \frac{C_1}{2\sqrt{W_{eff} \times L_{eff}}}$$

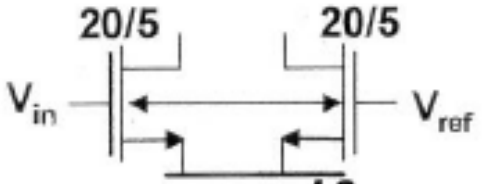
4x transistor area = ½ offset improvement

Calculate the Matching

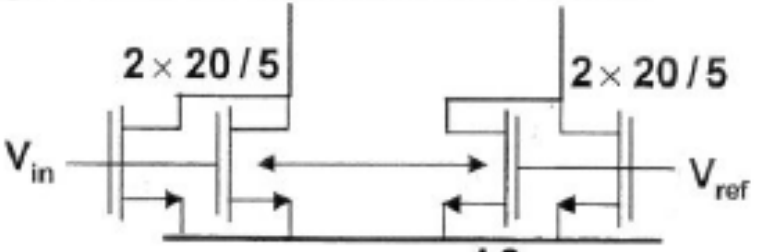
$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}} \qquad A_{VT} = 10\ mV\,\mu m$$

V_{ref} is fixed;

Calculate the input-voltage-referred standard deviation



$$\sigma_{\Delta(Vin-Vref)} = \frac{10}{\sqrt{100}}[mV]$$



$$\sigma_{\Delta(Vin-Vref)} = \frac{10}{\sqrt{200}}[mV]$$

END lecture 5a

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