Welcome to
046188 Winter semester 2012
Mixed Signal Electronic Circuits
Instructor: Dr. M. Moyal

Lecture 04

Jitter and Noise in Mixed Signal (Converters, and analog blocks).

1. Jitter + few examples (summary lect1-3)
2. Noise sources in Mixed Signal
3. Passives elements in Silicon

www.gigalogchip.com

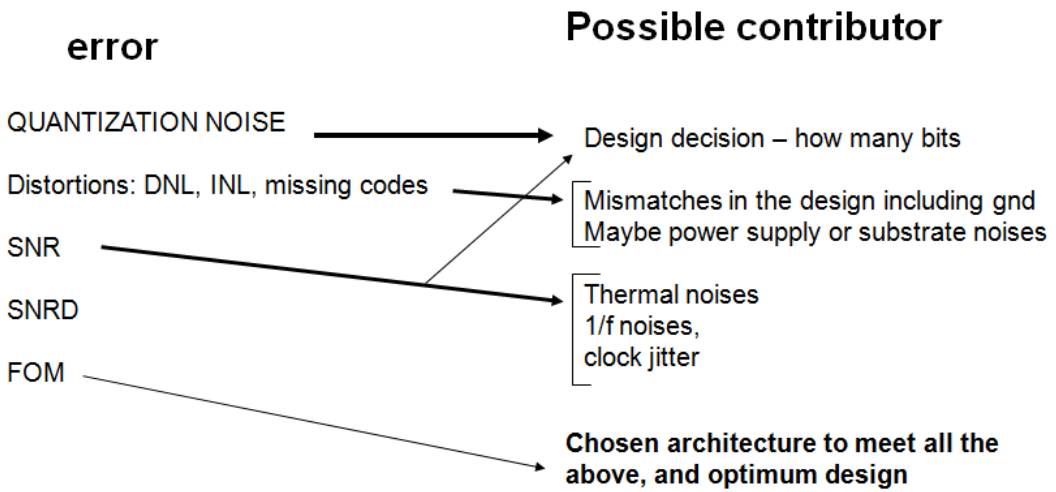
Quick-Summary lect. 2,3

number of bits n	S/N Accurate dB	S/N n 6.02 + 1.76 dB
1	6.31	7.78
2	13.30	13.80
3	19.52	19.82
4	25.59	25.84
5	31.65	31.86
6	37.70	37.88
7	43.76	43.90
8	49.82	49.92
9	55.87	55.94
10	61.93	61.96

Table 1.1: S/N as a function of the number of bits n

The signal-to-noise of an n-bit converter is accurately modeled with:

$$S/N(n) = \frac{A_1}{A_{quantization}} = \frac{2^{n-1} + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_1(2m\pi 2^{n-1})}{\sqrt{\sum_{q=1}^{\infty} (\sum_{m=1}^{\infty} \frac{2}{m\pi} J_{2q+1}(2m\pi 2^{n-1}))^2}} \quad (1.45)$$

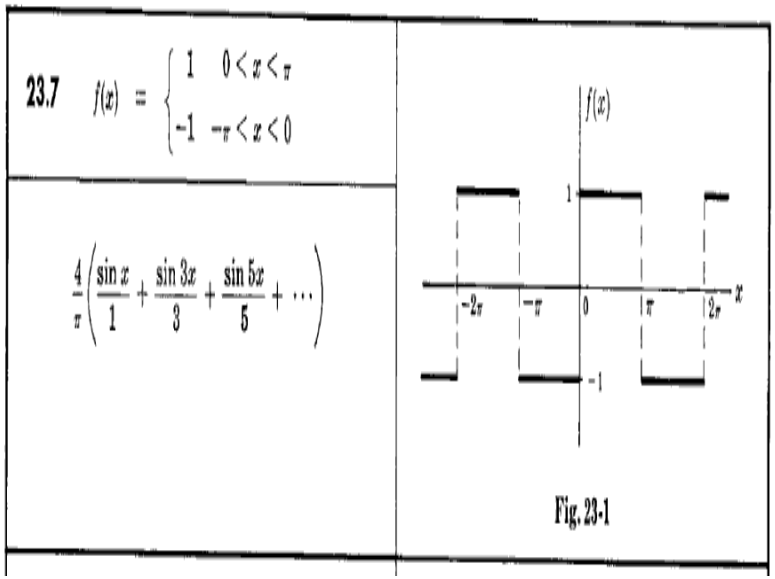


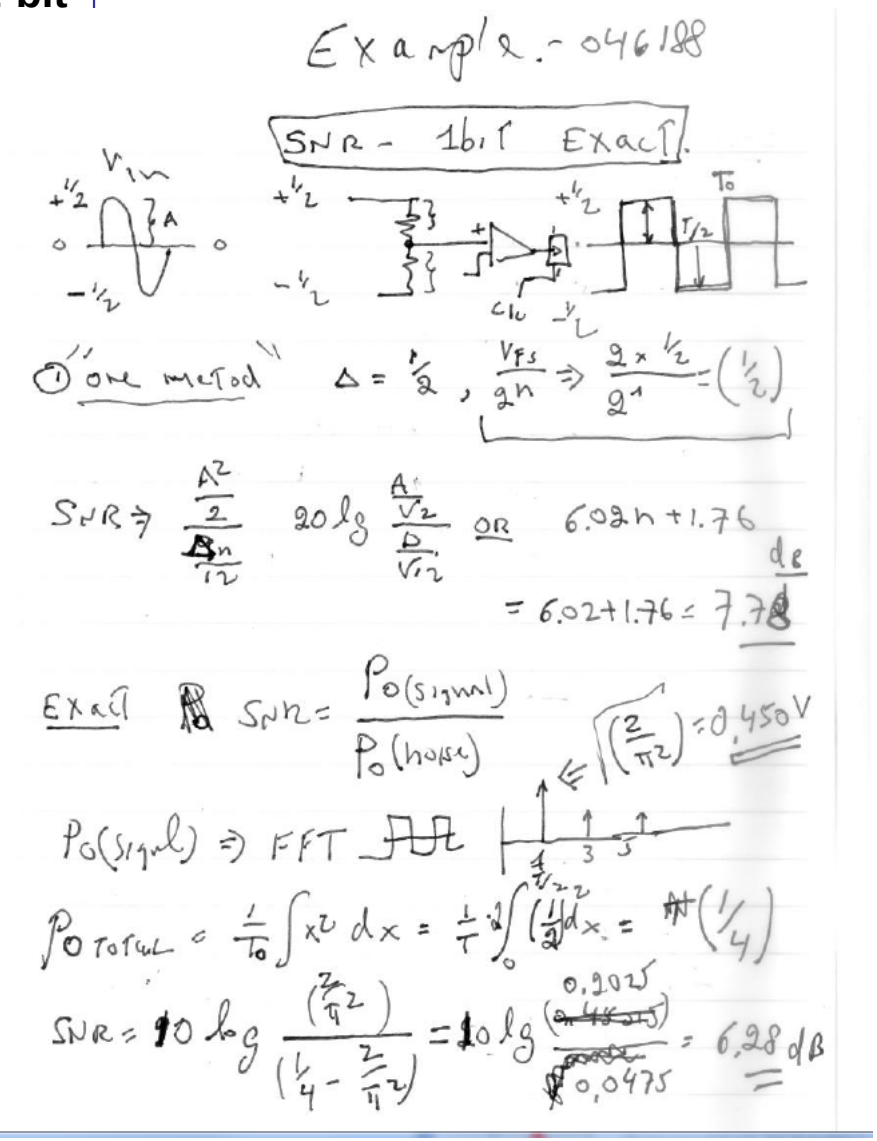
DNL Definition
Differences between two adjacent output digital or analog compared to a step size of LSB weight.

$$ENOBS(bit) \equiv SNDR(effec\ tive) - 1.76 \,/\, 6.02)$$

Industry “Accepted” Formula more correct for >3 bits..

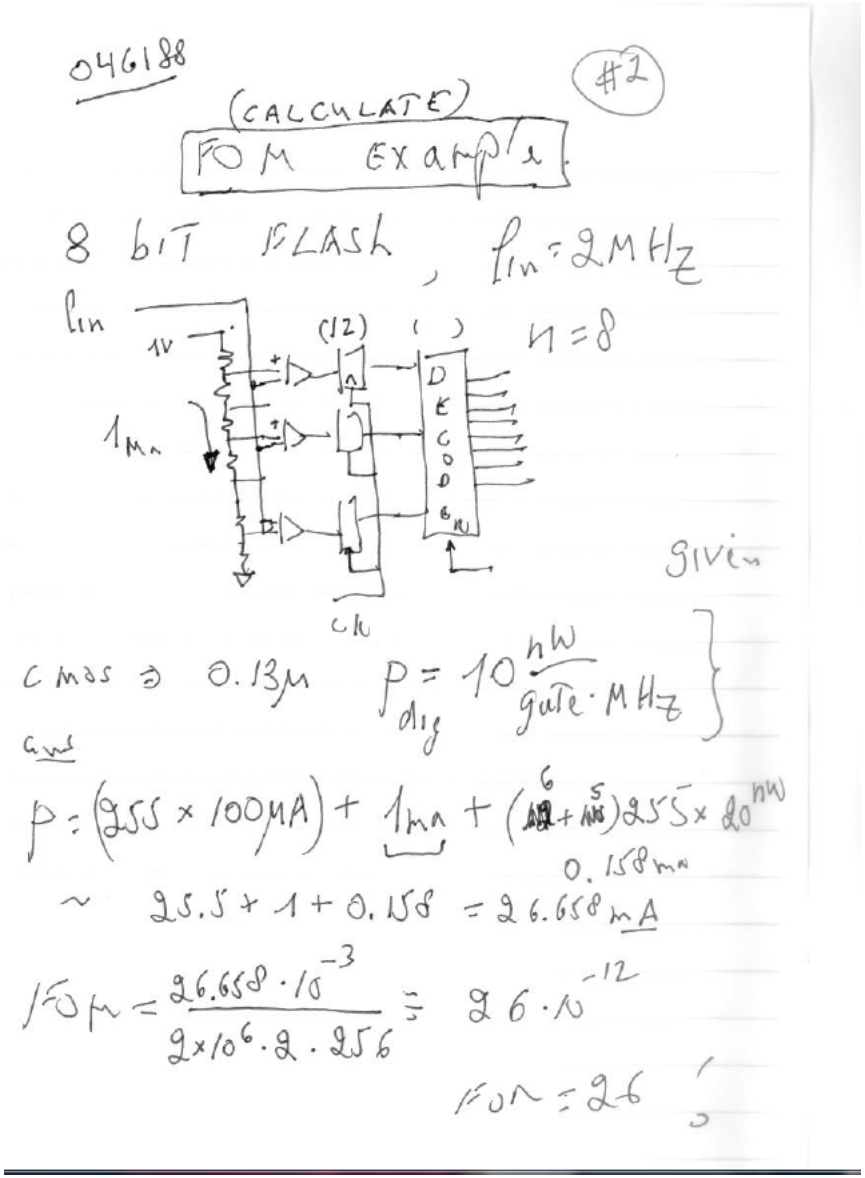
In class derivation example..exact SNR 1-bit

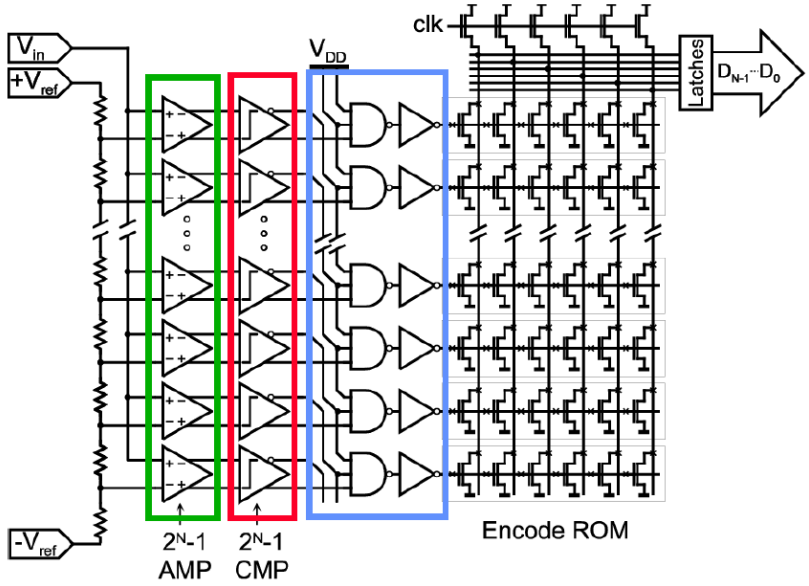




6.28dB is the correct answer not 7.78

In class derivation example..of FOM estimation





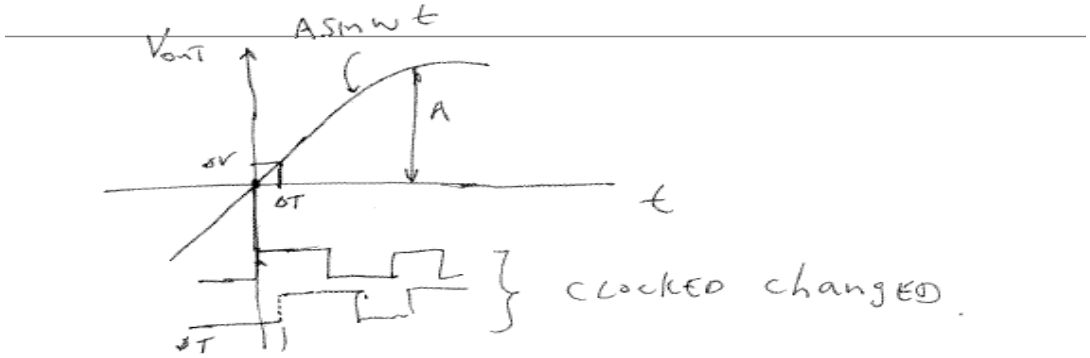
Step1:Inventory: rough est.

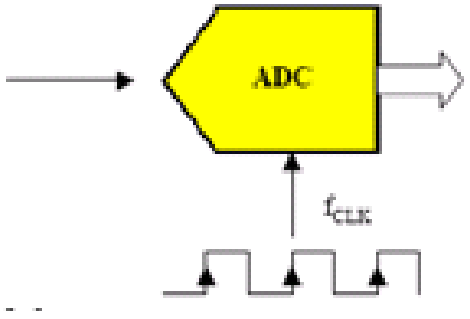
255 comparators, 255 resistors
255 FFs ~3 gates x 255
Thermometer/binary nand+inv+8trans ~3gates x 255
Clock to comp ~ 5/line x 255

Key: MOSTLY COMP POWER Why 100Ua/COMP ?

CLOCK JITTER EFFECT IN CONVERTERS

SAmpling TIME UNCERTAINTY





ΔT = JITTER

A = Signal amplitude $S_{INPUT} \Rightarrow A\sin\omega t$

SEARCH FOR MAX ΔV bnT $\Delta V \leq 1LSB$

$$\left.\frac{\Delta V}{\Delta T}\right|_{MAX} = \left.\frac{dv}{dt}\right|_{t=0} = A\omega\cos\omega t = A\omega$$

bnT $2A$ = CONVERTER RANGE $\Rightarrow LSB = \frac{2A}{2^n}$

FIND t_{JITTER} THAN NEVER COARSE TO GO OVER LSB

$$\frac{\Delta V}{\Delta T_{max}} = A\omega$$

$$\Delta T_{max} = \frac{\Delta SB \cdot 2}{\omega \cdot gn \cdot \Delta SB} = \frac{1}{\pi f_{in} \cdot 2^n}$$

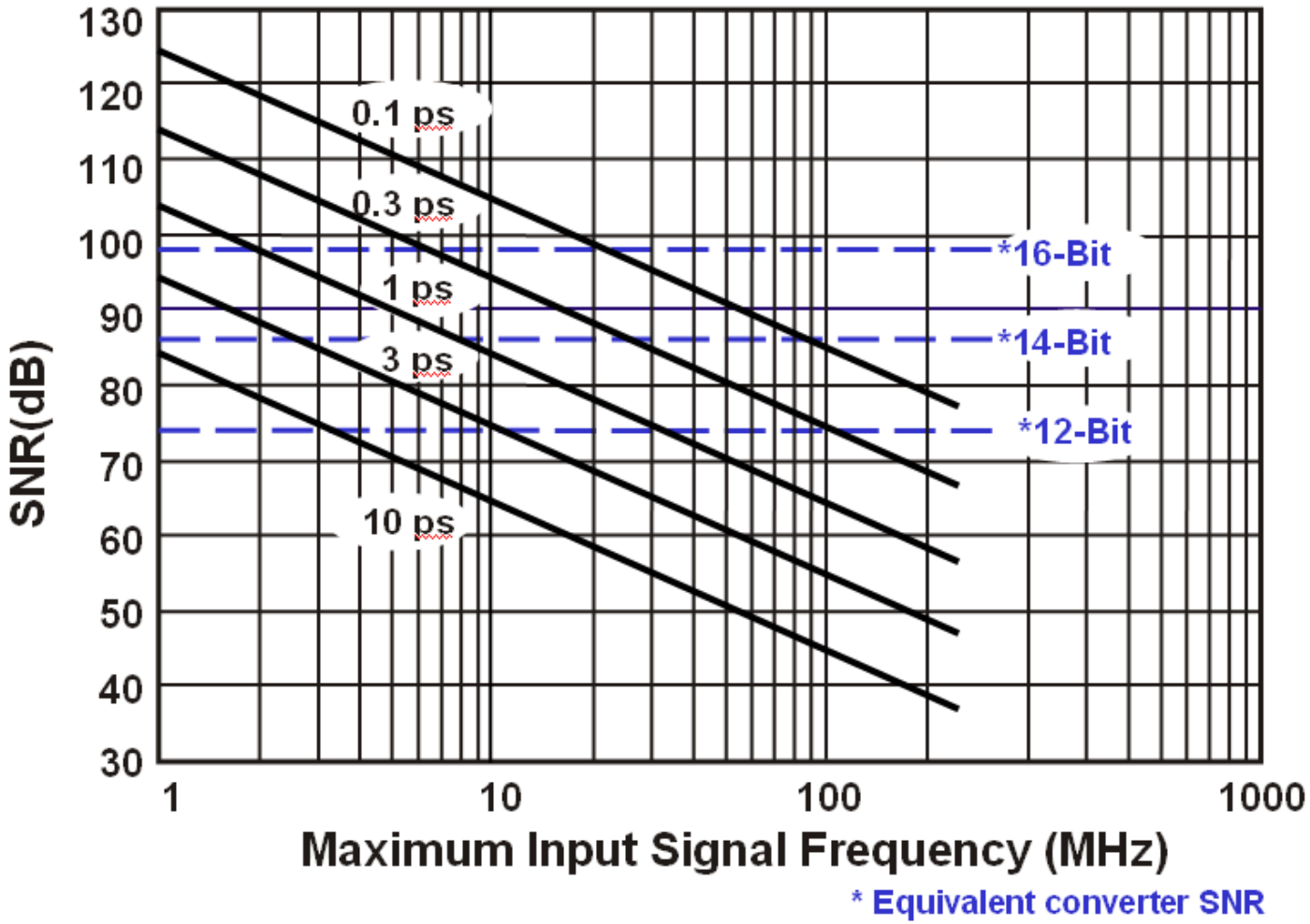
ΔT_{max} = Peak To peak clock uncertainty

bits	ΔT_{max}	
10	31ps	$f_{in} = 10MHz$
12	7.77 ps	
14	1.9 ps	
19	0.19ps	400MHz

TODAY PLL's $\Rightarrow \sim 2 - 20$ ps pk-pk

KEY: SNR due to jitter ifs input frequency dpepndent !

Jitter Limits



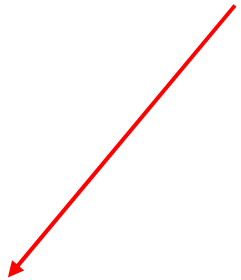
It is clear that the Clock effect is on high changing input (higer frequency..

But..
It is unclear where in the frequency lies this error ?
Random ?

How does it correlate to Phase noise ?

Part of the project is to plot spectrum of the Jitter..

Noise In Resistors and CMOS Transistors



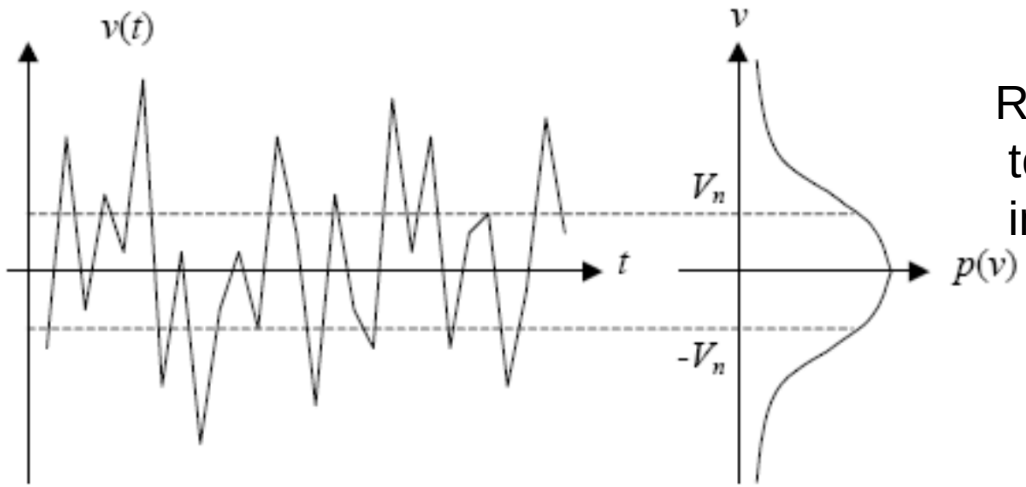
Noise set the fundamental limits of performance

Basics of Noise

Thermal energy in the device causes random charge carrier fluctuations, called thermal noise.

Thermal noise is considered
a “white” noise source because its power spectral density (PSD) is independent of frequency up to about ft (or the BW of the device).

We observe Voltage or Current noise of time and construct the PDF function

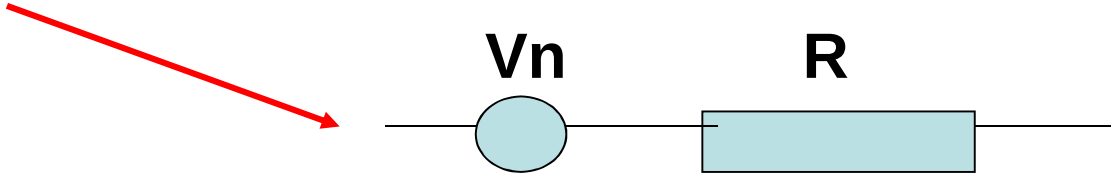


Root mean square is a way to quantify noise and as density in nV (mV) per square root Hz.

Source: T.H.Lee

Example: A resistor thermal noise

MODEL



Take KT=26mv x 1.6e-19C = 41.6 e-22 v square /ohm Hz
The model is a resistor with a voltage source
4KTR units are VxV/Hz

Can Take the square root – noise density Sn)

$$V_{noise}^2 = 4 \cdot k \cdot T \cdot R \cdot \Delta f$$

$$1K\Omega => 4.09 \cdot (\eta V / \sqrt{Hz})$$

NOISE EFFECT IN CMOS TRANSISTORS

MOS Noise

For MOS, We define 2 type of noises,

Two noise mechanism:

Thermal noise – white noise up to ft of the device
Flicker noise – low frequency noise (not so low for Nmos)

It possible that in one mode or another 1/f is almost nulled

There exists other type of definitions for noise – Phase Noise, Electron Noise (ENC)
Which are all derivatives or impacted from the basic Fliker and thermal noise (Mixing)

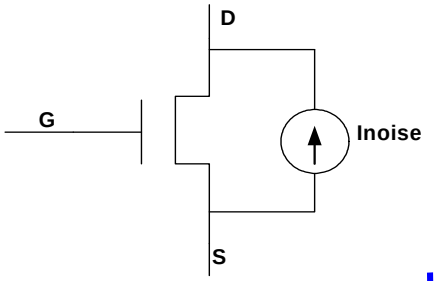
Thermal noise: Thermal energy in the device causes random charge carrier fluctuations, called thermal noise.

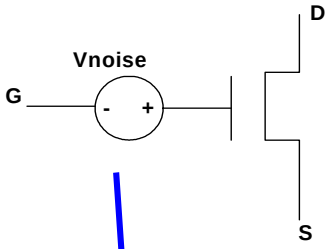
Thermal noise is considered
a "white" noise source because its power spectral density (PSD) is independent of frequency up to about ft (or the BW of the device).

Flicker noise: results from random motion of charge over potential barrier (need a gate).

Transistor Thermal and 1/f Noise

Gamma a process number ~1-2)





on class derive I noise

$$I_{noise}^2 = (2/3)4 \cdot k \cdot T \cdot \gamma \cdot g_m \cdot \Delta f$$

$$V_{in\_noise}^2 = \frac{(2/3) \bullet 4 \cdot k \cdot T \cdot \gamma}{g_m} \cdot \Delta f$$

Thermal

$$I_{noise}^2 = \frac{Ko \cdot k \cdot T \cdot gm \bullet gm}{W \bullet L \bullet f} \cdot \Delta f \sim \frac{1}{L \bullet L \bullet f} \cdot \Delta f$$

function of L2 not W

$$V_{in\_noise}^2 = \frac{Ko \bullet \cdot k \cdot T}{W \bullet L \bullet f} \cdot \Delta f$$

“1/f”

function of gm (sqrt W/L)

A model
For a voltage mode device (input referred noise)
For current mode device (a current source)

METAL OXIDE SEMICONDUCTOR FET (MOSFET)

The equivalent input noise voltage density of a metal oxide semiconductor FET (MOSFET) can be expressed as:

$$e_n^2 = 4kT\frac{2}{3g_m} + K_4\frac{1}{f}\cdot\frac{1}{W \cdot L}$$

Sum it up ! In nch
1/f corner ~50-500Hz

Noise and frequency

$$V_{in\_noise}^2 = \frac{(2/3) \bullet 4 \cdot k \cdot T \cdot \gamma}{g_m} \cdot \Delta f$$

The total noise (input referred) is always the area under the density noise curve the integral from f=0 to f="your design system uses"- hard to tell

Noise in not always flat in all frequency

Example: the total thermal noise from 1KHz-10MHz noise is:

$$V_{totalto1-10Mhz\_noise} = \sqrt{\frac{(2/3) \bullet 4 \cdot k \cdot T \cdot \gamma}{g_m}} \bullet \sqrt{9.999000}$$

Noise as W ,L , gm

as voltage mode:

Thermal noise:
Vn2 /del f = 8 KT/3 gm use large w/l and gm →lower noise

1/f noise
Vn2 /del f = Ko KT / f W L use large area W XL → lower noise

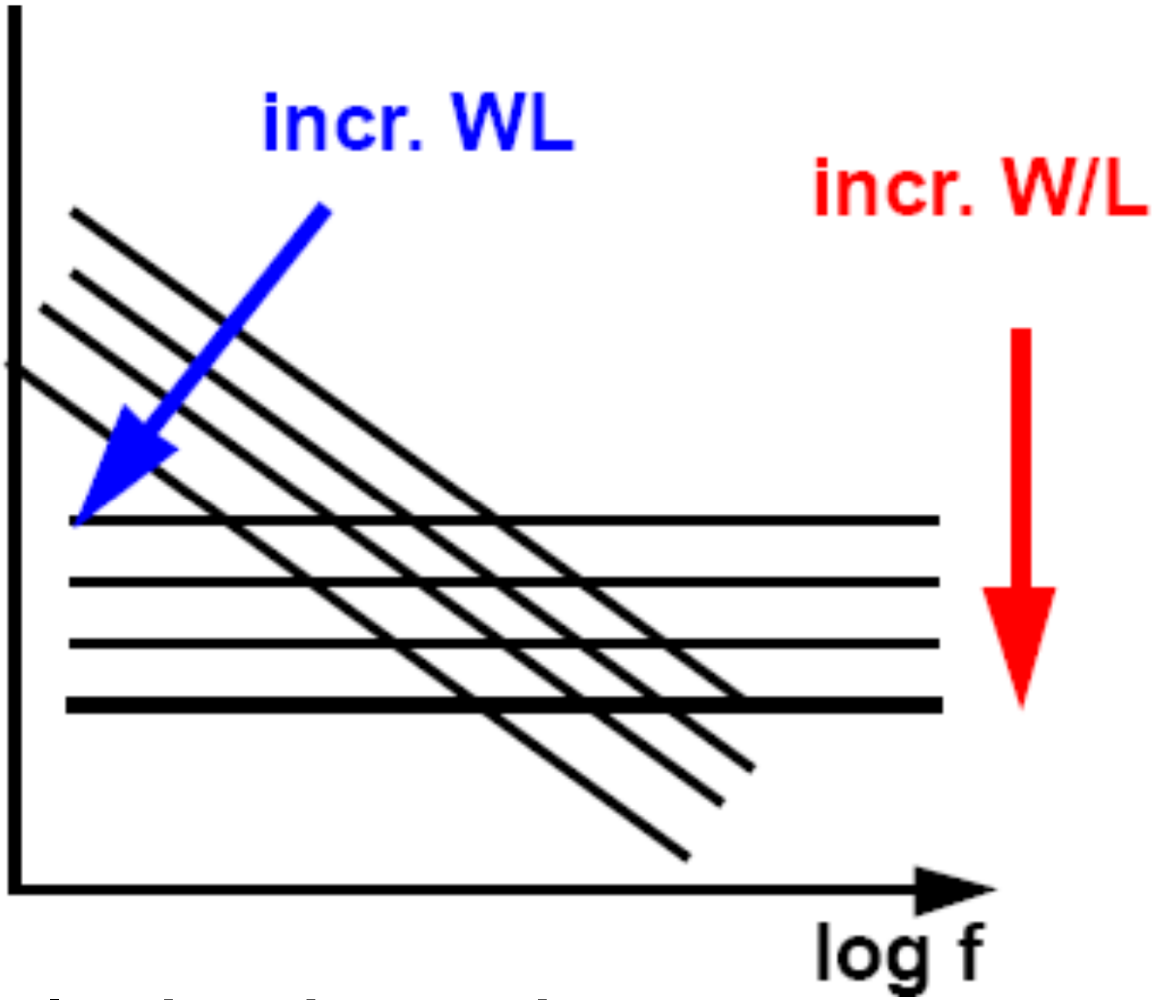
Drain current noise

In^2 /del f = 8 KT gm/3 function of gm (sqrt W/L)

In^2 /del f = Ko KT gm^2/ f W L function of L^2 not W

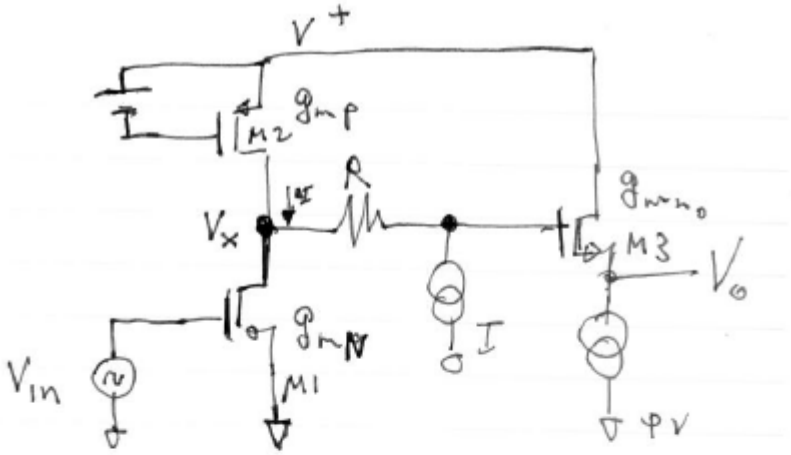
For fixed Ids in strong inversion (Voltage mode)

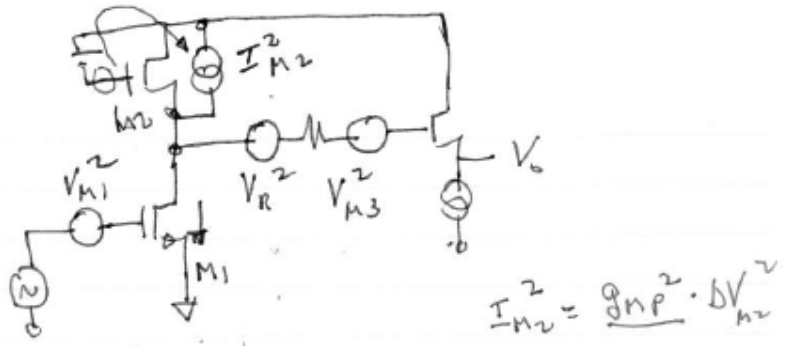
$V / \sqrt{Hz}$



fliker and thermal noises interactions

Example 1ckt noise of 2 gain stages – in class





$$I_{M2}^2 = g_{mp}^2 \cdot \Delta V_{M2}^2$$

→ what TOTAL input related noise AT moderate f (consider Thermal noise)

→ effect/consideration for conversion?

$$V_{M1}^2 = \frac{8}{3}\frac{kT}{g_{mN}} \qquad g_m = \sqrt{kC\frac{W}{L}I}$$

$$V_{M2}^2 = \frac{8}{3}\frac{kT}{g_{mp}}$$

$$V_R^2 = 4kT \cdot R \qquad V_x = V_{in}\, g_{mN}\left(R_{o_{M2}} \| R_{o_N}\right)$$

$$V_{M3}^2 = \frac{8}{3}\frac{kT}{g_{mn_0}} \qquad \Delta I = g_{m_1} \cdot \Delta V_{in}$$

TOTAL "input" noise

$$\sqrt{V_{M1}^2 + \frac{I_{M2}^2}{g_{M1}^2} + \frac{V_R^2 + V_{M3}}{g_{M1}^2 \cdot \left(R_{o_{M1}} \| R_{oM2}\right)^2}}$$

$$V_{in} = \sqrt{\frac{8}{3}\frac{kT}{g_{M1}} + \frac{\frac{8}{3}kT\left[g_{mp}^2\right]}{g_{M1}^2 / g_{mp}} + \frac{4kTR + \frac{8}{3}kT/g_{M3}}{g_{M1}^2 \cdot \left(R_{o_{M1}} \| R_{oM2}\right)^2}}$$

↑ LARGA

↑ "1/3" + SMALL

MAKE g_{mN} ↑ W↑ L↓

MAKE g_{mp} - LOW ↓

FOR ADC DAC

$$f_{NL} \sim \frac{1}{2}LSB \Rightarrow \frac{V_{FS}}{g_m} \sim \frac{1}{2}V_{in} \cdot (BW)$$

Passive RC in Silicon

and MISMATCHES

Mismatches

One of the most critical parameters in Mixes signal design.

Mostly ignored with normal simulators

Si passive Elements Used in Mixed Signal

Silicon Resistors:

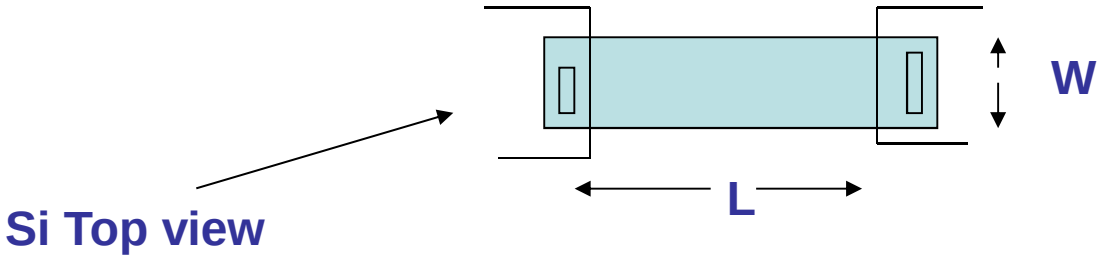
In Silicon **R** = Sheet resistance x Number of square.
Made of Si doped material.(poly and N+ or P+ or both.)

Problems: They have parasitic capacitances, (BW limitation) and Temperature variations :

R=v/i

$$R = Rs \bullet squares\,(1+\alpha T/To)$$

$$R \propto 1/(\mu qNa)$$



Polysilicon

Grown from pyrolytic decomposition of silane (SiH_4) at about 600°C.

The polycrystalline structure is made of monocrystal grains size in the range of 0.1 - 1 µm.

The typical layer are 200 - 600 nm thick with long term standard deviation in the 2% range.

The mobility is low because of the grain border resistance (30-40 cm^2/Vs).

In order to have a low sheet resistance the polysilicon must be strongly doped (10^{20}-10^{21} cm^{-3}). Part of the doping saturates the localized levels due to the grain border. The sheet resistance is in the range 20 - 40 Ω/□.

The sheet resistance can be reduced by using sandwich layers (polysilicide) made of 200 nm of polysilicon covered with a film of refractory metal silicide (WSi_2, $MoSi_2$, $TiSi_2$). The sheet resistance is reduced to 1 - 5 Ω/□.

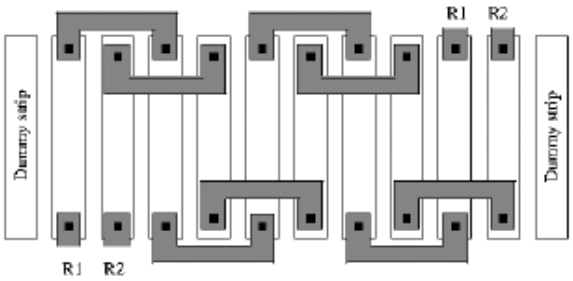
PASSIVE element tolerance

Common type of resistors in IC - silicon

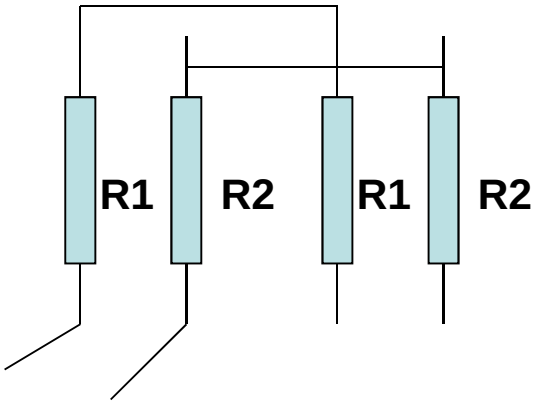
RESISTOR	Range	0hm/sq Value	% (1x1uu) matching	ppm/c ,ppm/v temco
Poly				
No siliside	+/-15%	200-1k	2%	0-400 ppm/c
With siliside		6	-	-
N+/P+	+/-20%	20-100		3000ppm/c, large v.
N well	+/- 20%	2k-4k	--	large
1 Contact	+/- 50%	1-3 ohm	---	----

Layout of resistors in silicon

Interdigitized structure :



Good matching

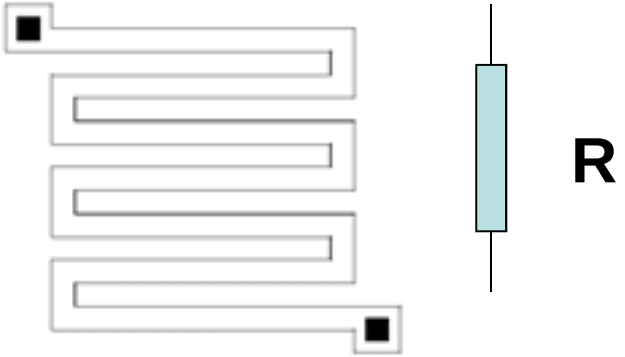


symbol

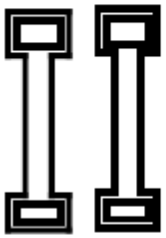
$$R = Rs \bullet length/width$$

$$Rtotal = R + 0.5Rs(numberturns) +$$

+ Contact resistance

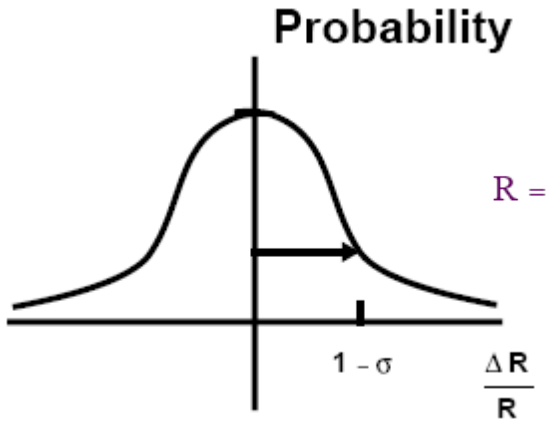


mismatches

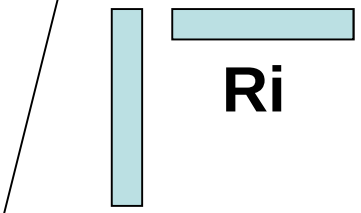


$$R = \frac{R_1 + R_2}{2}$$

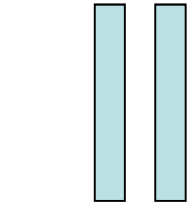
$$\Delta R = R_1 - R_2$$

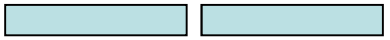


$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$



Ri





$$\left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)^2 + \left(\frac{\Delta x_j}{x_j}\right)^2$$

mismatches

$\left(\frac{\Delta x_j}{x_j}\right)$

- Implant dose
- Side diffusivity
- Deposition rate

$\left(\frac{\Delta L}{L}\right); \left(\frac{\Delta W}{W}\right)$

- Etching
- Boundary
- Side diffusivity

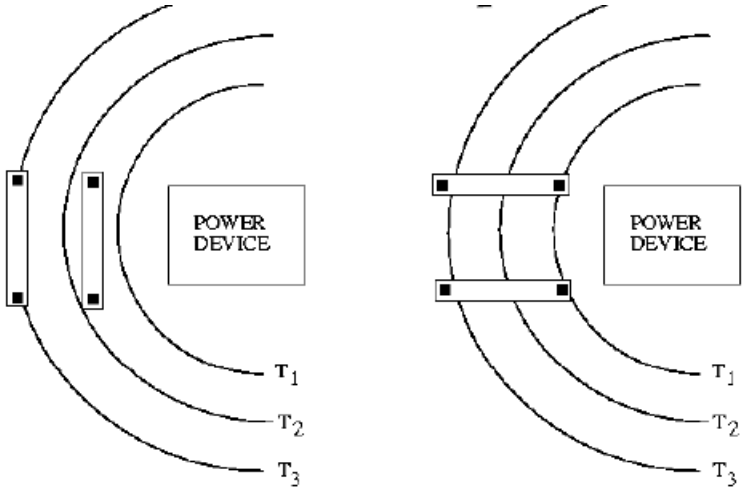
$\left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)$

- Polysilicon grain size
- Doping dose
- Crystal defects
- Stress
- Temperature

source: F. Maloberti

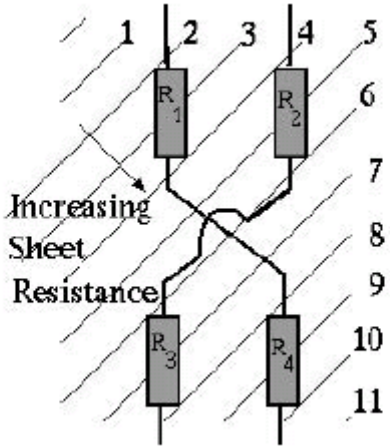
Improve mismatch (accuracy) errors : “good to do”

A- temperature:

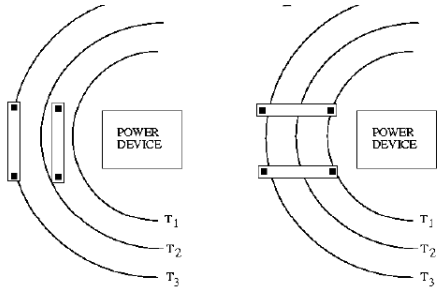


source: F. Maloberti

B- sheet resistance



"James C. Daly et al."



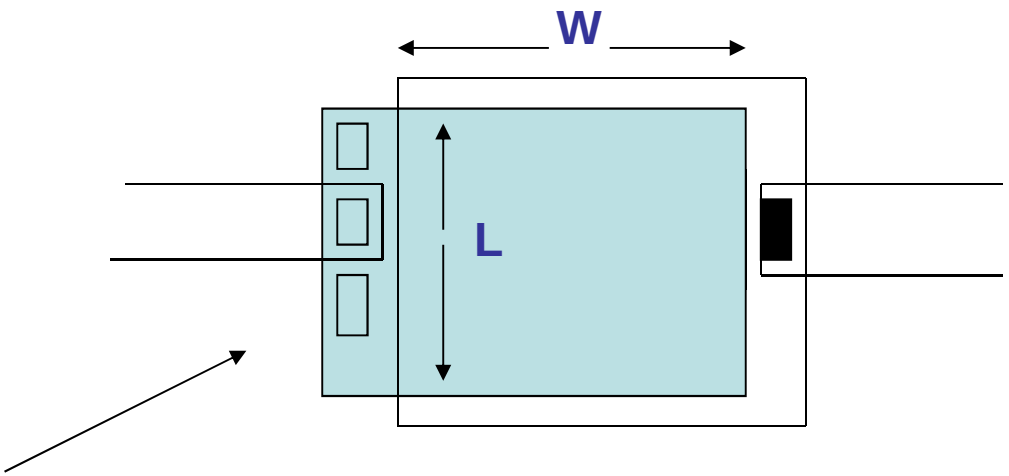
C) STRESS: away from edges..

Capacitors

Plated Capacitors

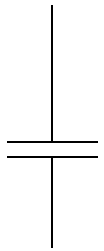
C= Ca x Area = Ca x W x L (W and L are dimension of plates)
1-4 ff/uu can. 20pF is already a large capacitors for Si application.

“Core Oxide caps”- will be reviewed later lectures.



Si Top view

i=C dv/dt



Capacitors

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

From here to here..

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

Insulator ~Si02

$$y = \frac{x_1 \cdot x_2}{x_3}$$

Look @

$$\frac{\partial y}{y} = ?$$

$$\left.\frac{\partial y}{y}\right|_{x_1} = \frac{\left(\frac{x_1}{x_3}\right) \cdot \partial x_2}{\left(\frac{x_1}{x_3}\right) x_2} = \frac{\partial x_2}{x_2}$$

$$\left.\frac{\partial y}{y}\right|_{x_2} = \frac{\partial x_2}{x_2}$$

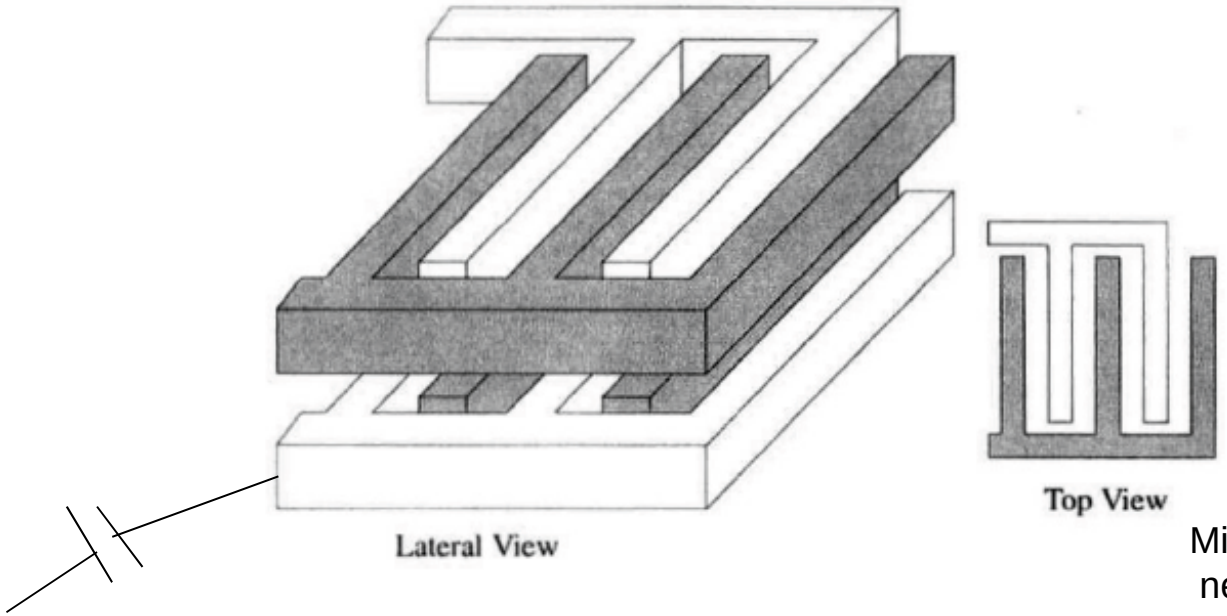
$$\left.\frac{\partial y}{y}\right|_{x_3} = \frac{x_1 x_2 x_3^{-2} \partial x_3 (-1)}{\left(\frac{x_1 x_2}{x_3}\right) 1} = \frac{-1}{x_3} \partial x_3$$

$$\left[\frac{\partial y}{y}\right]^2 = \left(\frac{\partial x_1}{x_1}\right)^2 + \left(\frac{\partial x_2}{x_2}\right)^2 + \left(\frac{\partial x_3}{x_3}\right)^2$$

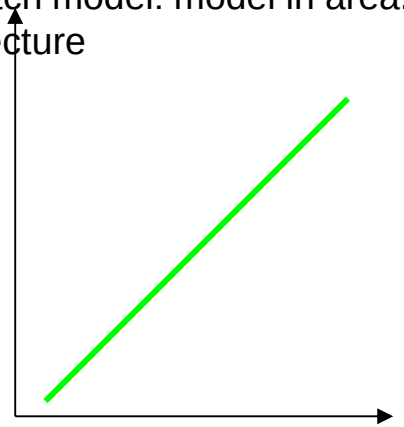
Mismatch model: know, but ignore the above use pelgrom rule !
Given mismatch for certain area everything and 4 time the area means double the matching- next lecture...

Metal Capacitors

METAL THICKNESS 2000-5000A



Mismatch model: model in area.. – next lecture



Example : 1-2 e-3 pF/uu
Variations = +/- 20%
Matching dc/c→ 10ff => 0.8%
Temco~0
C to Csub (parasitic) ~ 15:1

END lecture 04

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