Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

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TEL AVIV UNIVERSITY אוניברסיטת תל אביב

Lectures
http://www.gigalogchip.com/lectures.html

Lecture 4

Sample (Track) and Hold

Agenda

Part I : SAMPLING SAMPLE AND HOLD

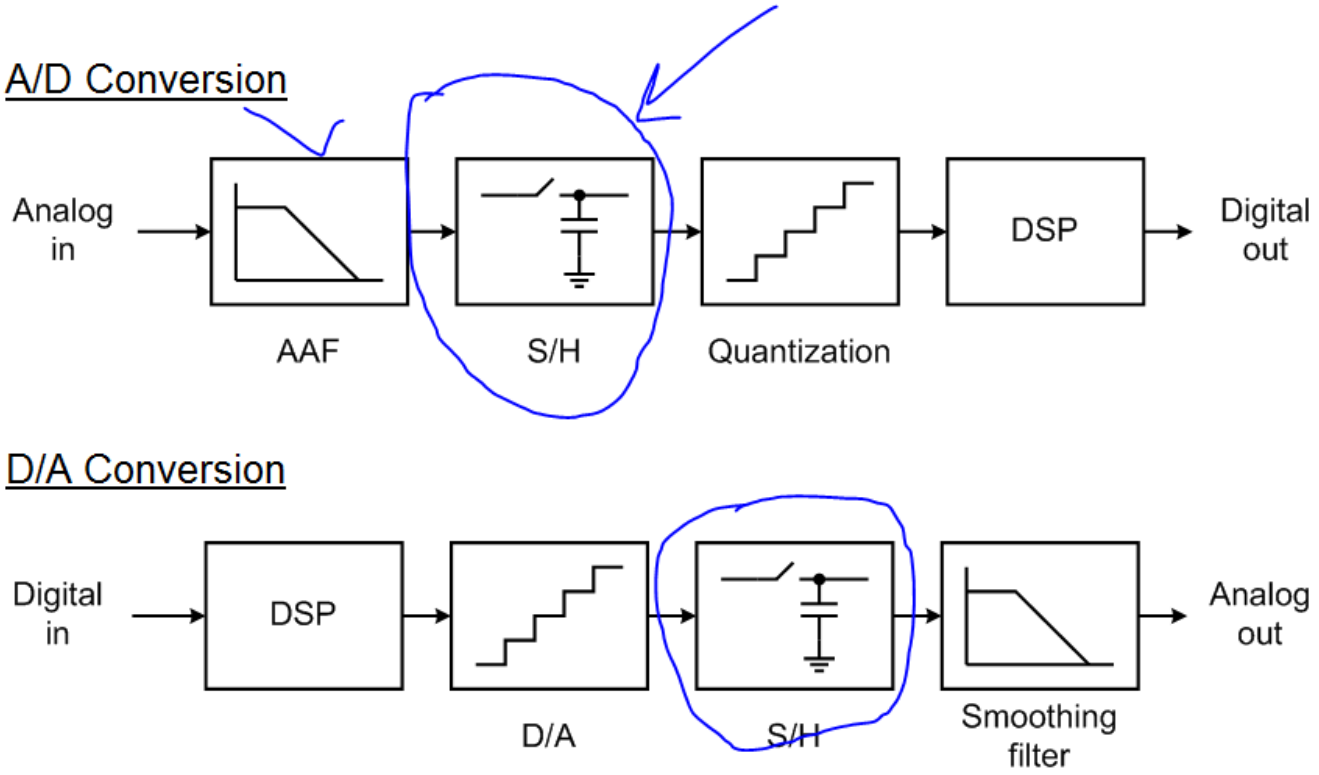
Part II : THE MOS SWITCH

Part III: S/H DISTORTION

Part IV: S/H CIRCUITS

Part V: S/H ACCOMPANYING BUFFERS

A/D and D/A Conversion



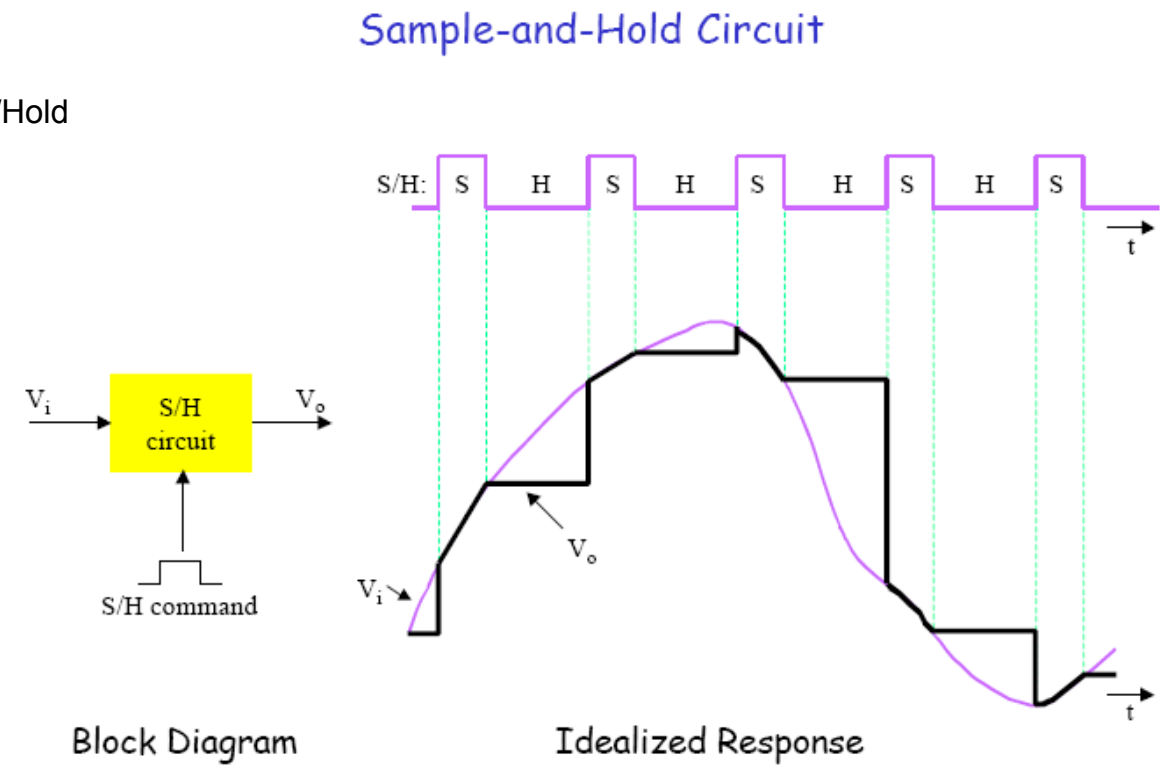
Why we need it

Some ADCs cant do without it

But
In high speed/accuracy it’s the limiting elements in ADCs
It’s the source of KT/C Noise and Harmonics
It’s one more source effected by clock jitter input
It’s the source of Power consumption (maybe the highest)

Part I : SAMPLING WITH SAMPLE AND HOLD SAMPLE/Trach AND HOLD –OPERATION

What does Track/Hold
Look like ?



Source: Analog MS centre TAMU

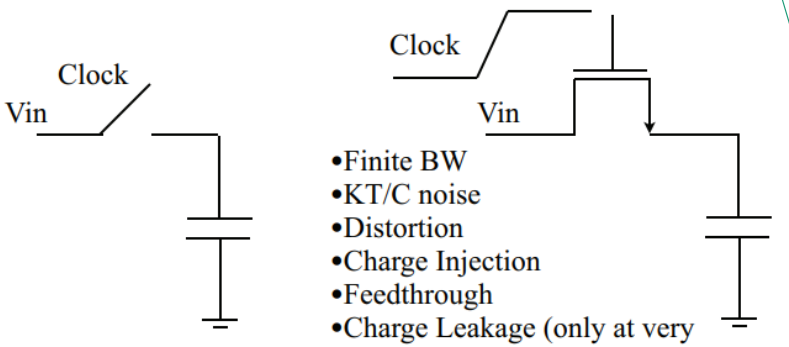
SAMPLING:

The Sample and hold keeps the Analog value fixed for a clock duration.

The MOS switch how to minimize error?

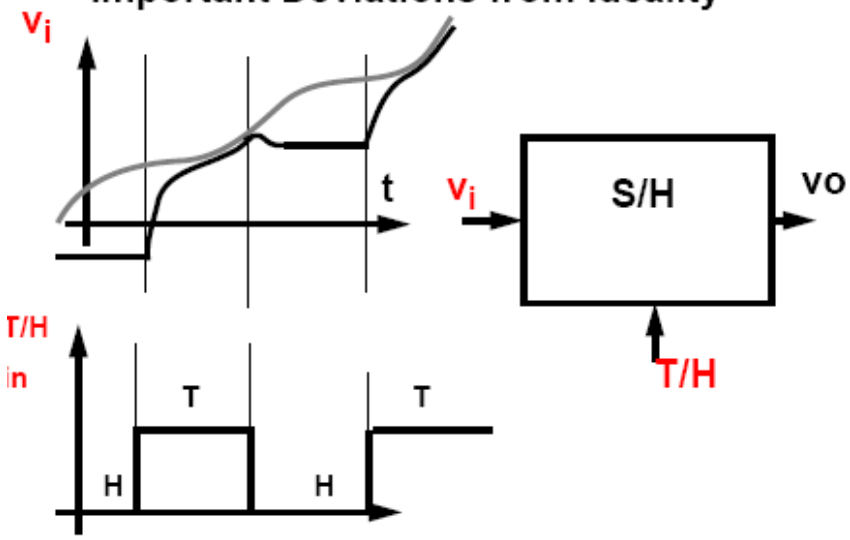
Ideal VS Real S/H

•Impulse-train sampling

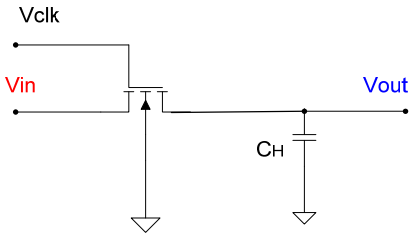


•Finite BW
•KT/C noise
•Distortion
•Charge Injection
•Feedthrough
•Charge Leakage (only at very low speed)

Important Deviations from Ideality



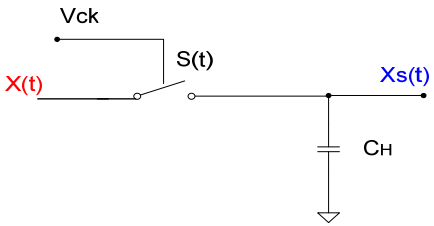
1. Hold to Track Transition
   - Finite acquisition time
2. Track Mode
   - DC offset
   - Finite Bandwidth
3. Track-Hold Transition
   - S/H Offset
   - Aperture Delay
   - Aperture Jitter
4. Hold Mode
   - Droop

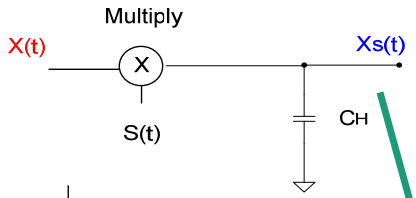


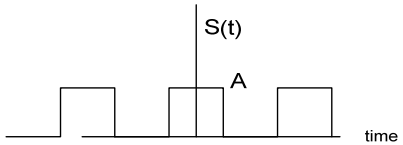
↘ **fundamental performance limits**

Frequency domain transfer function ←
Sample Jitter and clock jitter
Acquisition Time, Sample BW
Droop and Feed through
KT/C noise
Linearity Real Performance limits- distortions
Charge Injections
Apparatus time
PSRR

Fourier transform of S/H system Sampling- Basics





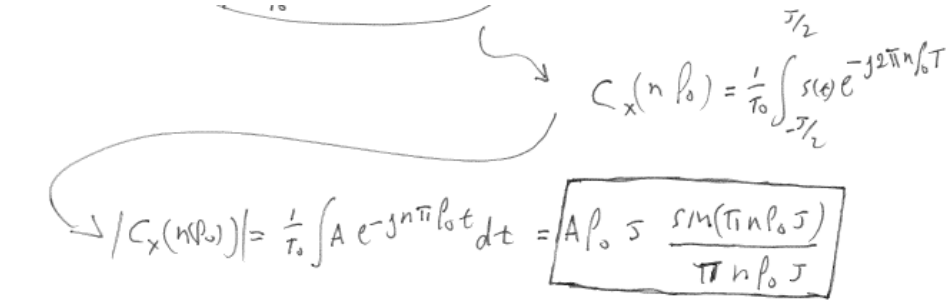


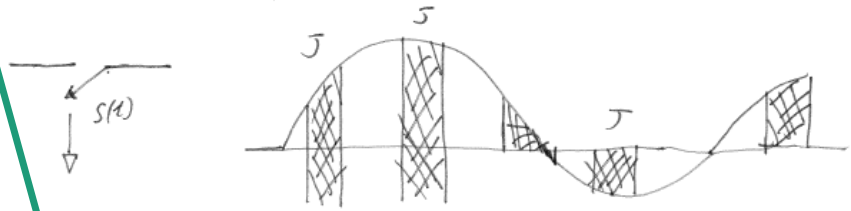
fs

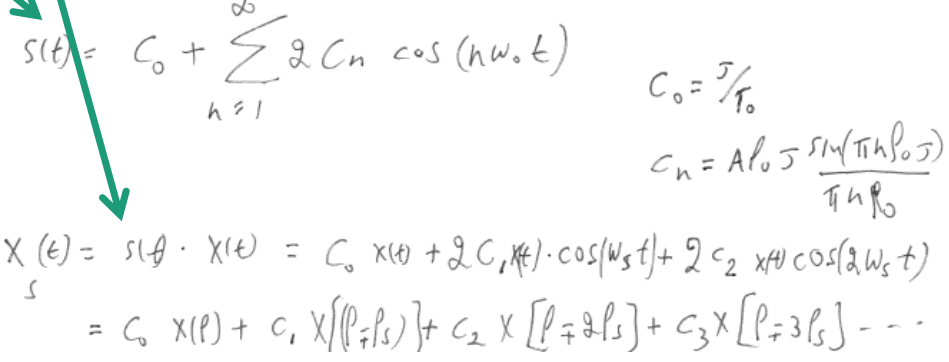
Do fft only on the hold area for tau length or on the tau section ..?

Vck is a clock at rate fo , fs

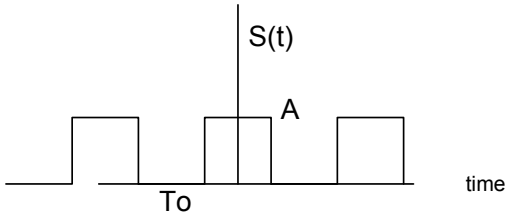
More details proof on lect. adc

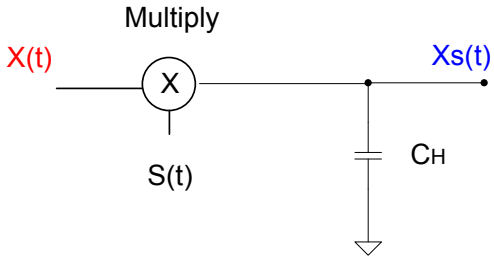


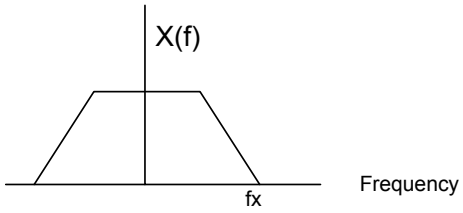


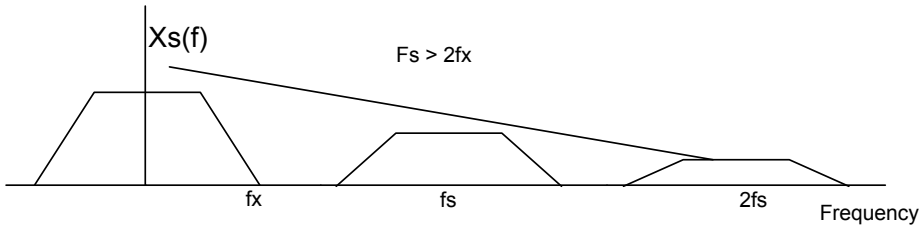


Frequency domain view









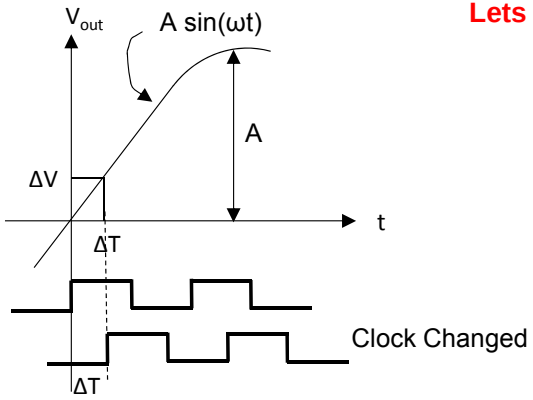
Key: Its also a filter…
But with folding.

So now we need to make sure fs farther than fx.- more on adc lect.

Sampling inaccuracy – Jitter

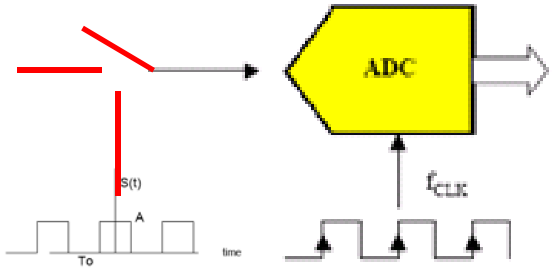
The TH is ideal but the clock is changing…

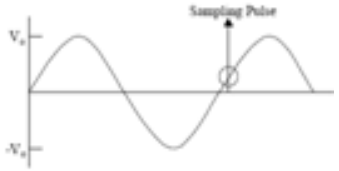
Jitter error – what will it do to a converter? – name it : Apparatus Error



Lets say the input is a pure sine wave

Sampling Time Uncertainty





ΔT = Jitter = t jitter
A = Signal Amplitude = A sin(ωt)

Search for Max ΔV, but ΔV ≤ 1LSB

$$\left.\frac{\Delta V}{\Delta T}\right|_{max} = \left.\frac{dV}{dT}\right|_{t=0} = A\omega \cos \omega t = A\omega$$

But:
2A = Converter Range → $LSB = \frac{2A}{2^n - 1}$

Find t_{Jitter} that don't let it cause more than an LSB or error.. (actually I use ¼.

Jitter effect: calculation

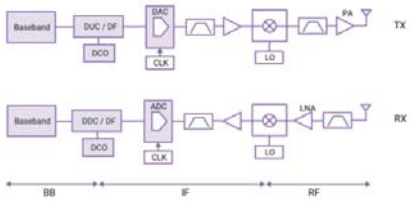
$$\left.\frac{\Delta V}{\Delta T}\right|_{max} = A\omega$$

$$\left.\Delta T\right|_{max} = \frac{LSB \cdot 2}{\omega \cdot 2^n \cdot LSB} = \frac{1}{\pi f_{in} 2^n}$$

$\Delta T|_{max}$ = Peak-to-Peak Clock Uncertainty

n=Bits	Δt_{max} [ps]	
10	31	f_{in} = 10MHz
12	7.77	
14	1.9	
12	0.19	f_{in} = 400MHz

This is **Jitter.. (depends on f input)**



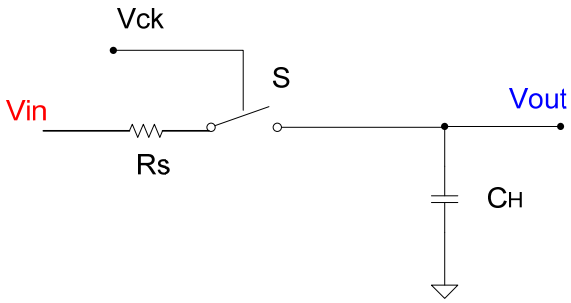
Key: Its worth case Reality you need phase noise…

What adc jitter needed for wifi-5G ?
3-4Gsps

WiFi/5G coordinate on unlicensed brands

53 e-15 ?

As for today, PLLs are ≈ 1-2ps.. below 100fs is hard to build



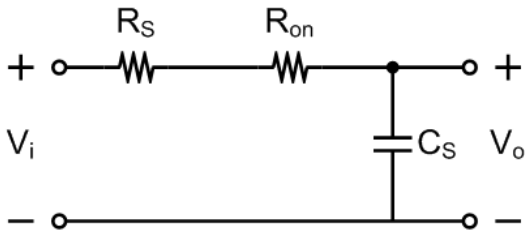
Simple model with source resistor

Small signal BW – Assuming we can charge the capacitor

f-3db = 1 / (2 pi RsCh)– cont. see page 15

Rs can be the driver resistance, and the switch, can vary
Ch- is load capacitance amplifier ? Comparator ? Wiring ?

Why we care ? – to catch the signal … acquisition. Time..
If we don't catch it ?



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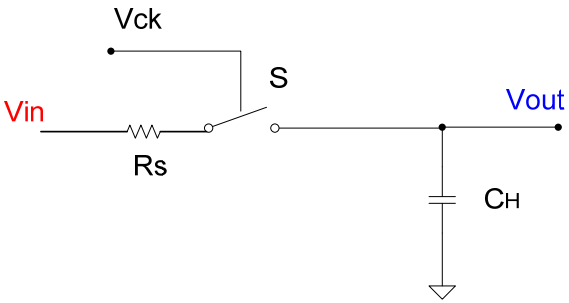
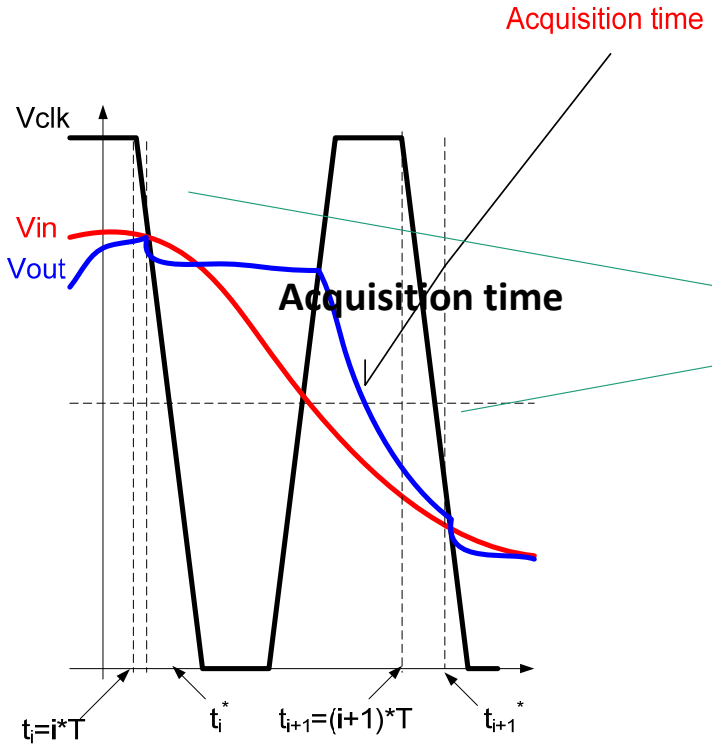
$$TBW = 1/(R_S + R_{on})C_S$$

Acquisition time





The problem the switch is the source and the clock is the gate

Remember the place of the two –Vt makes an off region..

Example acquisition time

Acquisition: For a step input the response is

Vout = (delV) (1-exp(-1/RsCh))

I max is at t=0 and it is Vmax=Vin-Vout

Imax = (Vmax) / Rs -----→ 50 ohm / 0.5v/2pf = 10mA

Here we don't deal with R switch or lump its maximum with Rs to be less than 50 ohm

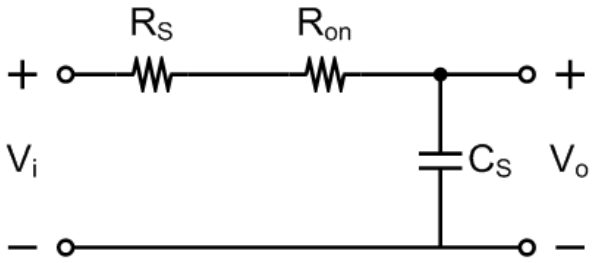
Accuracy Vs. Acquisition time

1% = 4.6 RsCh
0.1% = 6.9 RsCh = 10 bit
0.01% = 9.2 RsCh =1/10000 = 13.28 bit

In reality the input is moving, BW limited, and it is not a step input

if the input is **current limited** them the output is slewing at a rate of dVout / dt = Iin/Ch

Acquisition Time (t_{acq})



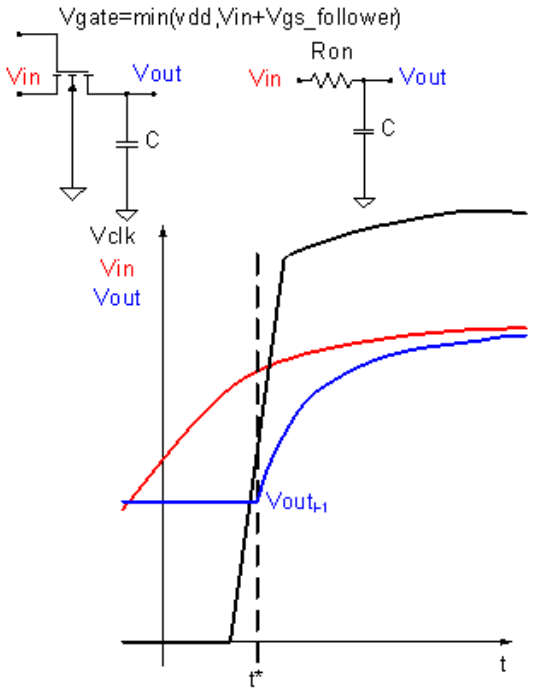
Accuracy	t_{acq}
1% (7b)	≥ 5τ
0.1% (10b)	≥ 7τ
0.01% (13b)	≥ 9τ

$$\tau = \frac{1}{TBW} = (R_S + R_{on})C_S$$

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th} - V_i)} = \frac{L^2}{\mu C_{ox} WL(V_{DD} - V_{th} - V_i)} = \frac{L^2}{\mu Q_{ch}}$$

Short L, thin t_{ox}, large W, large V_{ov}, and small V_i help reduce R_{on}

Complete form solution



Tracking/settling error calculation:

$$Vin(t) = Vcm + A\sin(2\pi f_{in} t)$$

$$Vin(t) = Vout(t) + Ron \cdot C\frac{\partial Vout}{\partial t} \qquad t = t^* \Rightarrow Vout = Vout_{i-1} \cong Vin\left(t^* - \frac{1}{2\,fsmp}\right)$$

Forced solution:

$$Vout^f(t) = Vcm + \frac{A\sin\left[2\pi f_{in} t - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}}$$

Homogenous solution:

$$Vout^h(t) = B \cdot e^{-\frac{t-t^*}{R_{on}C}}$$

Solution:

$$Vout(t) = Vout^h(t) + Vout^f(t)$$

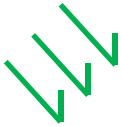
Set initial condition (determine B):

$$B = Vout_{i-1} - Vcm - \frac{A\sin\left[2\pi f_{in} t^* - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}} \cong$$

$$\cong \frac{A\sin\left[2\pi f_{in}\left(t^* - \frac{1}{2f_{smp}}\right) - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}} - \frac{A\sin\left[2\pi f_{in} t^* - \arctan(2\pi f_{in} R_{on} C)\right]}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}}$$

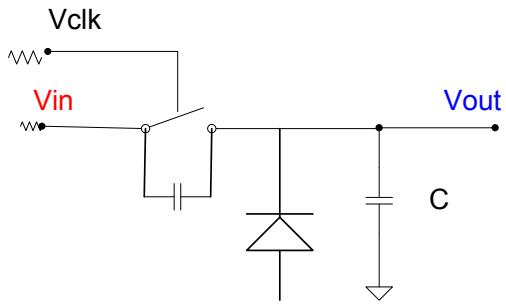
$$= \frac{-2A}{\sqrt{1+4\pi^2 f_{in}^2 R_{on}^2 C^2}}\cos\left[2\pi f_{in}\left(t^* - \frac{1}{4f_{smp}}\right) - \arctan(2\pi f_{in} R_{on} C)\right]\sin\left(\frac{\pi f_{in}}{2f_{smp}}\right)$$

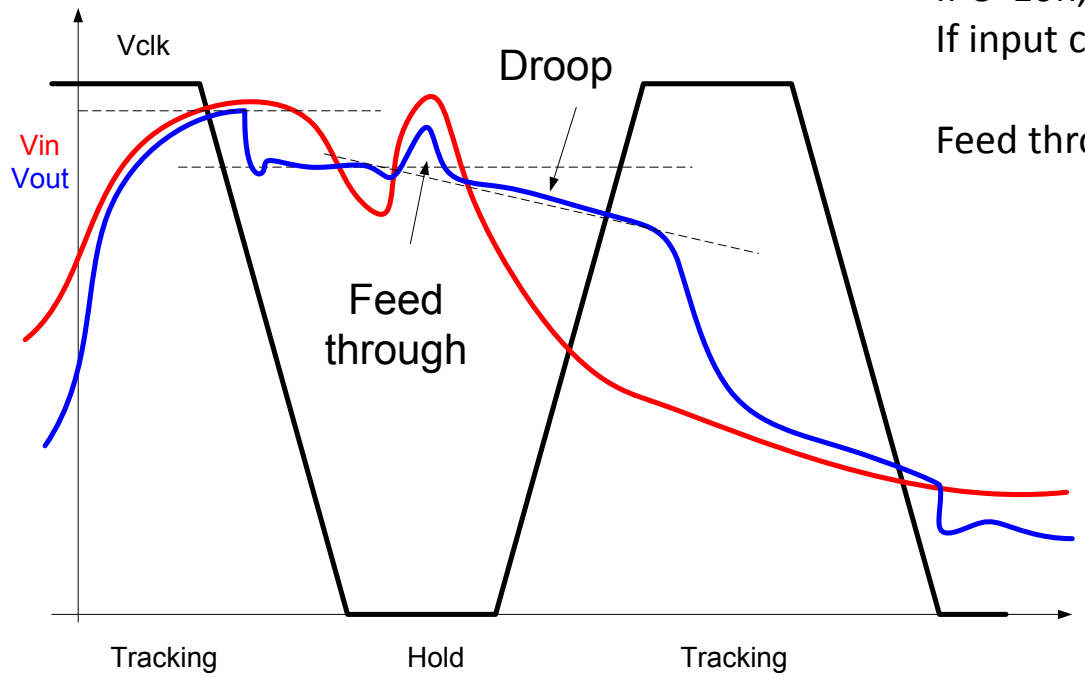
fundamental performance limits



Frequency domain transfer function
Sample Jitter and clock jitter
Acquisition Time, Sample BW
Droop and Feed through
KT/C noise
Real Performance limits
Charge Injections
Capacitive noise from Supply
PSRR
Linearity

Droop Mode and Feed through- MOS Switch





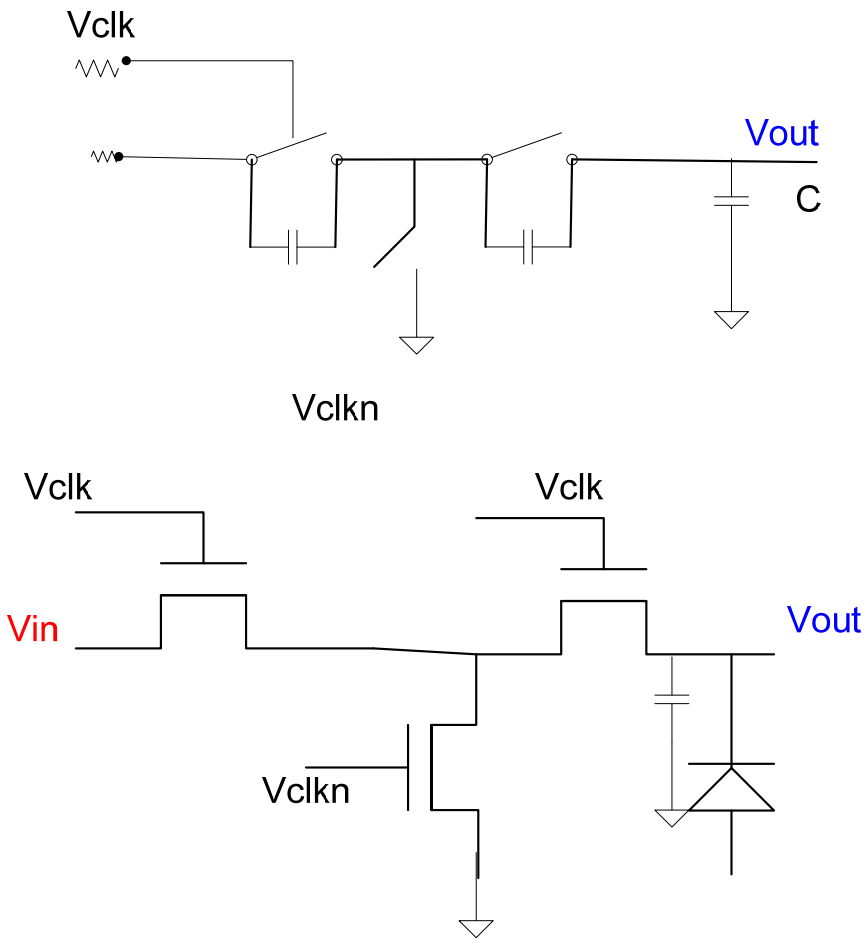
If C=10ff, Idiode=20fA,C=100fF

Drop by 1mv if, (c/i)dV, **off time=0.5ms**

If C=10ff, Idiode=20fA,C=100fF(with diode)
If input change 20mv during hold

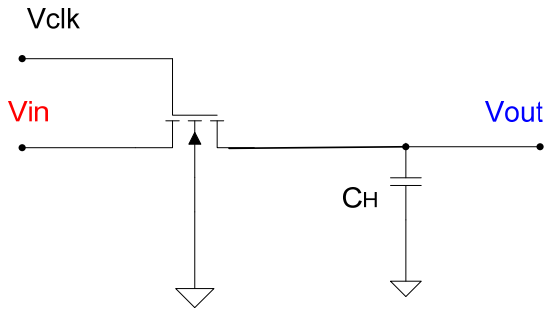
Feed through= “10/110”=1.8mV.

Improved feed-through problem



Cost: double the switch R

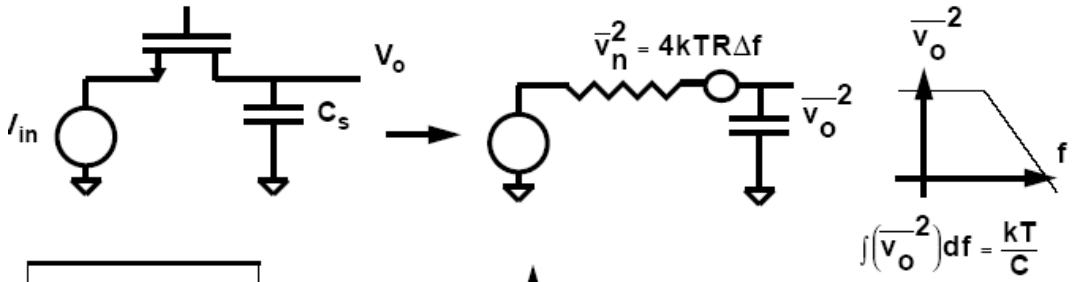
Part II : S/H MOS SWITCH Transistor as switch Basic Configuration:



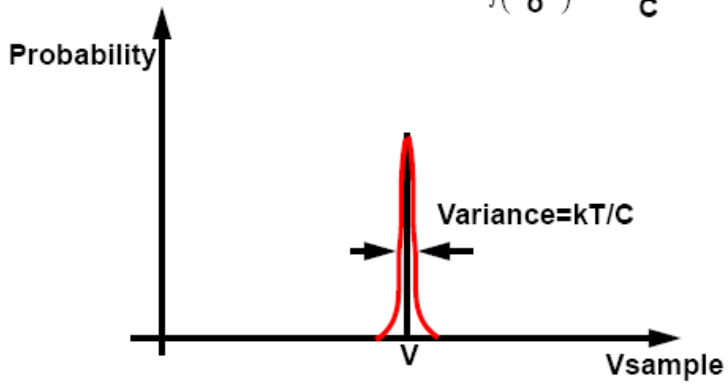
fundamental performance limits

KT/C noise
Real Performance limits
Charge Injections
Capacitive noise from Supply
PSRR
Linearity

kT/C Noise Limitation



C	$\sqrt{\frac{kT}{C}}$
100pF	6.4uV
10pF	21uV
1pF	64uV
100fF	210uV
10fF	0.64mV



Thermal noise:

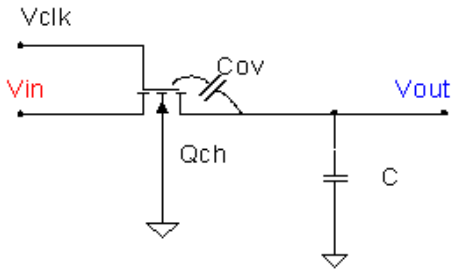
$$\Delta V_{thermal}^2 = \frac{kT}{C}$$

Key : Noise is determined by the hold capacitor.

Example:
0.2V sine wave and 100fF SNR= 56dB

VRms/Vn=141mv/210uV=671➔56dB=9bit

Clock feed through

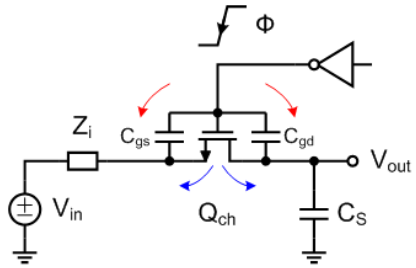


$$\Delta V_{feedthrough} \cong \Delta Vclk \frac{Cov}{C} \cong -vdd \frac{Cov}{C}$$

Its large because Vclk has large swing

Vout change=(Cov/(C+Cov) * Vclk

Cov <<C ..but Vclk is large



	Clock feedthrough (CF)
Fast turn-off	$\Delta V = -\frac{C_{gs}}{C_{gs}+C_S} V_{DD}$
Slow turn-off	$\Delta V = -\frac{C_{gs}}{C_{gs}+C_S}(V_{in}+V_{th})$

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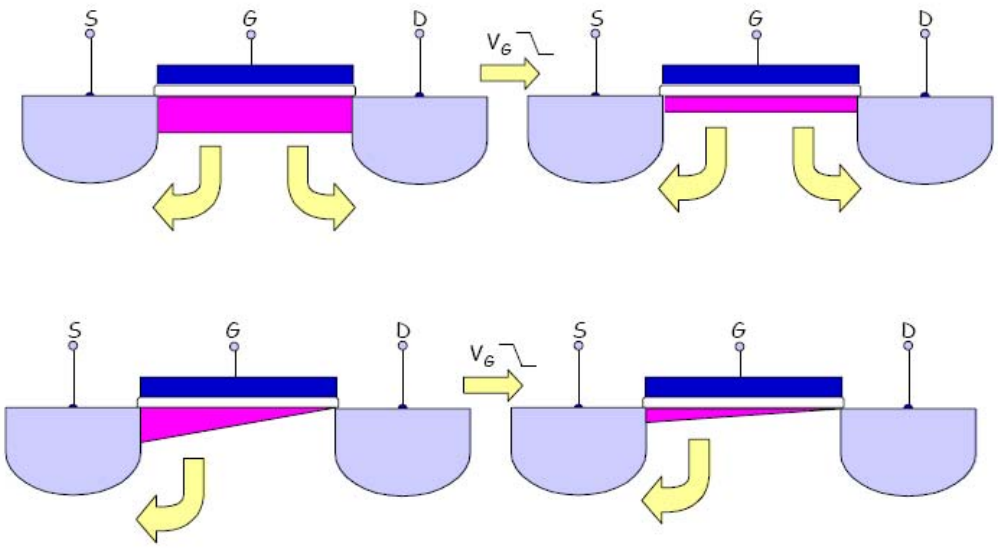
More exact

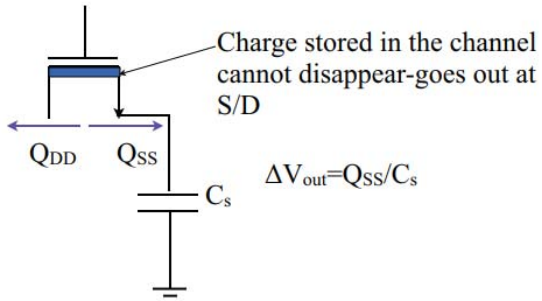
Charge injection from channel

Channel charge in (top) triode and (bottom) saturation



Problem : its function of vin, vgate

Charge Injection



Charge movement in the device..

1. **If the switch is in triode : charge split**

$$Q_{ch} = -WLC_{ox}(V_{GS} - V_T)$$

2. **If the switch in sat all escapes to the source (nothing to th drain) Can we design SH based on sat switch?**
3. **In sat Vdrain source cant reach 0**

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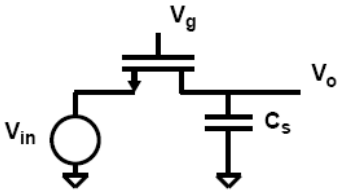
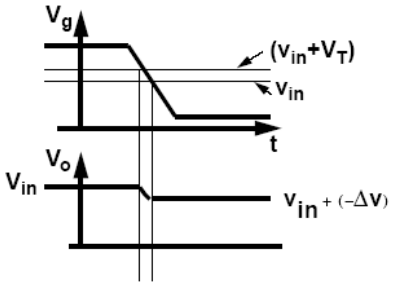
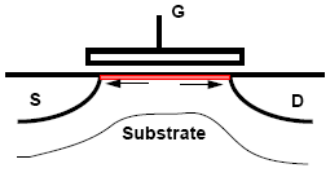
Offset charge injection from channel

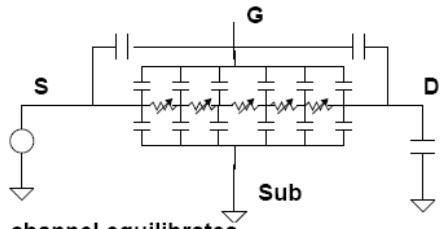
Sample/Hold Offset





What's happening in the device?





Limiting Case1: Slow gate fall time, channel equilibrates

Limiting Case 2: Fast gate fall time, 1/2 of qc goes each way

Sample-and-Hold Basic Architectures

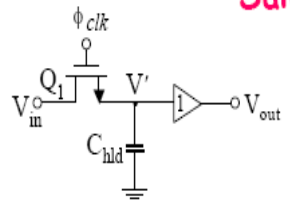


Fig. 1 An open-loop track and hold realized using MOS technology.

Analysis

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{OX}WLV_{eff\text{-}1}}{2}$$

where $V_{eff\text{-}1}$ is given by

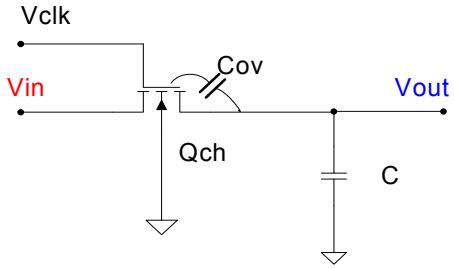
$$V_{eff\text{-}1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in}$$

$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{OX}WLV_{eff\text{-}1}}{2C_{hld}} = -\frac{C_{OX}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}}$$

Charge Injection (very simple model)
(Half the channel charge goes to C):

$$\Delta V_{charge} \cong \frac{Qch}{2C} \cong -\frac{Cox \cdot W \cdot L(Vgs - Vth)}{2C} = -\frac{Cox \cdot W \cdot L(vdd - Vin(t) - Vth(Vin(t)))}{2C}$$

Summary on those 3



$$\Delta V_{feedthrough} \cong \Delta Vclk \frac{Cov}{C} \cong -vdd \frac{Cov}{C}$$

Charge Injection (very simple model)
(Half the channel charge goes to C):

$$\Delta V_{charge} \cong \frac{Qch}{2C} \cong -\frac{Cox \cdot W \cdot L(Vgs - Vth)}{2C} = -\frac{Cox \cdot W \cdot L(vdd - Vin(t) - Vth(Vin(t)))}{2C}$$

Thermal noise:

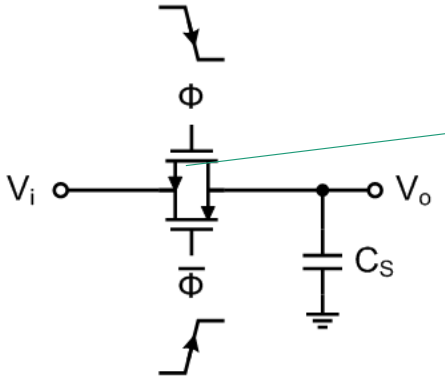
$$\Delta V_{thermal}^2 = \frac{kT}{C}$$

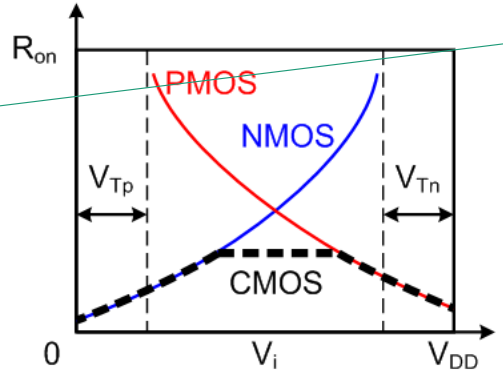
PRACTICAL DESIGN AND IMPLEMENTATIONS

CANCELLATION METHODS

Reduce Ron

CMOS Switch



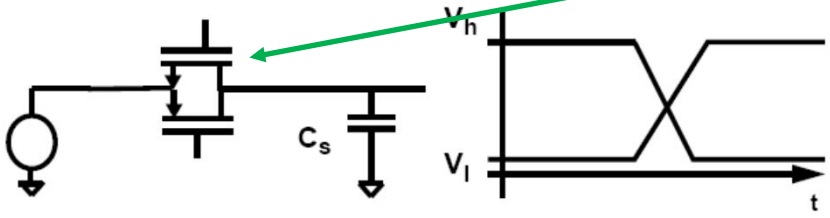


$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th} - V_i)} = \frac{L^2}{\mu C_{ox} WL(V_{DD} - V_{th} - V_i)} = \frac{L^2}{\mu Q_{ch}}$$

Short L, thin t_{ox}, large W, large V_{ov}, and small V_i help reduce R_{on}

- R_{on} still depends on V_{in} and is sensitive to N/P mismatch
- Large parasitic cap due to PMOS switch for symmetric R_{on}
- Clock rising/falling edge alignment

3. Complementary NMOS, PMOS



Assume fast case

$$\frac{1}{2}q_{CN} = \frac{1}{2}(V_H - |V_{TN}| - V_i)W_N L_N C_{oxN}$$

$$\frac{1}{2}q_{CP} = \frac{1}{2}(V_i - |V_{TP}| - V_L)W_P L_P C_{oxP}$$

$$\Delta V = -Vin(1+\varepsilon) + V_{os} \quad \text{where:}$$

$$\varepsilon = \left(\frac{W_P L_P C_{oxP} + W_N L_N C_{oxN}}{C_L}\right) \qquad V_{os} = (V_{OSN} - V_{OSP})\frac{C_{ol}}{C_L}$$

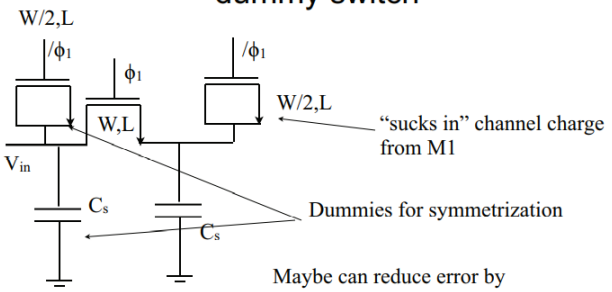
Key Point:

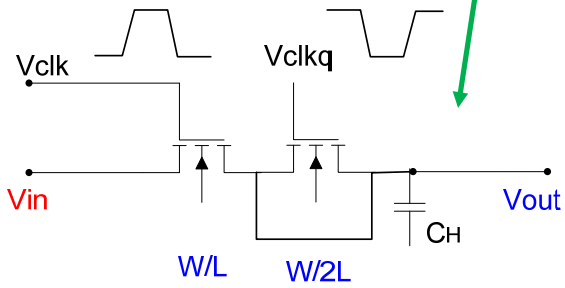
1. Offsets Partially Cancel
2. Gain errors ADD!!

Do this

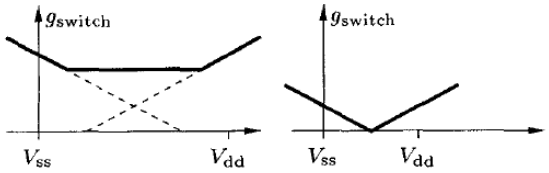
Or this

Charge injection mitigation(1) : dummy switch





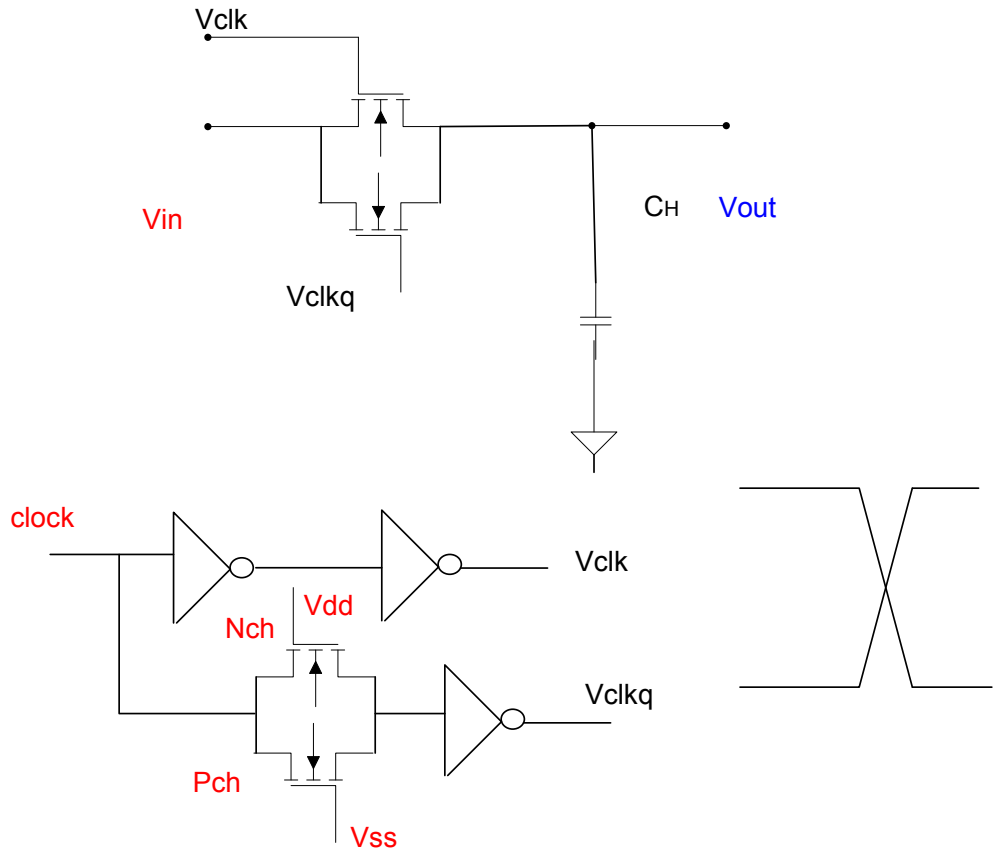
Dummy switch look for balancing clock fall and rise – not possible over all processes



(a) 3-V supply voltage (b) 1.5-V supply voltage

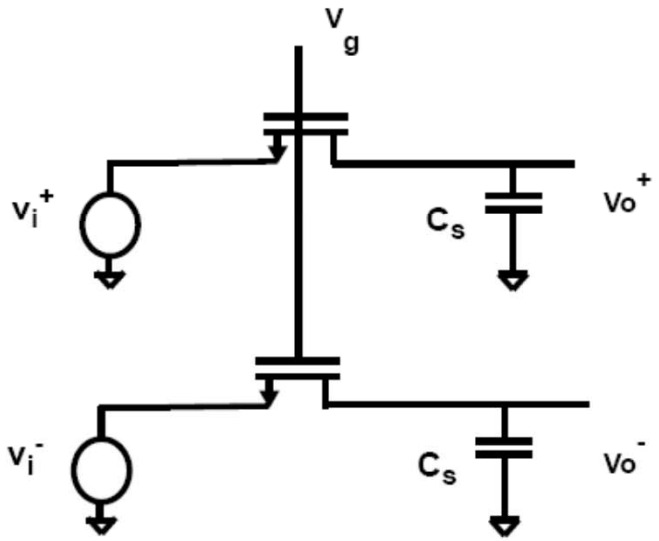
The Switch Ron improves

Balance clock rise and fall time



But this is better

4. Get rid of offset- Go Differential



$$v_{o1} = v_{i1}(1+\varepsilon) + V_{os1}$$

$$v_{o2} = v_{i2}(1+\varepsilon) + V_{os2}$$

$$\Delta v_o = \Delta v_i(1+\varepsilon)$$

Even harmonics eliminated *to large degree*

practical circuits

the biggest problem of all those lies in distortions…

How it all translate to ?

Distortion is the biggest issue

Distortion calculation and simulation

Unfortunately

$$R_{on} \approx R_0 \frac{V_{dd} - V_{th}}{V_{dd} - V_{th} - V_{in}} \longrightarrow \text{Distortion}$$

Bad mostly if $V_{in} > V_{dd}-V_{th}$ (NMOS) or $V_{in} < V_{th}$
[Think of Pass Transitor Logic in 141/241]

Constant Vin $\quad V_{out} \approx V_{in}(1 - e^{\frac{T_s}{2R_0C}(1-\frac{Vin}{V_{dd}-V_{th}})})$

Remember competing effects large w/l to reduce Ron but charge injection grow as w&l

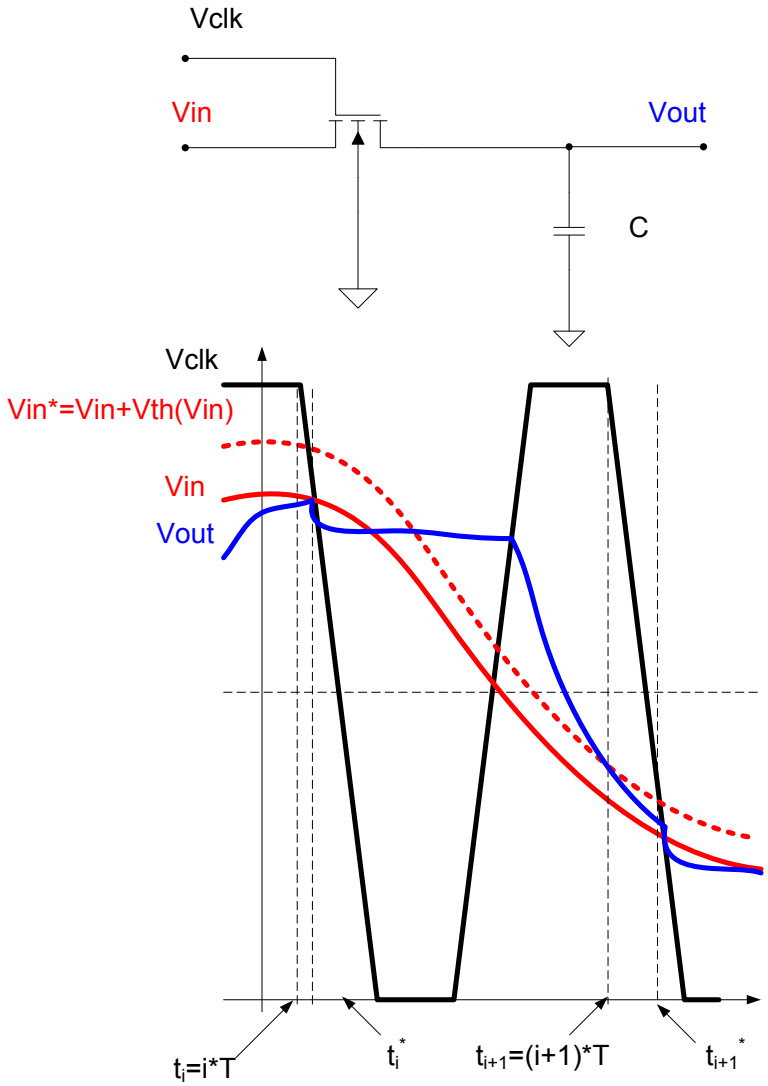
Lets combine all er**rors that related to input or output they all leads to non linearities…**

1) **Do first pss sim- its fast and will let you know if the switch impedance is ok**

you are lucky to get 80dB for 5GHz

1) **Then do fft on the results output- if bad either start taking vare of all issues**
2) **Optimize base in 1, 2 :Size, devices, use differentially, p and n in parallel**
3) **Then if not meet spec(fft) .. go to gate boosting..**

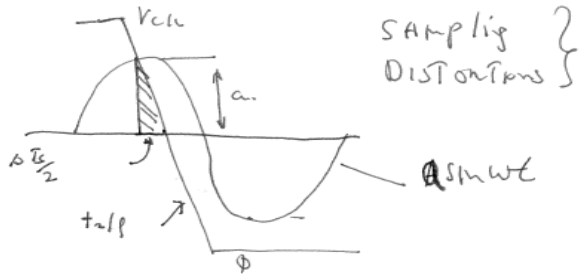
Aperture time accuracy - Pictorial view



The time when hold start is not the same on time

Distortion due to sampling time (apparatus time accuracy) calculations

Single mode



SAMPLIG DISTORTIONS

$\Delta T_{MX} = \frac{\Delta t_s}{2} = \left(\frac{a}{V_{clk}}\right) t_{rlp}$

$t_{rlp} \Rightarrow$ VERY SMALL w sin wt $\ll \frac{1}{\Delta T}$

IF Input $V_{in} = a \sin wt$

$\Delta T = \left(\frac{a}{V_{clk}}\right) t_{rlp} \cdot \sin wt =$

$V_{outT} = a \sin w(t + \Delta T) = a \sin w\left(t + \frac{a}{V_{clk}} t_{rlp} \sin wt\right)$

$= a \sin wt + n w \Delta T \cos wt \sin wt$

$= \underbrace{\frac{a}{2} w \Delta T}_{DC} + \underbrace{a \sin wt}_{signal} + \underbrace{\frac{a}{2} w \Delta T \sin 2wt}_{H_2}$

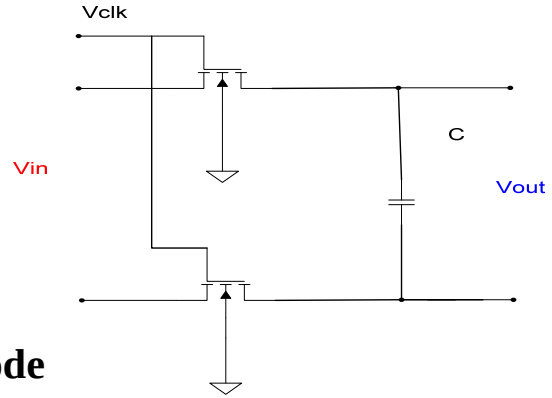
$$H_2 = \frac{w \Delta T}{2} = \frac{a}{2V_{clk}} 2\pi f_{in} t_{rise}$$

Can always be removed diff!

100ps, $V_{clk} = 1.2V$ $a = 0.2V$ $f_{in} = 100MHz$

$H_2 = -45dB$ ⟸

Diff. mode



$V_{outT}^{+} = a \sin w[t + \Delta T \sin wt]$

$V_{out}^{-} = -a \sin w[t - \Delta T \sin wt]$ $\Big\}$ $R_1 = R_2$

$V_{outT} = \left[V_{outT}^{+} - V_{outT}^{-}\right] = a \sin w[t + \Delta T \sin wt) + a \sin w(t - \Delta T \sin wt)$

$H_2 = \Phi$ IF $R_1 = R_2$

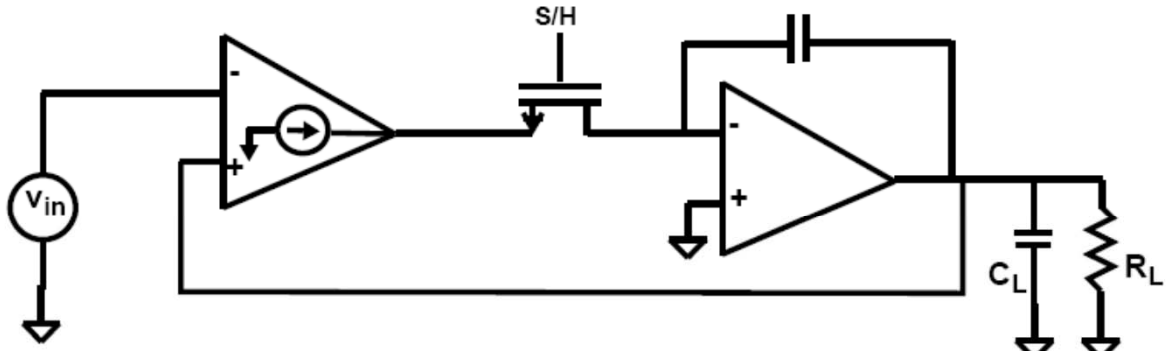
$H_3 \rightarrow$ how EXISTS $H_3 = \frac{1}{8} w^2 \Delta t^2$

Example.

$= \frac{\pi^2}{2}\left(\frac{a}{V_{clk}}\right)^2 (f_{sig} \cdot t_{rlp})^2 = -97 dB$

IF $R_1 = 0.9R_2 \sim 70!$

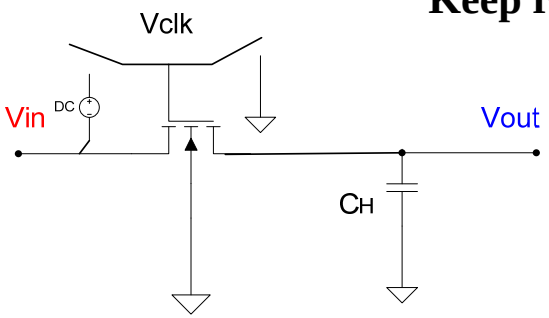
Example: Wooley JSC 12-89, Stafford JSC 12/74

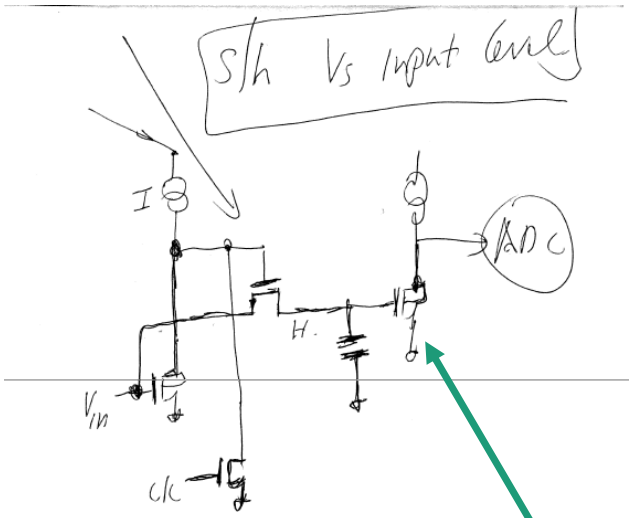


- Bottom-Plate Sampling- Different Implementation
- Output amp always active and valid
- Widely used in building blocks
- Disadvantage- Sample Mode Bandwidth limited by active devices
- Disadvantage- Offset, Noise limited by Amps

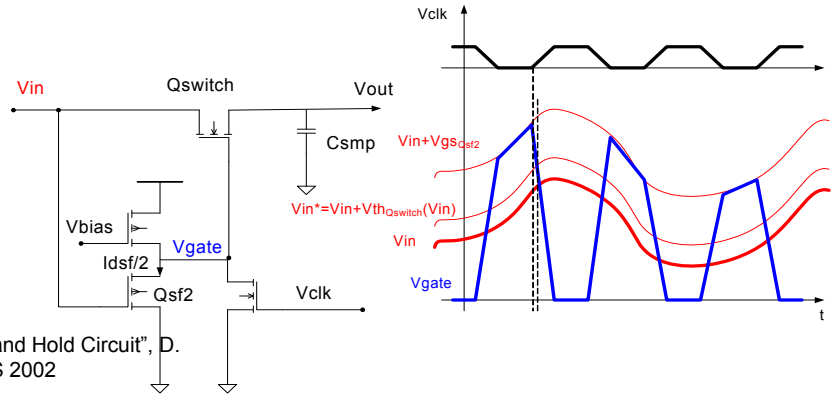
LINEARIZATION

Keep resistance constant





Option 1:



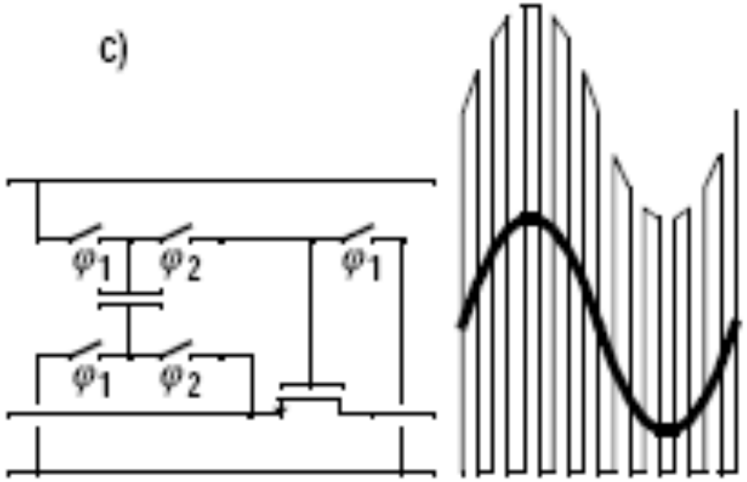
"A 1GHz Linearized CMOS Track-and Hold Circuit", D. Jakonis, C. Svensson, IEEE ISCAS 2002

Need to include buffer

Can limit distortion +65-75 dB

Boot strapping

Option 2:



Abo and grey)

And the linearity at high speed (1Ghz) is a problem
For both the S/H and the buffer – No time for feedback opamps – Levels shifter are preferable

Basic Boosted Switch Configurations

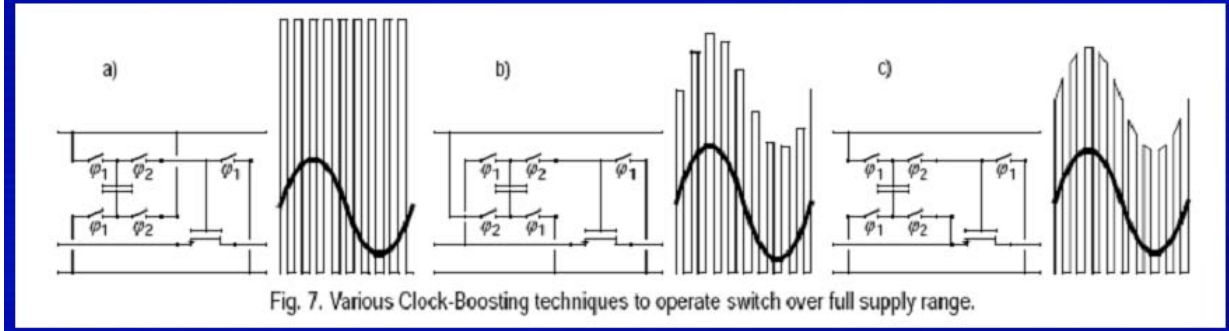


Fig. 7. Various Clock-Boosting techniques to operate switch over full supply range.

a) Boosting the clock to 2x Vdd
- Improved Ron (faster settling)
- Signal dependent settling
- Constant clock feed-through

b) Boosting the clock to Vdd + Vin
- Improved Ron (faster settling)
- Almost signal independent settling
- Signal dependent clock feed-through
- Input signal is loaded by boost cap during hold time

c) Boosting the clock to Vin + Vdd
- Improved Ron (faster settling)
- Signal independent settling
- Signal dependent clock feed-through
- Input signal is loaded by boost cap during track time

"Analog Design in Deep Sub-Micron CMOS" Klaas BultA, ESSCIRC, 2000

E N D
lecture 04