Welcome to

046188 Winter semester 2013

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 03 (part b)

(1st ½ and back to lect. 2 continue what we did not finished)

FLASH ADC

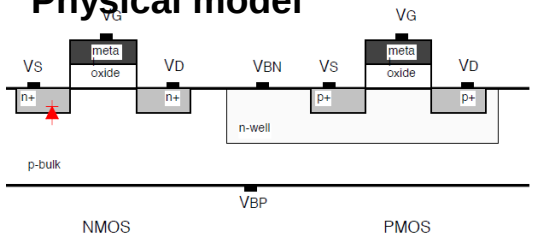
Agenda - you will get familiar with

www.gigalogchip.com

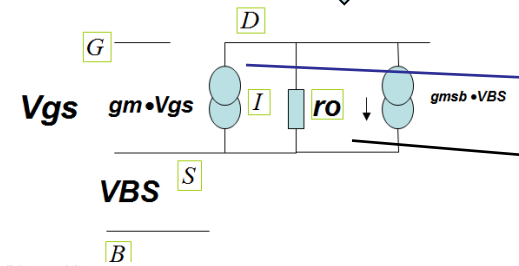
Flash ADCs – no error sources

Summary lect. 01,02

Physical model

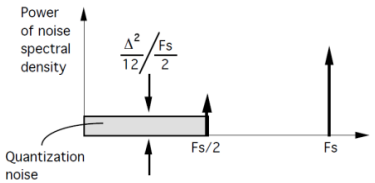


Small signal



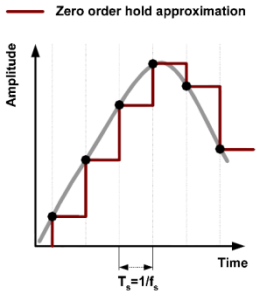
Linear region	$V_{GS} > V_{TH}$	$V_{DS} < V_{GS} - V_{TH}$
	$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right]$	
	$g_m = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{DS}$	
	$g_{ds} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH} - V_{DS})$	
Saturation region	$V_{GS} > V_{TH}$	$V_{DS} > V_{GS} - V_{TH}$
	$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$	
	$g_m = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} = \frac{2 \cdot I_D}{V_{GS} - V_{TH}}$	
	$g_{ds} = \frac{\lambda' \cdot I}{L}$	$r_{ds} = \frac{L}{\lambda' \cdot I}$

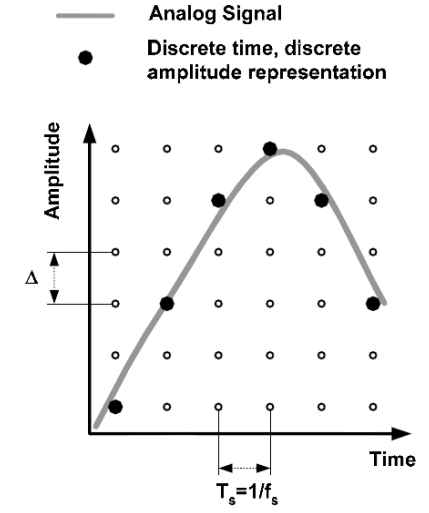
- It is assumed that the quantization noise exhibits a white spectrum



- The power-of-noise spectral density is:

$$n_q^2(f) = \frac{\frac{\Delta^2}{12}}{\frac{F_s}{2}}$$

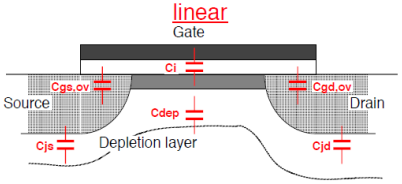




B. Murmann

Quantization error

Small Signal Equivalent Circuit –Capacitances



$$C_i = C_{ox}\,WL$$

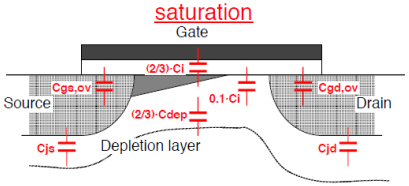
$$C_{dep} = \frac{\varepsilon_{si}}{x_{dep}}\,WL$$

$$C_{gs} = C_{gs,ov} + \frac{C_i}{2}$$

$$C_{gd} = C_{gd,ov} + \frac{C_i}{2}$$

$$C_{sb} = C_{js} + \frac{C_{dep}}{2}$$

$$C_{db} = C_{jd} + \frac{C_{dep}}{2}$$



$$C_{gs} = C_{gs,ov} + \frac{2}{3}\,C_i; \qquad C_{gd} \cong C_{gd,ov}$$

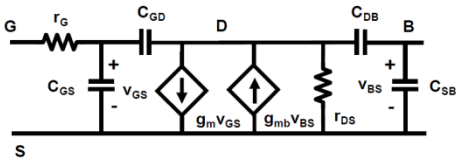
$$C_{sb} = C_{js} + \frac{2}{3}\,C_{dep}; \qquad C_{db} = C_{jd}$$

$$C_{gb} \cong \frac{1}{10}\,C_i$$

$$C_j \cong \frac{C_{j0}}{\sqrt{1 - \frac{V}{\Phi_T}}}$$

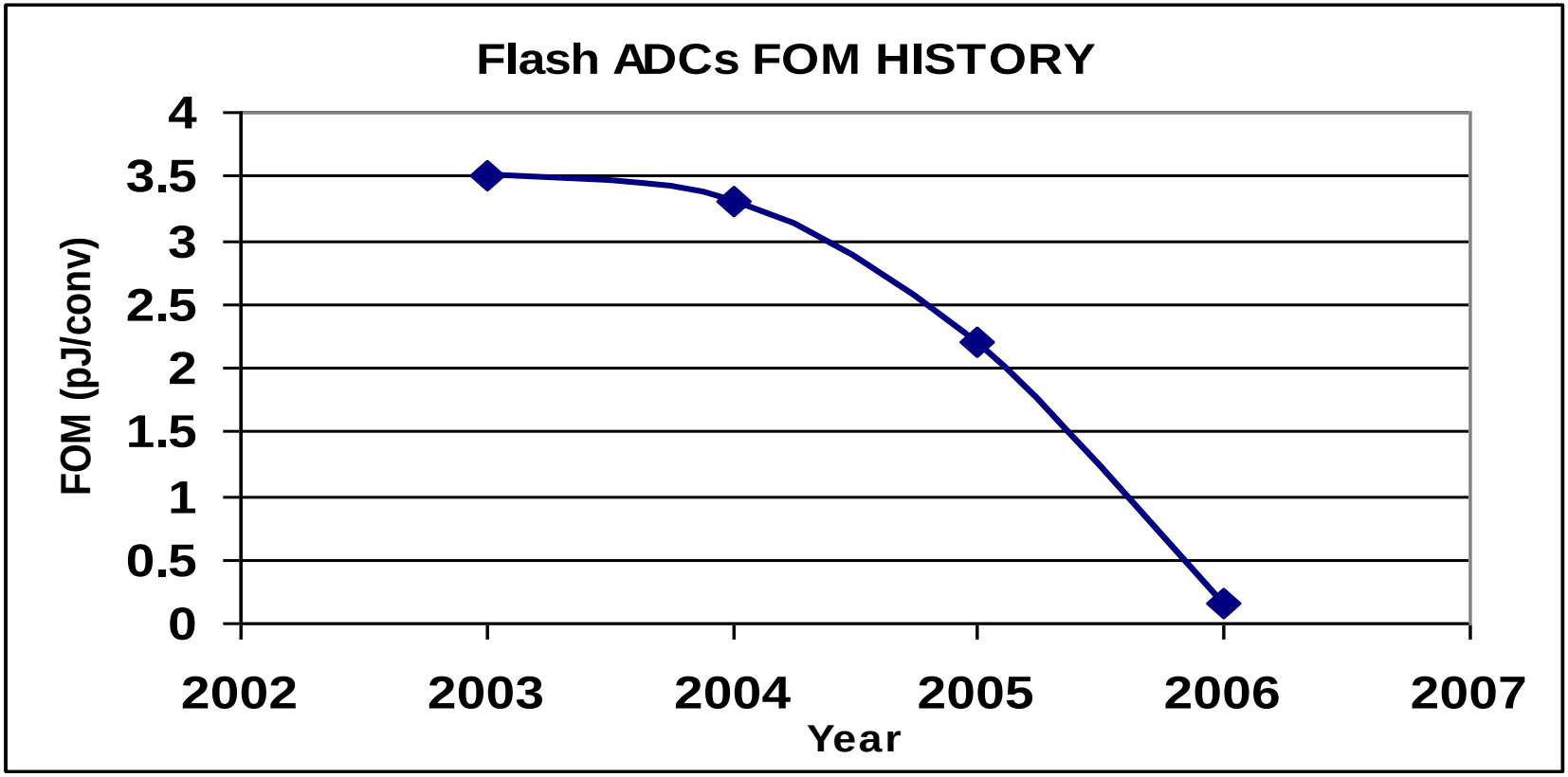
$$\Phi_T = \frac{kT}{q}\,ln\left(\frac{N_D\,N_A}{n_i^2}\right)$$

Small signal



wi : weak inversion

$$I_{DSwi} = I_{D0}\,\frac{W}{L}\,\exp^{\frac{V_{GS}}{nkT/q}}$$



2003 ➔ 6b & 2Gs/s (180nm CMOS)

2004 ➔ 6b & 300Ms/s (0.25um CMOS)

2005 ➔ 6b & 1.2Gs/s (130nm CMOS)

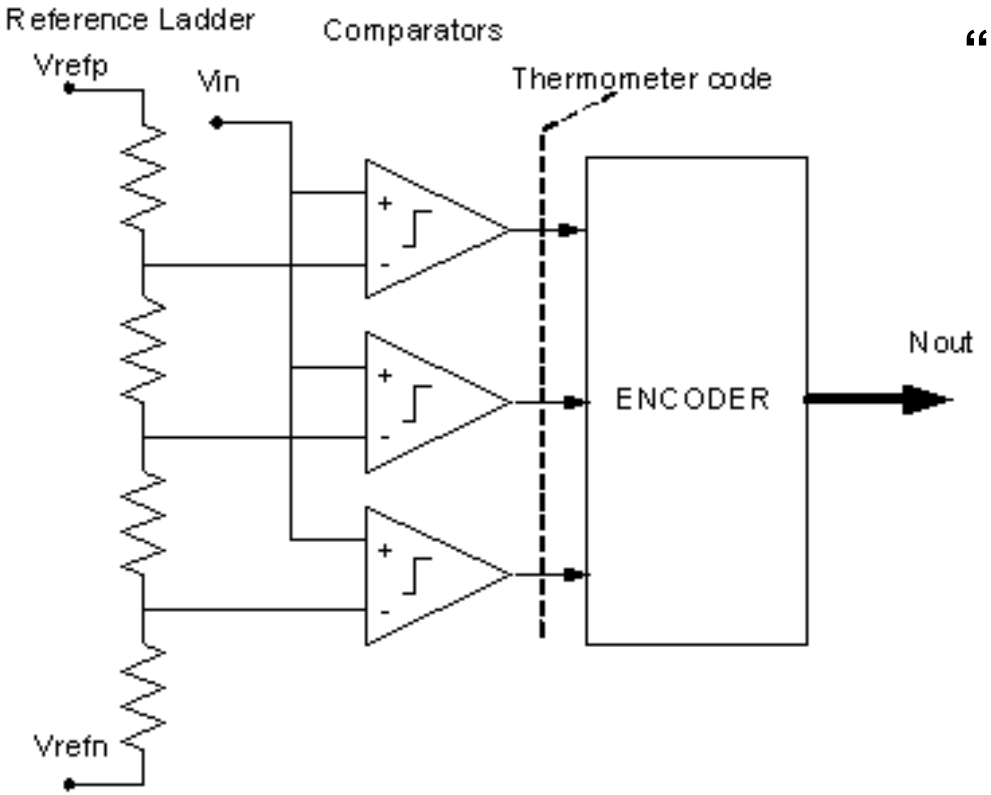
2006 ➔ 4b & 1.25Gs/s (90nm CMOS)

Flash ADC- beginning..This lecture.

Other ADC's – later…

SAR ADC
Pipelined ADC
Over sampling ADCs
Folding/Interpolating
Algorithmic ADC
Combined Parallel ADCs

Basic Flash ADC



“Classic mixed signal”

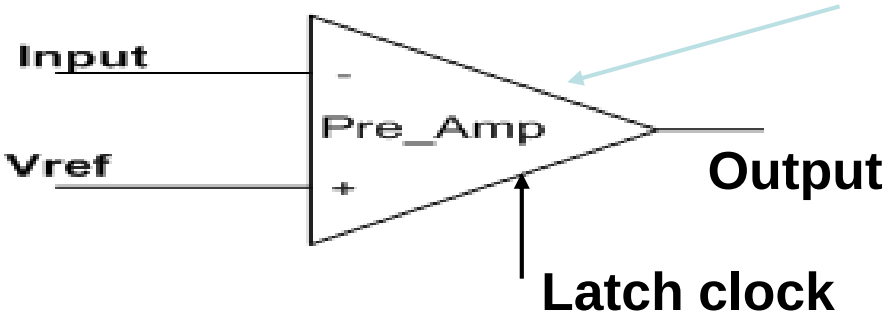
No Feed Back No Amplifiers all in “Open Loop”

Monotonic increasing: no missing codes due to R

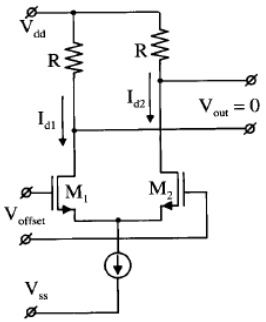
Comparator is the main element.

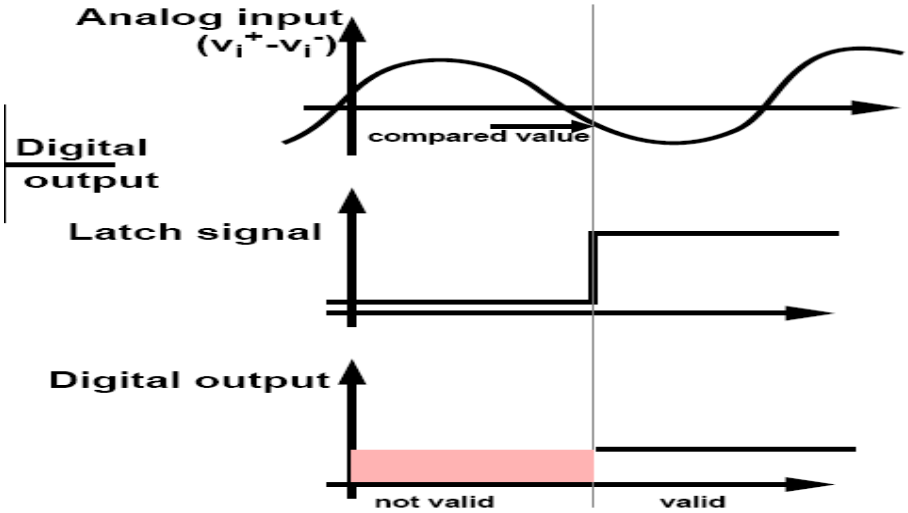
What's a Comparator

It's a chain of gain stages (unlike op amp) to achieve fast response



Symbol

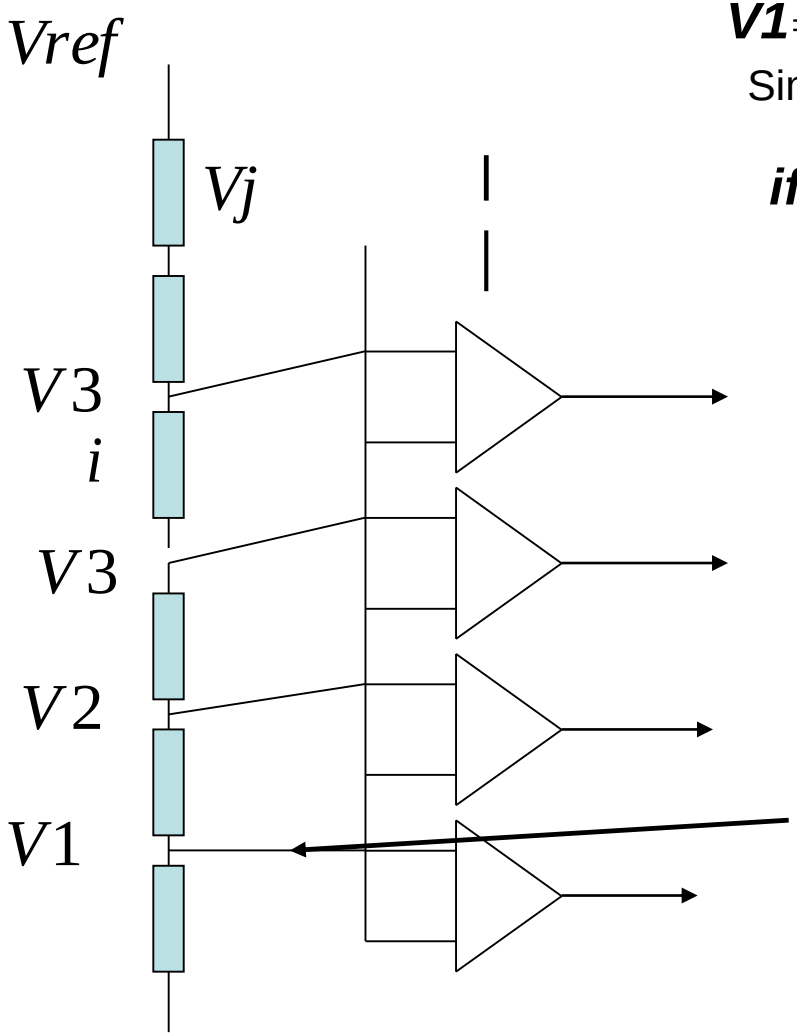




2 types :

Analog-Time Cont.
clocked-Latched
(Later lectures)

FLASH continue: Operation Equation



$$Vi = iR * Vref \ /(\sum_{i=1}^{j} Ri)$$

V1 = R1/(R1+R2+R3..Rj)*Vref

Simple voltage divider

if R1 = R1 = R2 = R3 = Rj = R)

$$Vi = iR * Vref \ /(\sum_{i=1}^{j} Ri)$$

$$V3 = 3R * Vref \ /(\sum_{i=1}^{j} Ri)$$

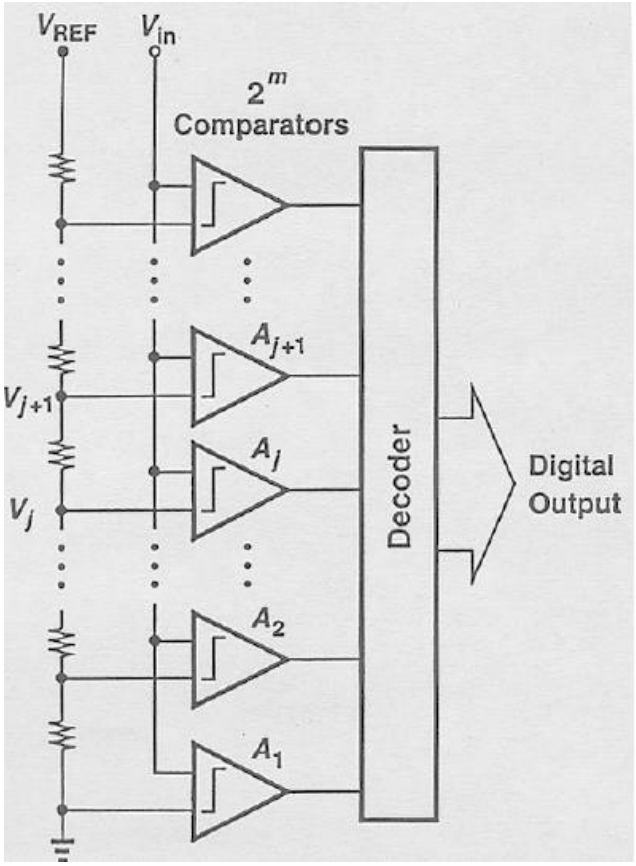
$$V2 = 2R * Vref \ /(\sum_{i=1}^{j} Ri)$$

$$V1 = R * Vref \ /(\sum_{i=1}^{j} Ri)$$

For n bit need 2 to the n -1 comparators

For n bit need 2 to the n resistors

FLASH continue: Number of Comparator Needed



Suited well up to 7-8 bits of resolution – 127 - 255 comparators

Flash speed: as the comparator, logic, and input impedance driving the comparators.

Output levels are like a "thermometer"

Example
Bot to top
11111100000
11111000000
11110000000
11100000000
11000000000
10000000000

INPUT LEVELS	BINARY CODE d c b a	GRAY CODE d c b a
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

Table 3.2: Binary-Gray code implementation

total number of comparators required is $2^N - 1$, where N is the resolution of the ADC

FLASH DESIGN EXAMPLE- later lecture

A good way to see the errors lets go over flash design

An 8 bits Flash ADC

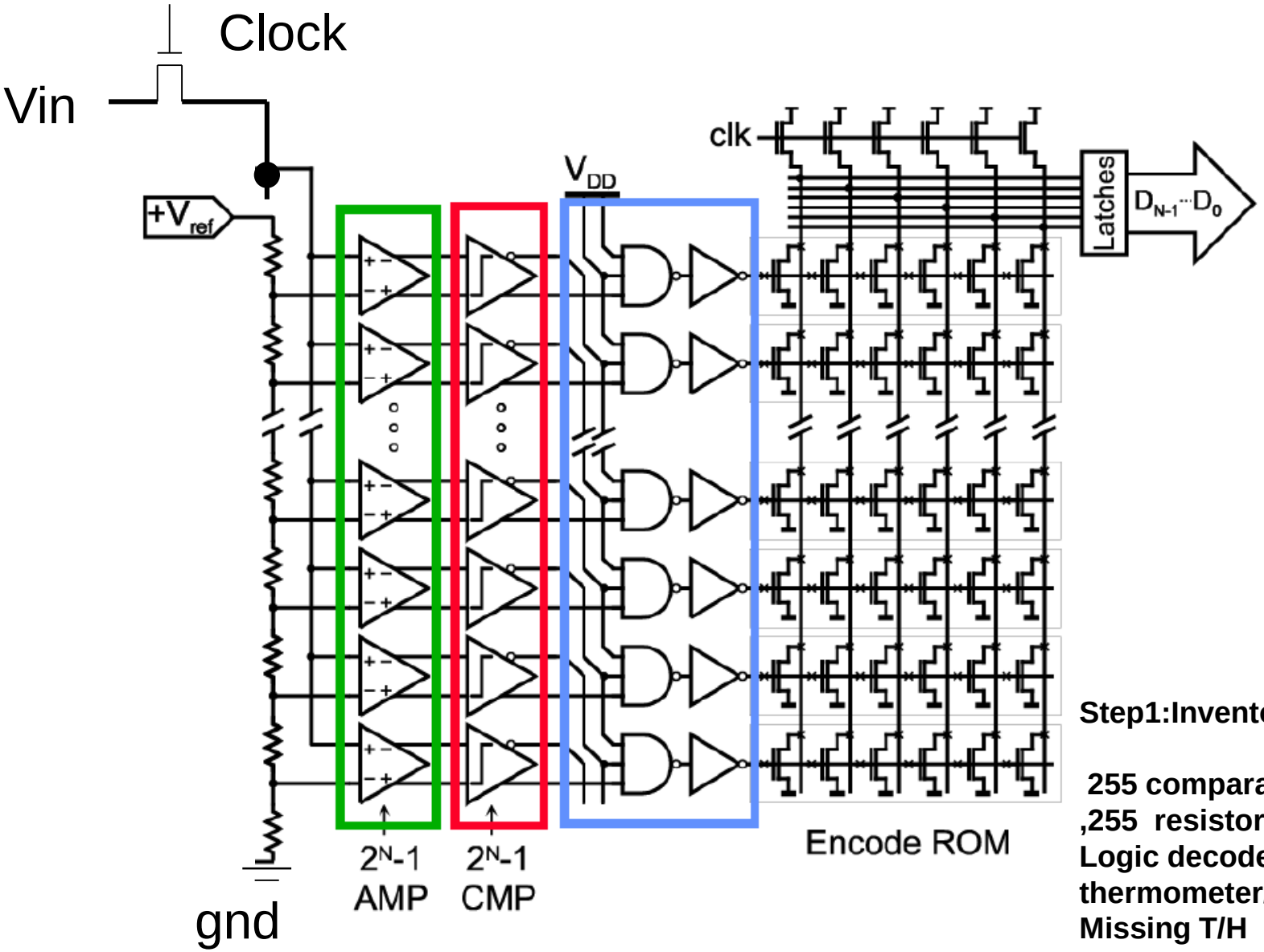
Assuming:

Process 0.18um, cox~6ff/uu, Kn= 60e-6 Kp=20e-6

$Kn = \mu Cox$

Step1: Choose an architecture – our task

Architecture – now to the details..



Source : K.. Leuven

Step1:Inventory:

255 comparators/amp
,255 resistors
Logic decoder
thermometer/binary
Missing T/H
References

Later: Detail look each element in the FLASH\

And how to deal/fix it..

Comparator Offset
Resistor mismatches
Power
Speed limit first stage
Signal Feed through
Gain
Dynamic Range – Max Vref
Comparator Meta stability (and speed)
Following stages – (bubbles)
Clock distribution

Detail look each error-element in the FLASH

Now we don’t have the tools to do this so we
Stop learn and get back to this in ~lect 5.

End lecture 3 (part b)