Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

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Lectures
http://www.gigalogchip.com/lectures.html

Lecture 3.

Comparator: operation and design

Mini Summary as of today..

some typ. numbers

CMOS tran.

$$I_{ds} = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{gs} - V_{th})^2(1 + \lambda V_{ds})$$ → **Keep Vdsat>120mV**

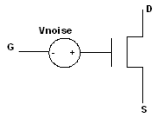
$$I_{ds} = g_m \cdot V_{gs}$$ → **gm = 1e-3**

$$\sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{ds}}$$

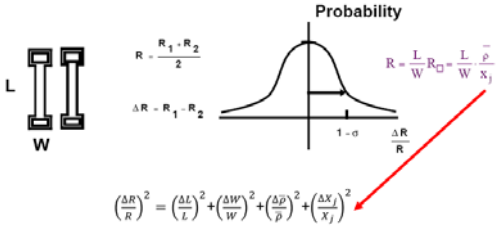
Change of I due to change of Vin

$$v_n^2 = \frac{8}{3}\frac{kT}{g_{m_n}}$$

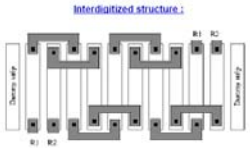
CMOS Noise



Not easy to be below 5nV/sqrtHz.
Add 1/f , convert to I noise.. By multip.*gm



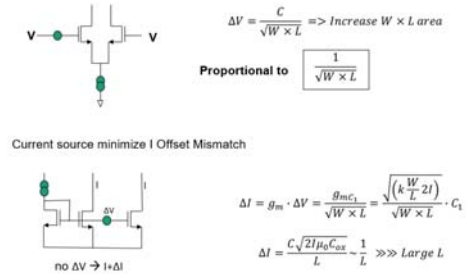
matching



1un x 1um resistor can mismatch 1%

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}}$$

2-5 mv/1um square



Transisors like large area
As current large L

Agenda

Quick review on analog circuits basics

- Comparator basics
- Architectures
- Parameters and Error sources
- Comparator Examples

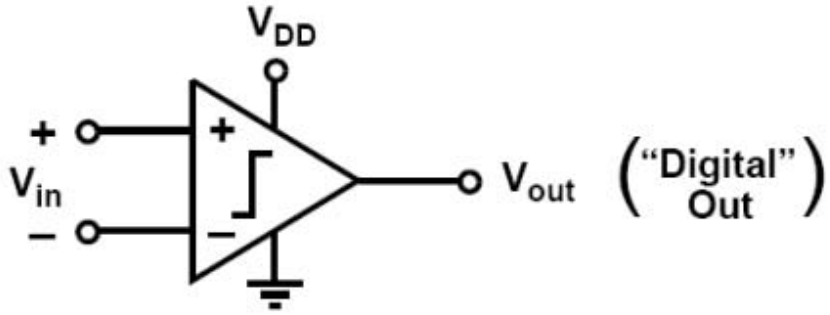
Comparator basics

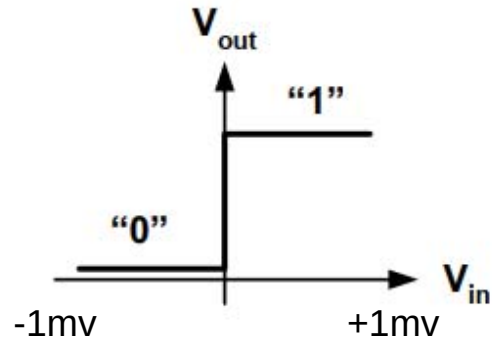
- Comparator:
  - A Link from Analog to Digital – Quantizer
- Definition:
  - Compares between 2 or more inputs and produce a digital value high or low- *“Its a 1 bit ADC !”*
- Structure:
  - A chain of gain stages (no feed back-unlike amplifier)
- It is used in an “open Loop” configuration to achieve fast digital response (opamps are slow and big)

Comparator basics

- types
  - Non Sampled
  - Sampled

Comparator basics: Operation





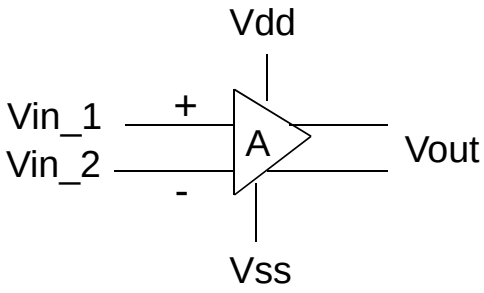
- Function
  - Compare the instantaneous values of two analog voltages (e.g. an input signal and a reference voltage) and generate a digital 1 or 0 indicating the polarity of that difference

Mathematical descriptions for low frequency

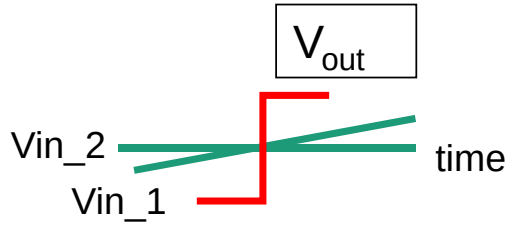
For small V_{in1}-V_{in2}

$$V_{out} = A(V_{in\_1} - V_{in\_2})$$

A = Gain of the combine structure



For all large V_{in1}-V_{in2} V_{out}=clamp at either supply



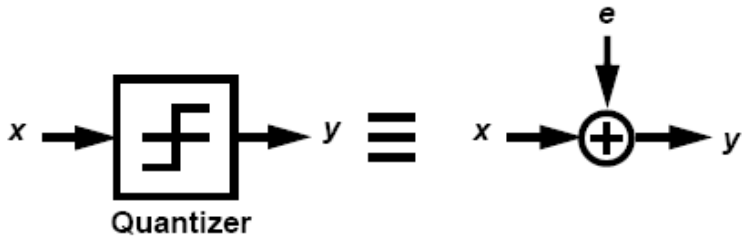
Ideal

$V_{out} = A(V_{in\_1} - V_{in\_2})$ → results fall between supplies (realistically its exponential)

$$V_{out} = V_{dd} \quad if\ A(V_{in\_1} - V_{in\_2}) > V_{dd} - V_{ss}$$

$$V_{out} = V_{ss} \quad if\ A(V_{in\_1} - V_{in\_2}) < V_{dd} - V_{ss}$$

What is gain=A how we make it noise ?



Important model in
Sigma Delta ADCs

exact model if *e* is defined properly
ex. *y=sgn(x)*, then *e=y-x=sgn(x)-x*

becomes an approximation when we claim noise is independent

Most comparator:
The key of successful comparator is how to create needed/maximum gain at minimum time…
competing parameters…

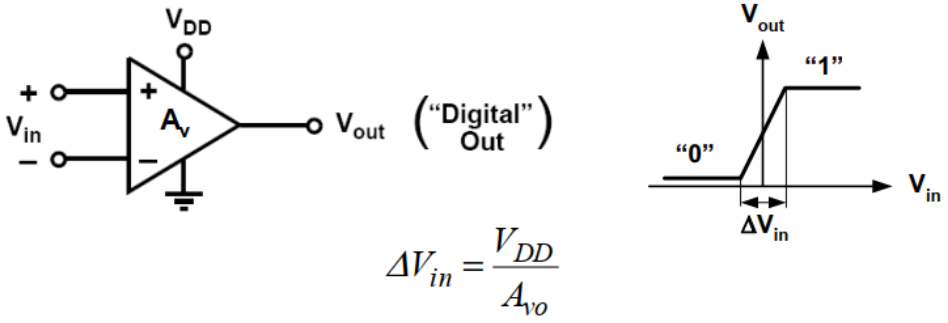
Errors/parameters in comparators:

- Gain
- Offset
- Meta State
- Speed
- Kick Back
- Noises and supply noise

Gain

Voltage gain: is the DC differential gain of the comparator. The output peak-to-peak swing is in the range of 3-5 V. Therefore, for low speed, in order to detect a 1 mV signal a voltage gain of 5000 is sufficient.

Gain Requirements



$$\Delta V_{in} = \frac{V_{DD}}{A_{vo}}$$

No matter how fast, the needed gain is required. but it is sonly 1 parameter..

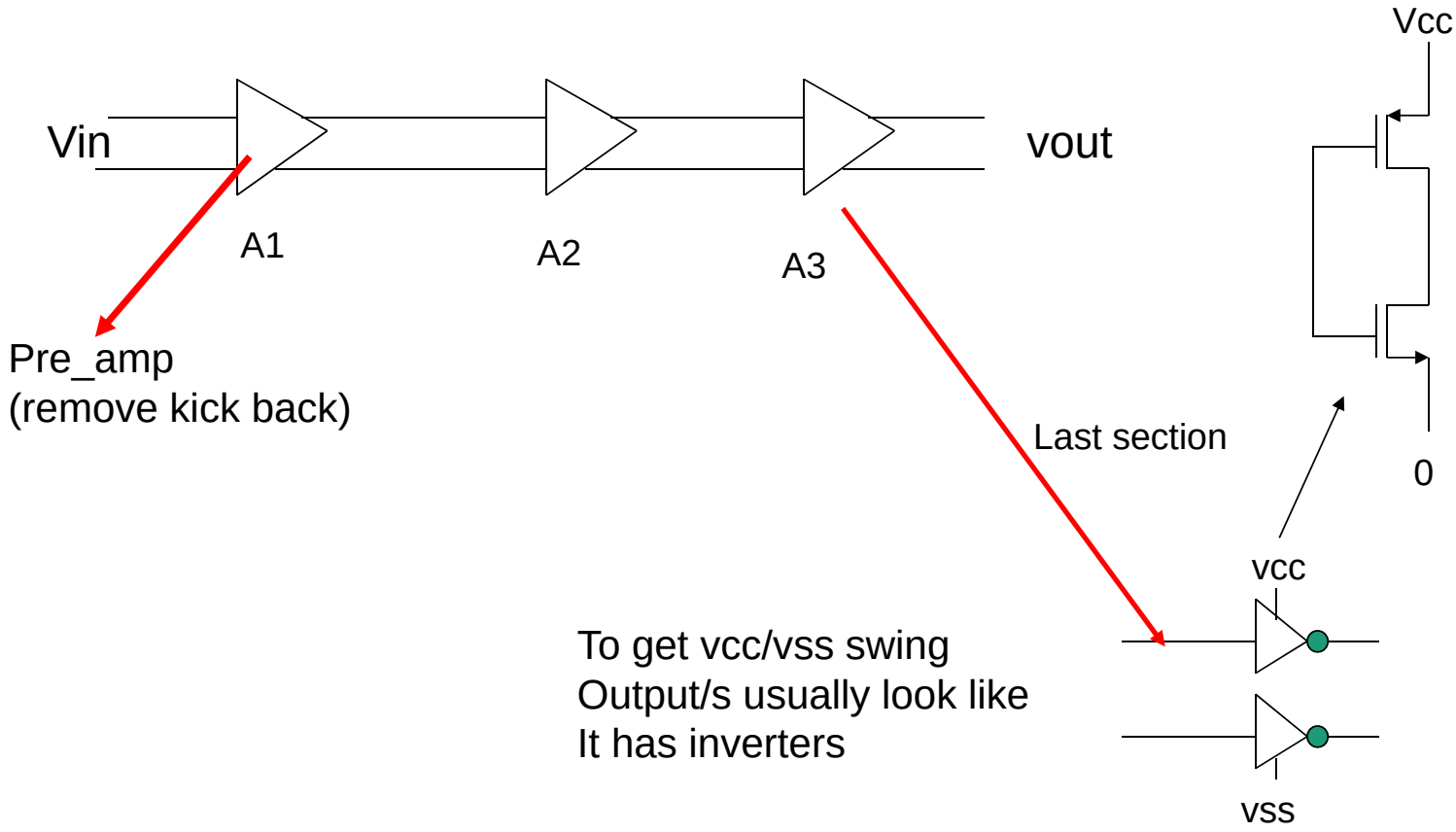
- E.g. 12-bit ADC, V_{DD}=1.8V, FSR=0.9V, ⇒LSB=0.9V/4096
- For 1/2 LSB precision, we need

$$A_v = \frac{1.8V}{0.5 \cdot 0.9V / 4096} \cong 16{,}000 = 84dB$$

To achieve this gain we use more than one stage…
or some other architectures.. and our symbol stay a triangle

comparator architecture – choice 1

- Non Sampled: Continuous Time (CT)
- Output is gain time input differences:
  - slow because internal nodes need to recovered – cross each other first

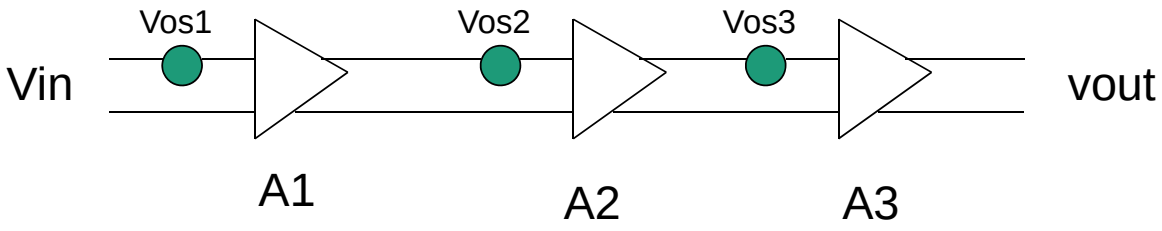


Input offset

Input offset: is the voltage that must be applied to the input to get the transition between the low and the high state (same as the op-amp).

Offset and gain of comparator

V_{os}(total)



$$V_{os\,(total)} = \sqrt{V_{os1}^2 + \frac{V_{os2}^2}{A_1^2} + \frac{V_{os3}^2}{A_1^2 A_2^2}}$$

Key:
- ❑ V_{os} is a statistic parameter
- ❑ Further stages (A2 and A3) have larger offset using minimum sizes..

Example: 8 bit ADC

for 8 bit with V_{fs}=0.5v , V_{dd}=1v at 1/10LSB =
A1 x A2 x A3 required ~ 5000 ➔ (1v/(0.5/255 x 10=0.2mv)
If:
Vos1=2mv, vos2=10mv, vos3=20mv
If we take: A1=10 A2=25 A3=20

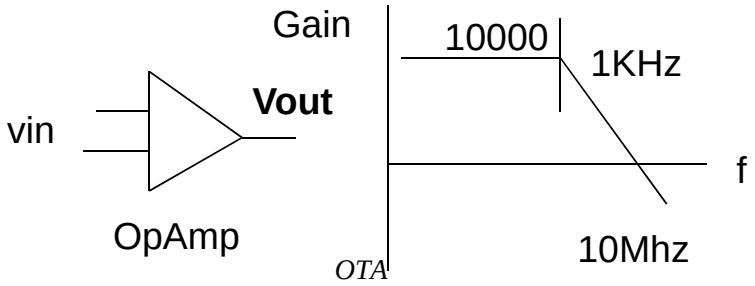
remember lect. 2 ? Mismatches ?

$$V_{os\,(total)} = \sqrt{2^2 + \frac{10^2}{10^2} + \frac{20^2}{10^2 25^2}} = 2.23mV$$

We are in trouble .. We need to detect 0.2mv but no detection due to offset

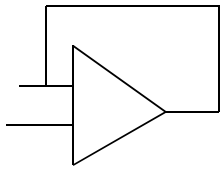
Quick detour to see the difference of a comparator to an op amp

Speed and feedback basics



Speed	Gain(dc)
$\tau = 1ms$	80dB

Vout rise to 63% final value in 1ms



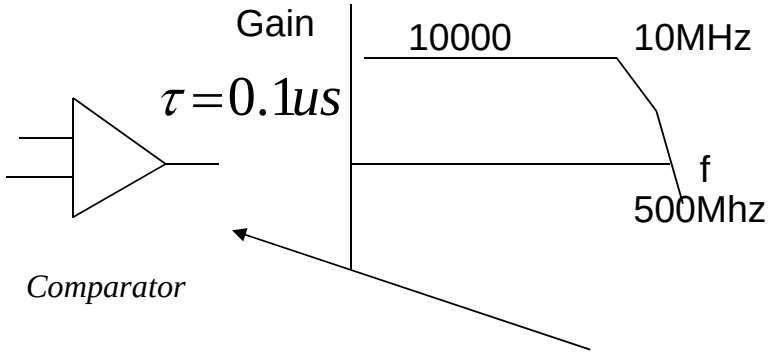
Gain=1

And accurate

$\tau = 0.1us$	0dB

Vout rise to 63% of vin in 1us

Feed _ back

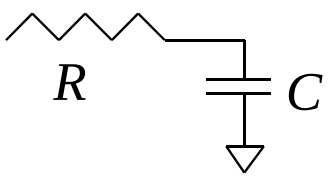


$\tau \sim 0.1us$	80dB

comparator from an amplifier if you removed all compensation no feed back needed..

Contradiction..feed back can improve speed. (lost A+1) gain

"SLOW"

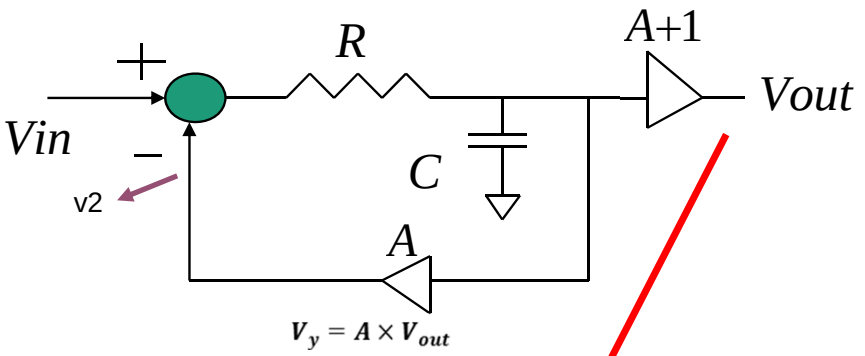


$$V_{out}(t) = V_{in}\left[1 - e^{-t/\tau}\right]$$

$$\tau = RC$$

$$Gain_{DC} = 1$$

"FAST"



$$V_{out}(t) = V_{in}\left[1 - e^{-t(A+1)/\tau}\right]$$

$$\tau(new) = RC/(A+1)$$

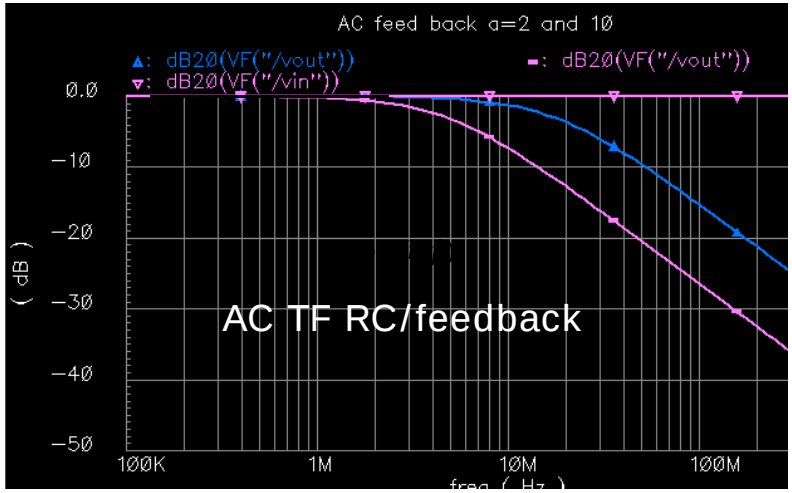
$$Gain_{DC} = 1/(1+A)$$

But at V_2:

$$Gain_{DC} = \frac{A}{1+A} \approx 1$$

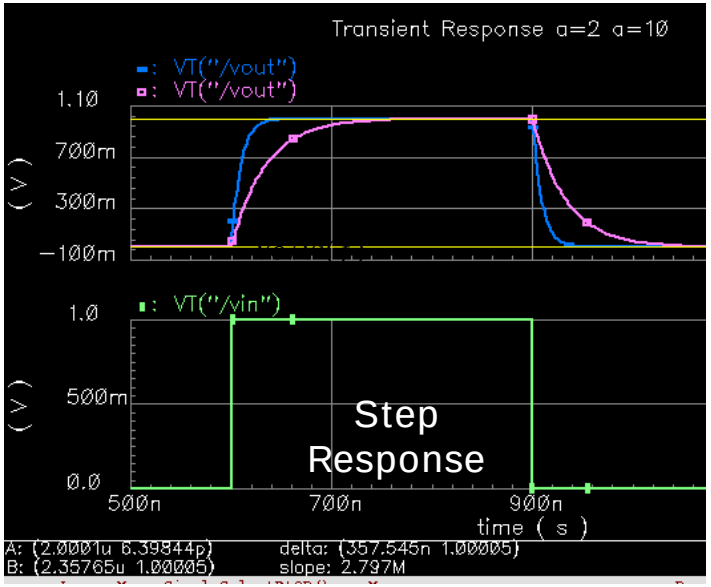
Basic Feedback to Boost BW

Simulation: A=2 and A=10



Frequency

$$Vo/Vi(f)$$



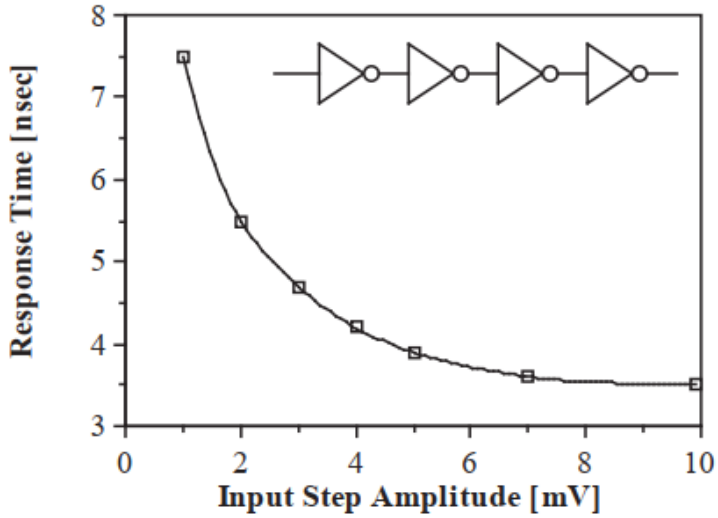
Time

AC Response

Time Domain

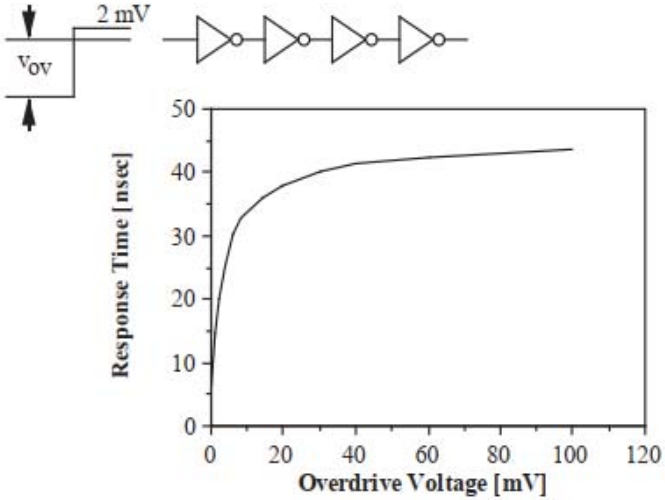
Main 3 parameters..

Response time: is the time interval between the application of a step input and the time when the output reaches the respective logic level. The response time depends on the amplitude of the step input.



F. Maloberti: *Design of CMOS Analog Integrated Circuits* - "CMOS Comparators" 6/3

Overdrive recovery time: if the input is driven with a voltage larger than the one required to cause the output saturation, the comparator is over driven. The response time for a given input amplitude, depends on the value of the overdrive voltage at which the comparator was driven.



F. Maloberti: *Design of CMOS Analog Integrated Circuits* - "CMOS Comparators" 6/4

I consider this the biggest challenge

Three

Sensitivity- It is the minimum voltage or current that produces a consistent output signal within the expected comparison time- Meta state

the list of errors parameters goes for ever..

- Kick back input noise – Caused in evaluation state due to transition response: Switching noise

Latching compatibility. A latch command and an unlatch command stores and releases the output logic state. Typically the load set-up time is around 2 nsec.

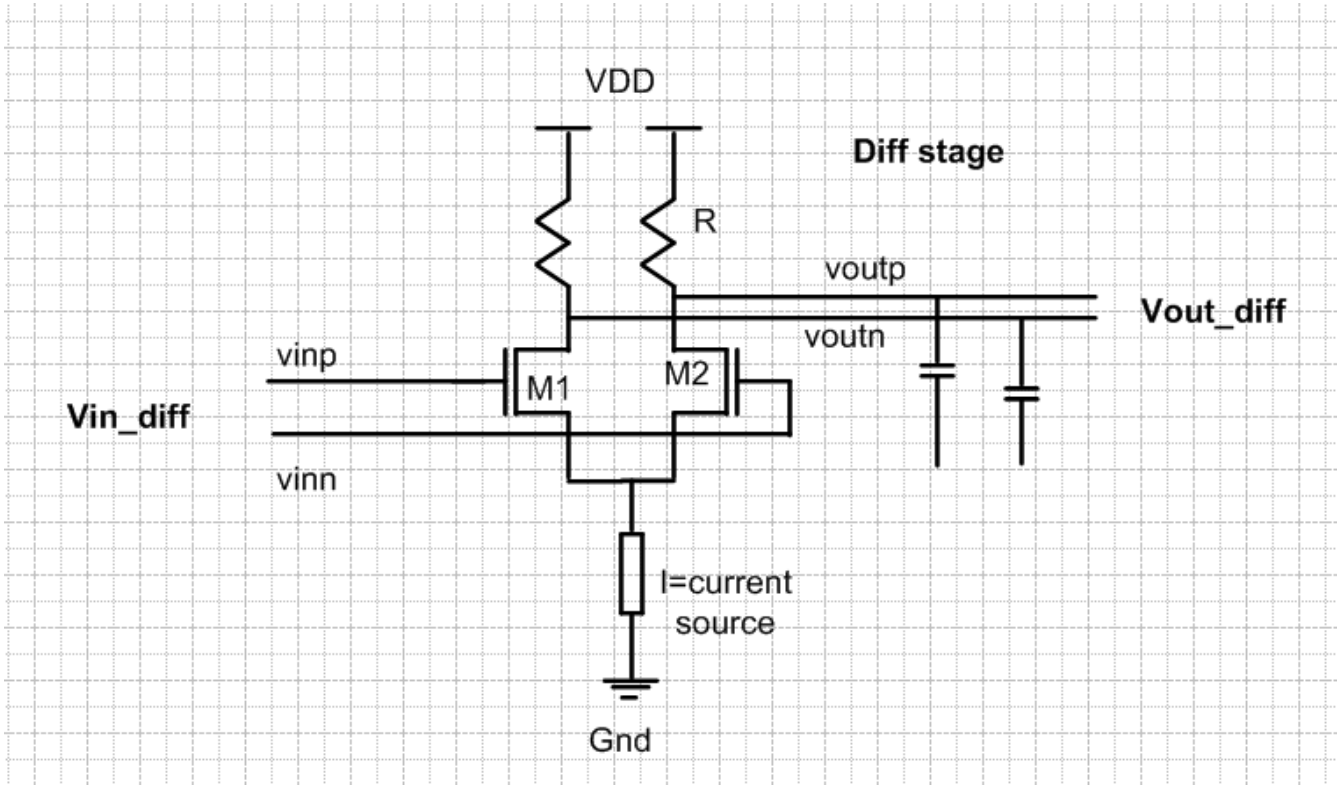
Power supply rejection. Transfer function between the supply rails and the output of the comparator.

Power consumption. Power dissipated at DC (static) and during the comparison (dynamic).

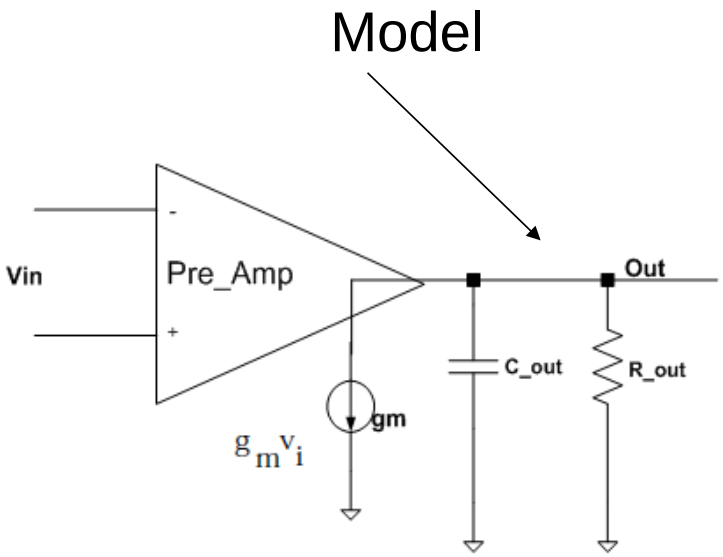
Hysteresis. The threshold voltage for rising input signals is different from the threshold voltage for falling input signals.

Lets look at the guts of the comparator

Gm Rout … diff stage..



Basic Analysis – non sampled clocked –non latched



$$t \ll \tau = R_L C_L$$

$$V_{out} = g_m R_L V_i (1 - e^{-t/(R_L C_L)}) \cong V_i \frac{g_m}{C_L} t$$

Key derivative = t x Vi x A

What about second stage ?
It sees t x Vin= txt..

$$V_{out}(t) = V_{in} \cdot g_m \cdot R_{\_out} \cdot (1 - e^{-t_{reg}/\tau})$$

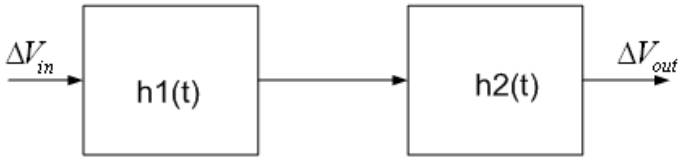
$$Where: \tau = R_{out} \cdot C_{out}$$

$$g_m = \frac{I}{V_{in}}$$

Cascade stages

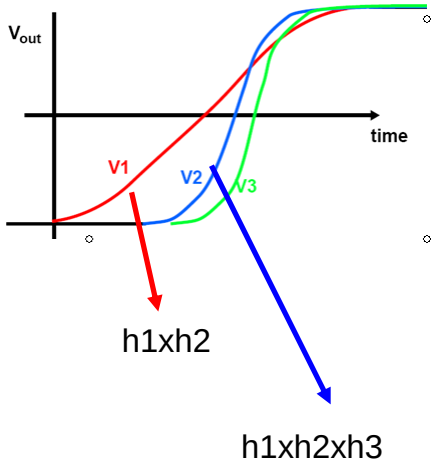
$$v_{oN} = \frac{\omega_u^N}{s^N} v_{in}$$

Band width reduction



$$h(t) = h_1(t) * h_2(t) = \left(e^{\frac{g_m}{C_L}\cdot t} * e^{\frac{g_m}{C_L}\cdot t} \right) = t \cdot e^{\frac{g_m}{C_L}\cdot t}$$

$$\Delta V_{out}(t) \approx \Delta V_{in} \cdot K \cdot t \cdot e^{\frac{g_m}{C_L}\cdot t}$$

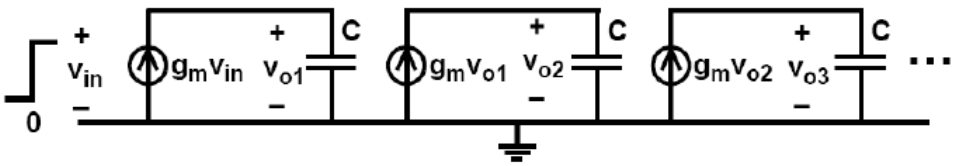


Note: if we have n-stages of the regenerative feedbacks then

$$h_n(t) = h_1(t) * h_2(t) \cdots * h_{n-1} * h_n = \left(e^{\frac{g_m}{C_L}\cdot t} * e^{\frac{g_m}{C_L}\cdot t} \ldots * e^{\frac{g_m}{C_L}\cdot t} * e^{\frac{g_m}{C_L}\cdot t} \right) = \frac{t^{n-1} \cdot e^{\frac{g_m}{C_L}\cdot t}}{(\quad)!}$$

In all n same

$$V_{out} = V_{in}\left(\frac{g_m}{C_L}\right)^n \cdot \frac{t^n}{n!}$$



Example

Given: gm=1e-3 , C=25fF vin=1mv step.

Find t for vout=100mV (why ? - so second stage can work well..)

$$V_i \frac{g_m}{C_L} t$$

Answer: n=1
t=100*25e-15/1e-3= **2.5n**s long time…

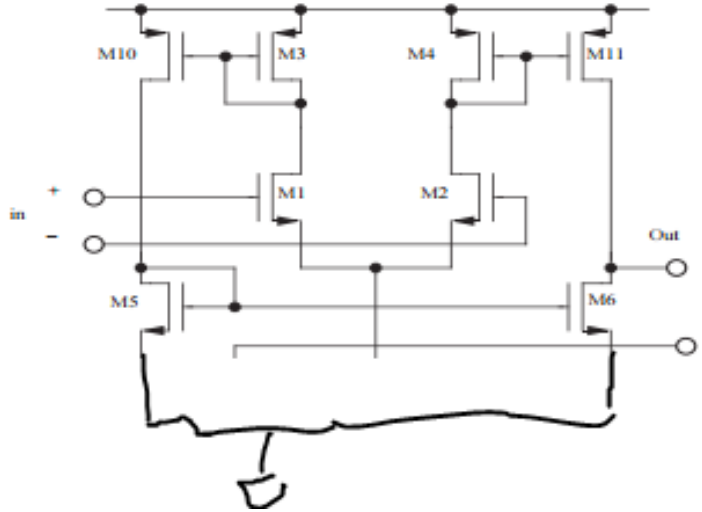
$$V_{out} = V_{in}\left(\frac{g_m}{C_L}\right)^n \cdot \frac{t^n}{n!}$$

Answer n=2
If we take 2 gain sages each gain stage=10
First stage reach 10 in 0.25ns
.
T=SQR(100*2*625)*(e-24) ~350e-12=**0.35ns**

But this is not always real life signals don't start from their equilibrium..

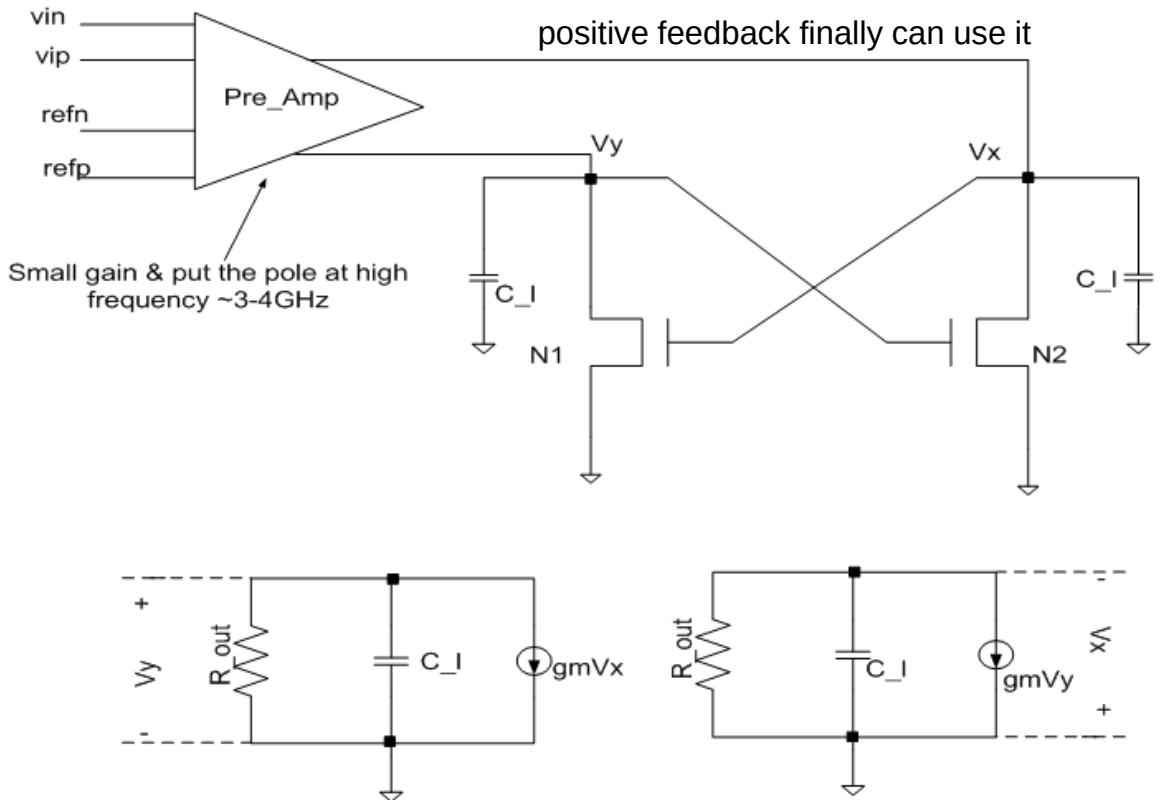
Speed increases by increasing gm/C

Popular stage



Comparators with positive feedback – sampled

With positive feedback – Sampled



Its nice but its stuck for ever ? or..

Math – positive feedback comparator latch

$$g_m \cdot V_y = -C_L \cdot \frac{dV_x}{dt} - \frac{V_x}{R_{out}} \qquad g_m \cdot V_x = -C_L \cdot \frac{dV_y}{dt} - \frac{V_y}{R_{out}}$$

$$\begin{cases} \tau \cdot \frac{dV_x}{dt} + V_x = -A \cdot V_y \\ \tau \cdot \frac{dV_y}{dt} + V_y = -A \cdot V_x \end{cases} \rightarrow \text{where} \quad \tau = R_{out} \cdot C_L, \quad A = g_m \cdot R_{out}$$

Look not R but gm–
Great speed improvement

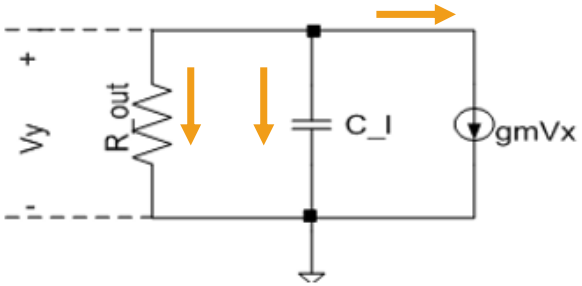
$$\tau \cdot \frac{d(\Delta V)}{dt} = \Delta V(A-1)$$

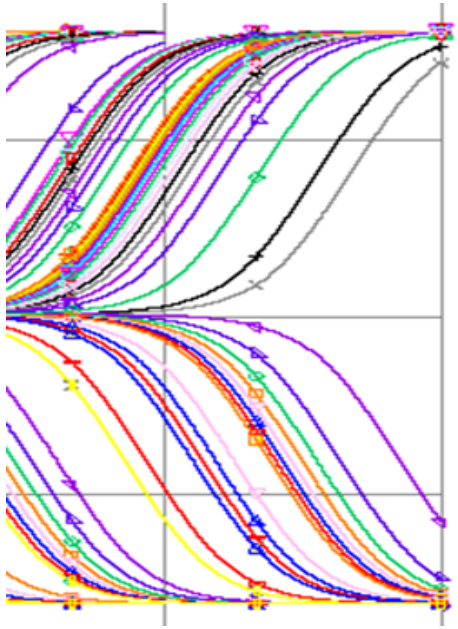
$$\frac{\tau}{A-1} \cdot \frac{d(\Delta V)}{dt} = \Delta V$$

Solution →

$$\Delta V = \Delta V_0 \cdot e^{\frac{A-1}{\tau} t} \approx \Delta V_0 \cdot e^{\frac{g_m}{C_L} t}$$

$$\frac{A-1}{\tau} = \frac{g_m \cdot R_{out} - 1}{R_{out} \cdot C_L} \approx \frac{g_m}{C_L}$$



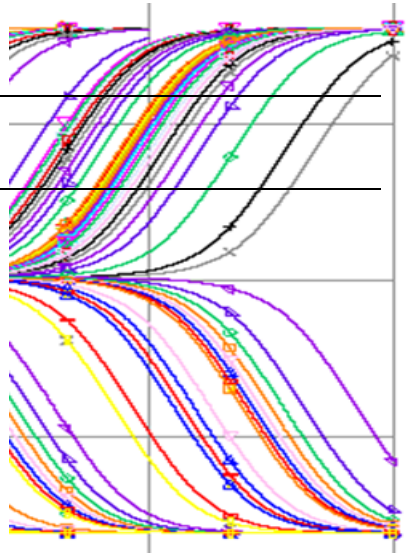


Meta-stability in comparator

- Meta-stability is a potentially catastrophic event that can occur when asynchronous inputs and regenerative/flip-flops are used
- Meta-stable outputs are not logic high or logic low and cause delays and system failures
- Meta-Stability is a probabilistic event, because the difference between the input signal and the reference voltage is a random variable
- The smaller the difference between the input signal and reference voltage, the longer the decision time required. On the limit the decision time can approach infinity

Hysteresis won't help..

Not a defined place



Analytical Derivation of Meta-Stability & Mean Time To Failure (MTF)

- The probability event given following: where t is the actual comparison time, T is the allowed time

$$\Pr(t > T) = e^{\left(-\frac{A}{\tau}\cdot T\right)} = e^{-\frac{g_m}{C_{out}}\cdot T}$$

- If one can have a collection of N such comparators all clocking at a frequency fs, then one can found MTF following

$$MTF \approx \frac{e^{\frac{A}{\tau}\cdot T}}{N\cdot f_s} = \frac{e^{\frac{g_m}{C_{out}}\cdot T}}{N\cdot f_s}$$

~ Set it for > month

Example

- Example: 6-bit, 500MHz Flash ADC, $T_{max}=T_s/2=1ns$, $\tau_u=1/(2\pi\cdot 5GHz)=32ps$, $A_v=3$, $V_{FS}=0.5V_{DD}$

$$P(Error)=\frac{2}{3}\left(2^6-1\right)\cdot e^{-1000/32}\cong 10^{-12}$$

- Mean time to failure (MTF)

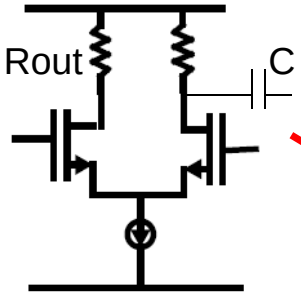
$$MTF=\frac{1}{P(Error)\cdot f_s}=\frac{1}{10^{-12}\cdot 0.5\cdot 10^9}s=2000s\cong 33\text{minutes}$$

source: Prof. Murmann stanford

Comparator circuits

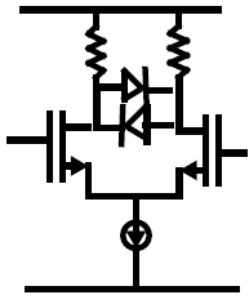
Front Stage Architectures- with Resistors

1. Use small values of R_l
- **Minimizes swing**
- **Shortens time constant**



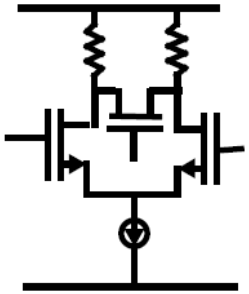
$$V_{out}(t) = V_{in} \cdot g_m \cdot R_{\_out} \cdot (1 - e^{-t_{reg}/\tau})$$
$$Where: \tau = R_{out} \cdot C_{out}$$

2. Use Passive Clamps
- **Limits Swing**
- **Adds parasitics**



BW = 1 / 2pi(RoutC)

3. Use active nulling clamps
- **Good in principle**
- **Tough clock generation problem**

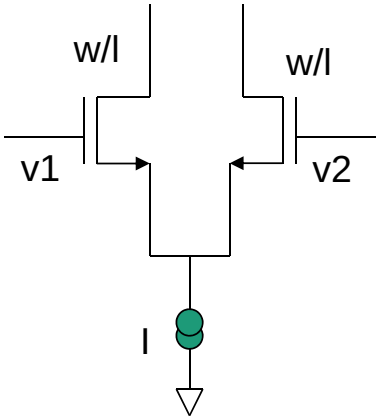


Source: P Gray

Summary:
Number of stages and gain needed
is process and project dependent no fixed analytical solution.

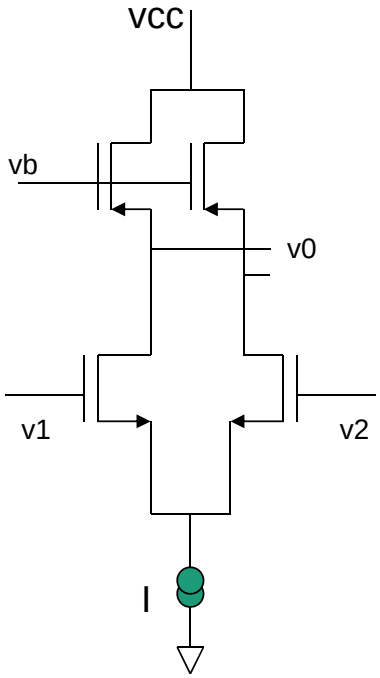
Best empirical gmR=4-8 number of stages ~ 2-4

Input Stage: Architectures Options - Using PMOS



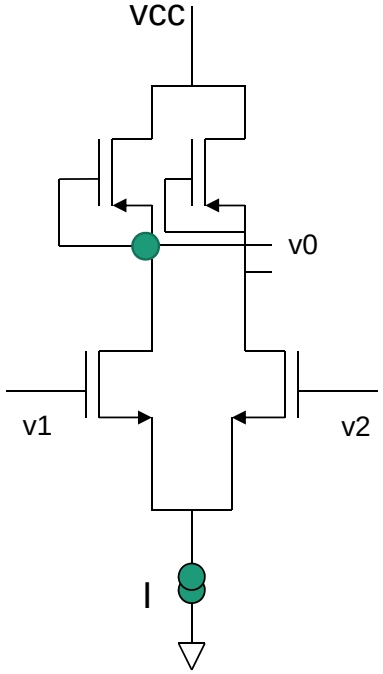
gm x what

A



gm x Rop/Ron
Kickback
Large gain

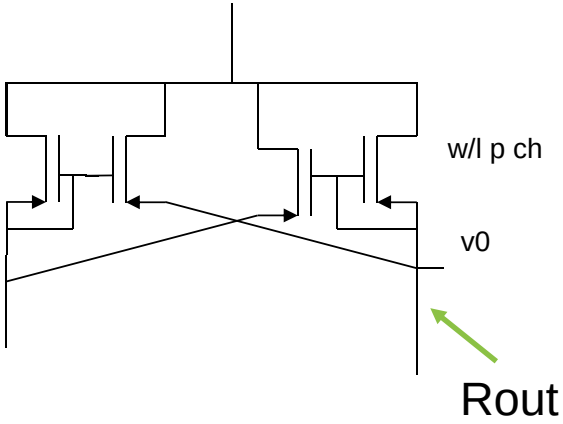
B

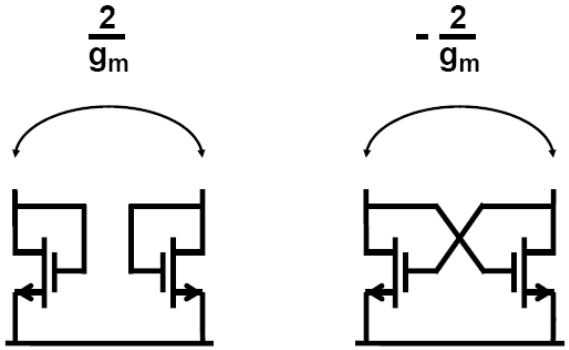


gm x 1/gmp
Low gain

C

Added Feedback to load

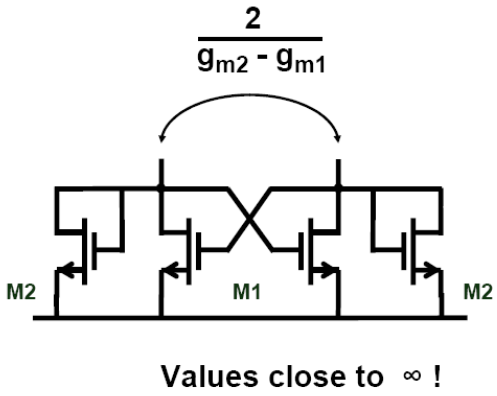




positive feedback to raise Rout

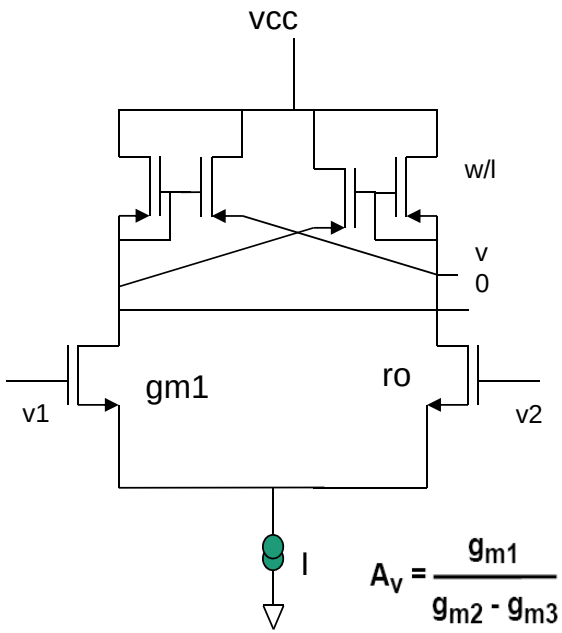
Effective rout =infinite

In class proof.

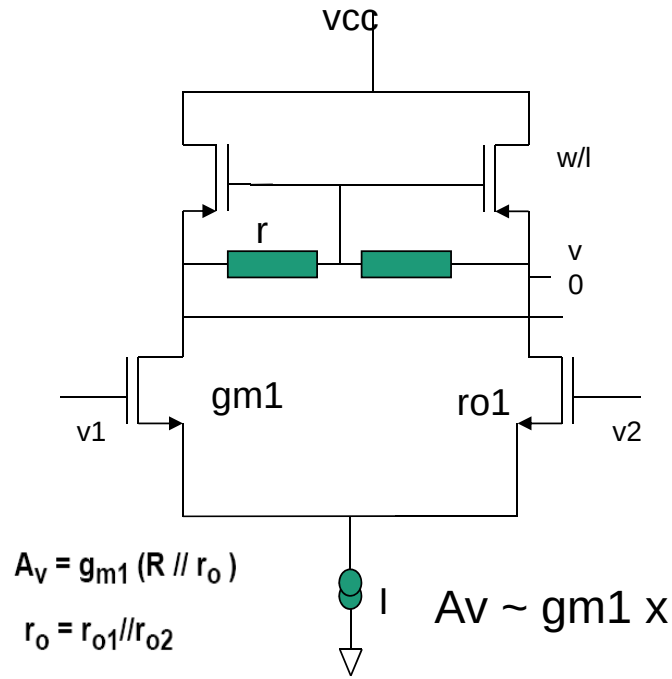


Source: Willy Snasen 2005

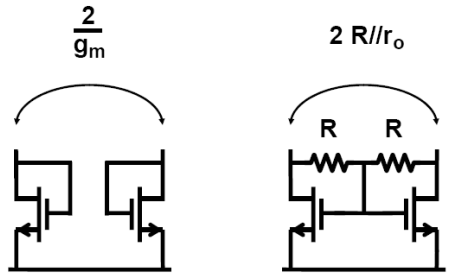
Input stage: architectures options



AV ~ gm1 x ro



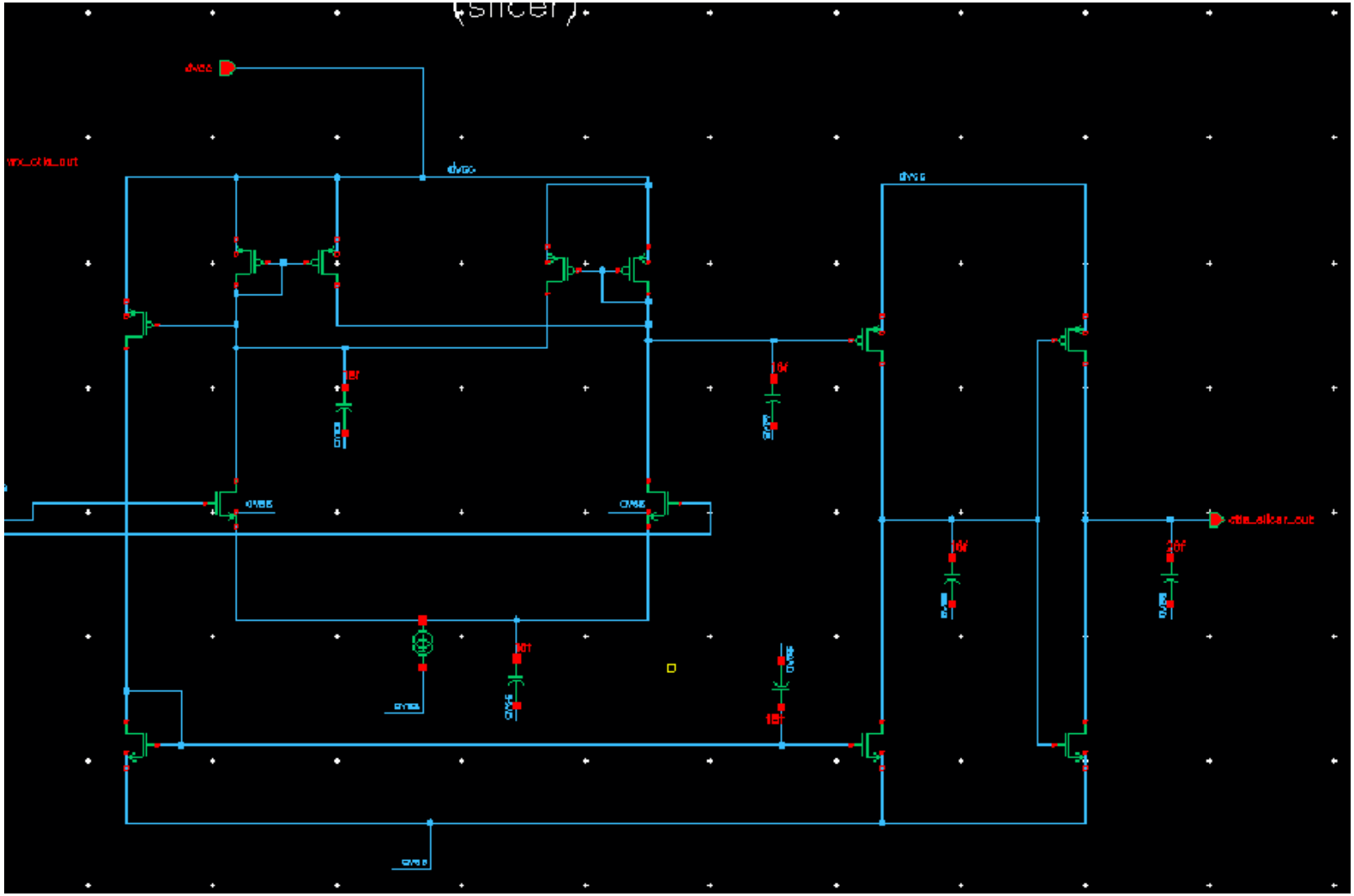
Av ~ gm1 x r



Source: Willy Snasen 2005

Comparator examples

Utilizing the feed back..



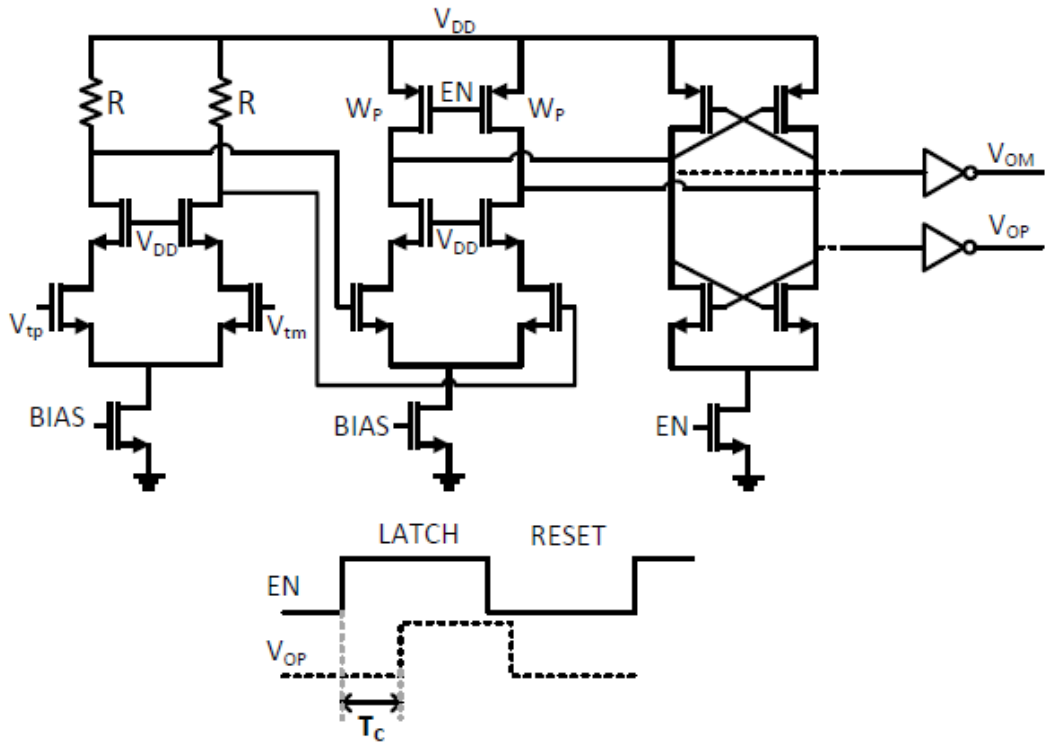
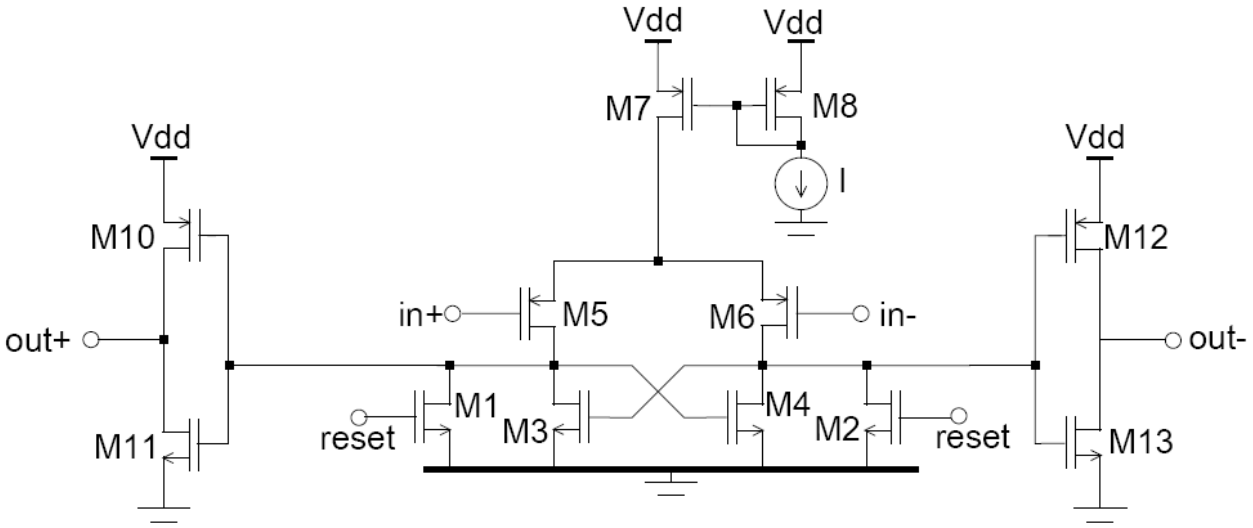


Fig. 5. Comparator schematic and timing.

In class review….
Fix problems ..

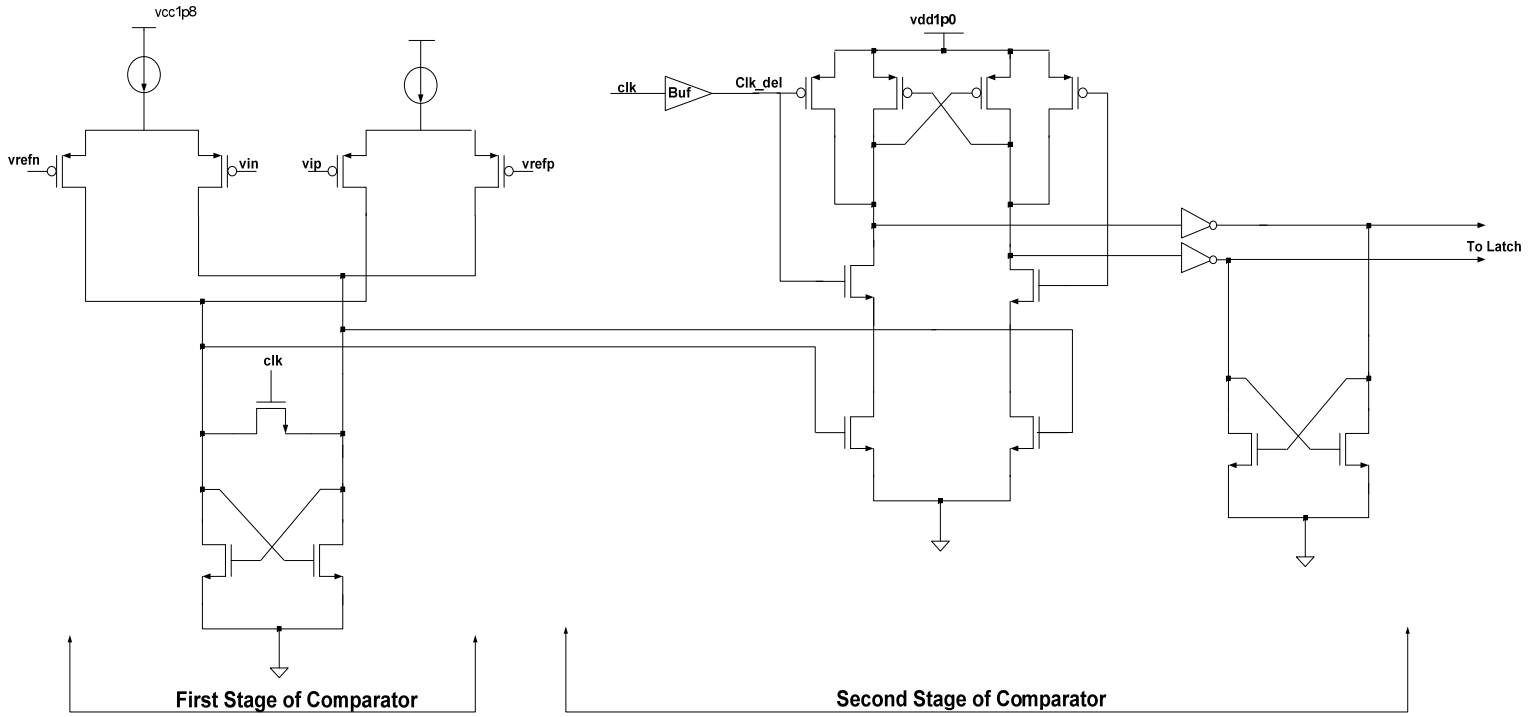


Simple

Good for low supply
Reset switch to ground
Kick back

Question can the outputs (inverter) swing to Vss ?

Differential Input Two Stage Comparator Option (no pre_amp)



More Example of comparators

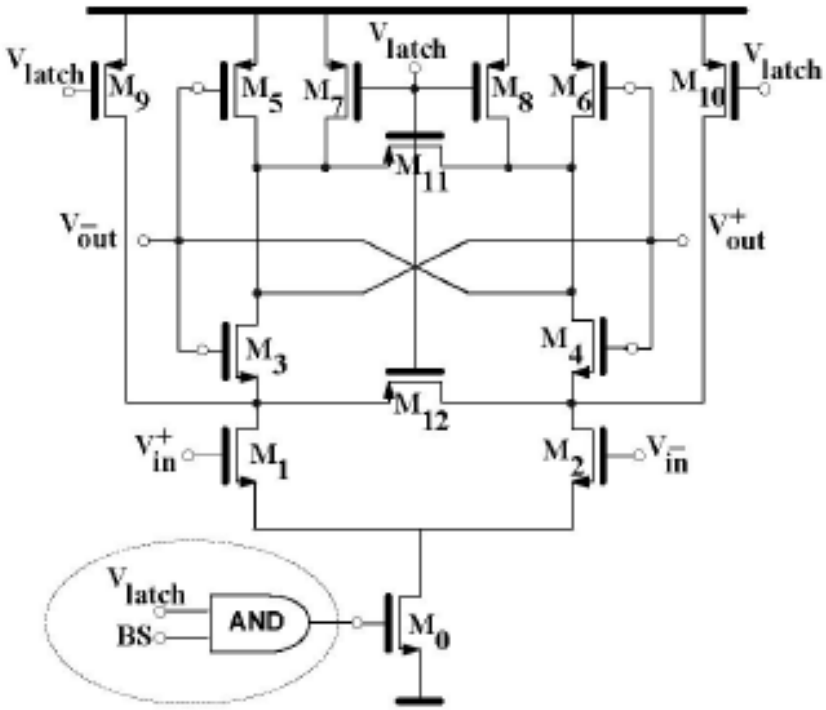


Fig. 5: High speed comparator and its switching circuit

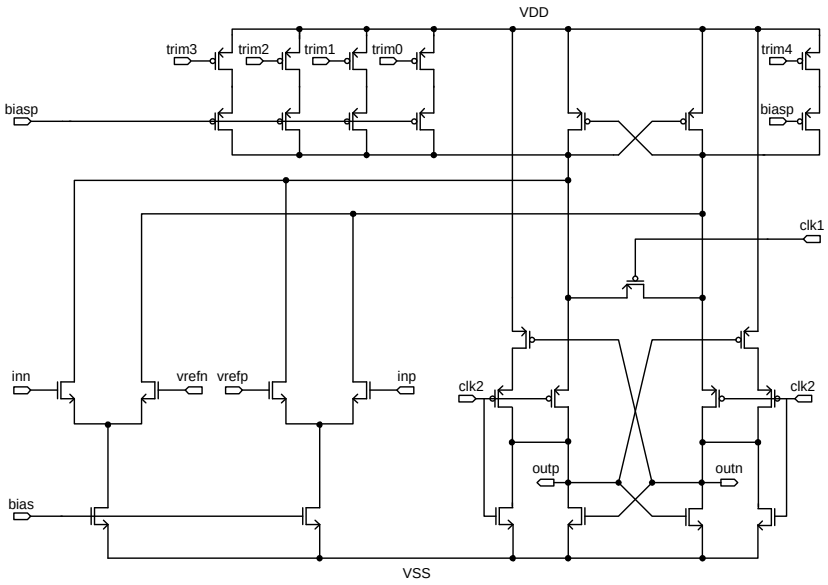
A Power-Efficient 1.056 GS/s Resolution-Switchable 5-bit/6-bit Flash ADC for UWB Applications

Jun-Xia Ma, Sai-Weng Sin, Seng-Pan U [1], R.P.Martins [2]

Offset Calibration of Comparators:

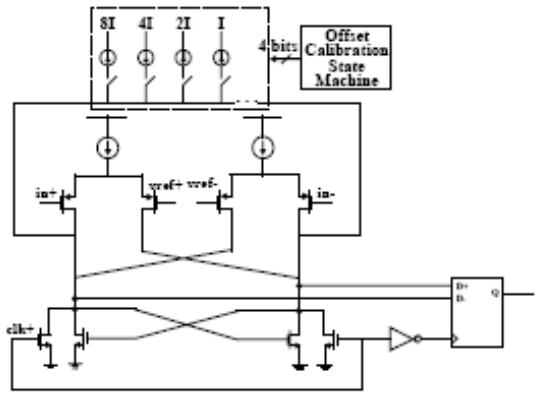
Why? → One good reason lower input capacitance

Differential – Latched with Calibration Differential



A 10.3GS/s 6bit (5.1 ENOB at Nyquist) Time-Interleaved/Pipelined ADC Using Open-Loop Amplifiers and Digital Calibration in 90nm CMOS

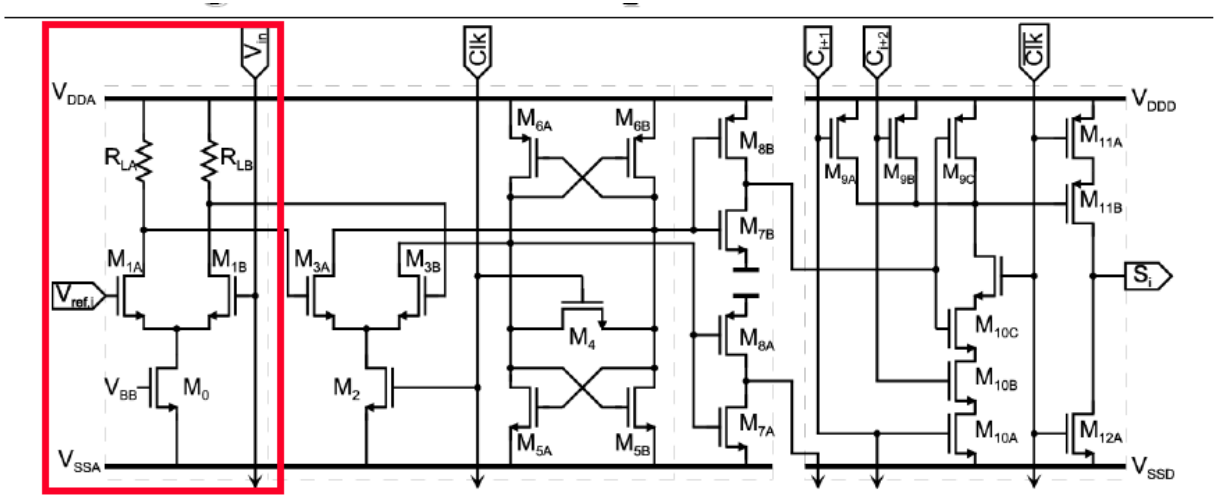
Ali Nazemi[1], Carl Grace[1], Lanny Lewyn[1], Bilal Kobeissy[1], Oscar Agazzi[1,2], Paul Voois[1], Cindra Abidin[1], George Eaton[1], Mahyar Kargar[1], Cesar Marquez[1], Sumant Ramprasad[1], Federico Bollo[2], Vladimir A. Posse[1], Stephen Wang[1], Georgios Asmanis[1]
ClariPhy Communications, Inc., 16 Technology Drive, Suite 165, Irvine, CA 92618, USA, E-mail: ali.nazemi@clariphy.com
[2]ClariPhy Argentina S.A., Cordoba, Argentina



Comparator schematic with digital offset calibration.

Special Topics – Lower kick signal back to the input

Architectures examples



- ***Pre-amplifier [M1a,M1b]***
  - **Differential Pair with resistive load**
  - **Reduce Kick-back noise**
  - **Reduce Input Referred Offset Comparator**

Source: Esat-Micas esscirc00

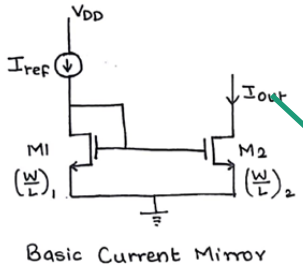
Summary: what to do

- ***Key issues*** in comparator design
  - Optimization of the ***number of stages*** to achieve the desired ***response time*** with a given ***power consumption***
  - Offset cancellation ➜ ***Autozero*** technique
  - ***Clock feedthrough***, ***power supply*** and ***common mode*** rejection ratios ➜ Fully differential structures
  - ***Overdrive recovery*** ➜ Limit the voltage swing at critical nodes or when possible introduce a ***reset*** phase

End Lecture 3

Curent sources- the **heart** of Analog blocks. In class discussions.. $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\frac{\Delta L}{L})$

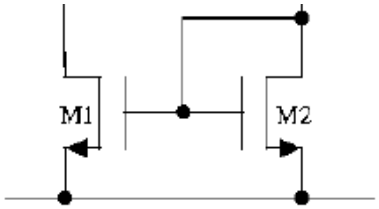
Rout makes:
the difference in I M1 vs M2
and.. Mismatch

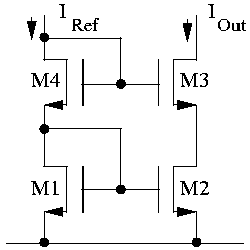


$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$

$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}$

In sat: remember mostly Vgs make the difference
Process corners… are problematic.

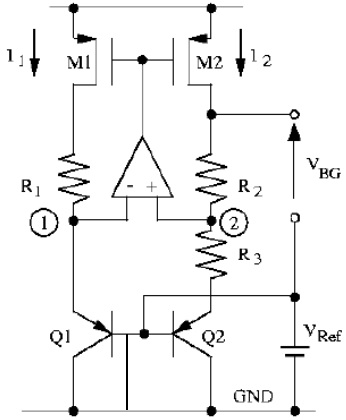




More analog if time allow

Cascode/cascade

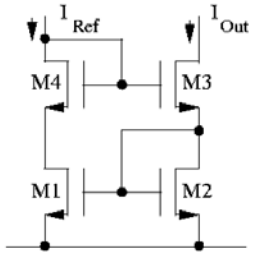
use it in vgap many places

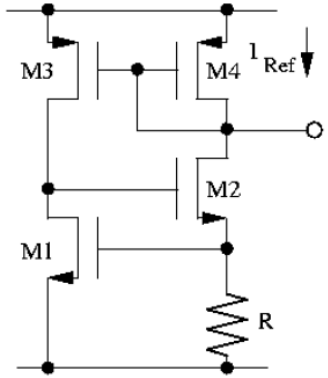


What's important ?

Compliance ?
Change as drain change ?
Noise ?
Simplicity ?

Improved Wilson Current Mirror





many more
variations exists