Welcome to

7718 semester 1 2022

Mixed Signal Electronic Circuits

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TEL AVIV UNIVERSITY אוניברסיטת תל אביב

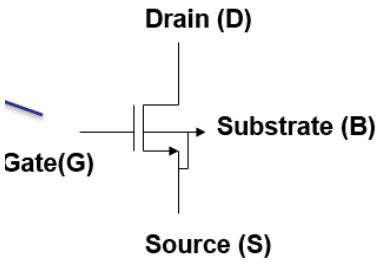
Lecture 02

Noise, and mismatches in Mixed Signal

1.Basic circuit examples, and assignment 1
2.Noise
3.Mismatche

Lectures
http://www.gigalogchip.com/lectures.html

Last lecture summary



1

$$I_{ds} = \mu C_{ox}\left(\frac{W}{2L}\right)(V_{gs} - V_{th})^2$$

2

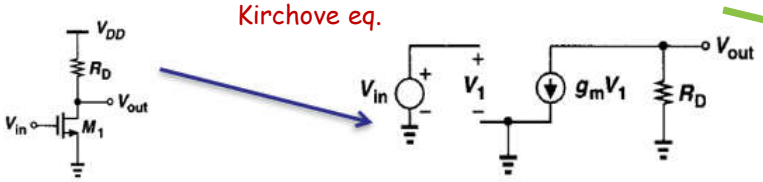
Mathematical way to model non linear with lin ckt if..I same

$$g_m \equiv \frac{\partial I_{ds}}{\partial V_{gs}} \qquad I_{ds} = g_m \cdot V_{gs}$$

$$g_{ds} \equiv \frac{\partial I_{ds}}{\partial V_{ds}} \qquad r_o = \frac{1}{\lambda \cdot I_{ds}}$$

3

Just solve Kirchove eq.



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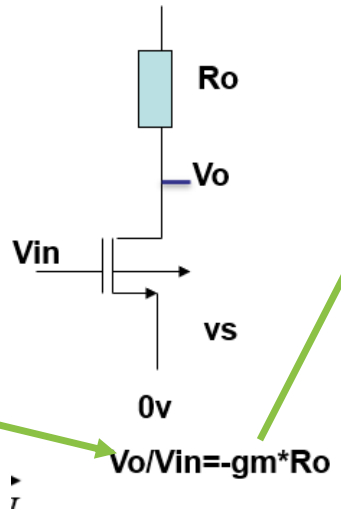
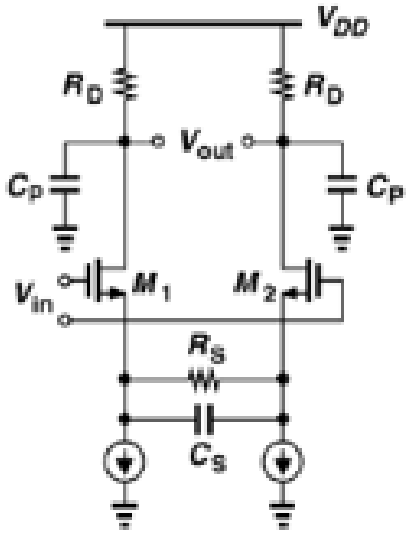


Vo/Vin=-gm*Ro

$$g_{msat} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{ds}}$$

$$g_{mwk\_inv} = \frac{I_{ds}}{KT/q}$$



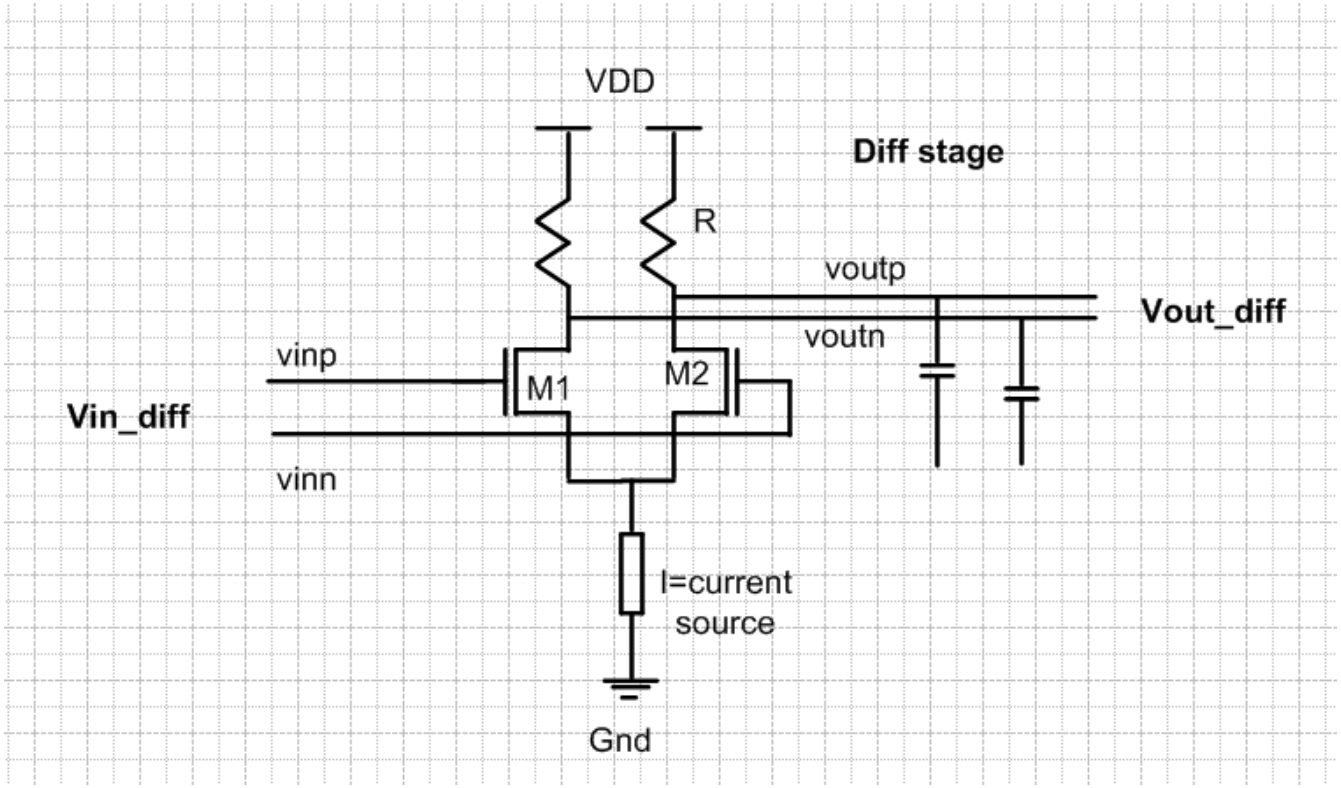
Assignment #1

I put in the site..

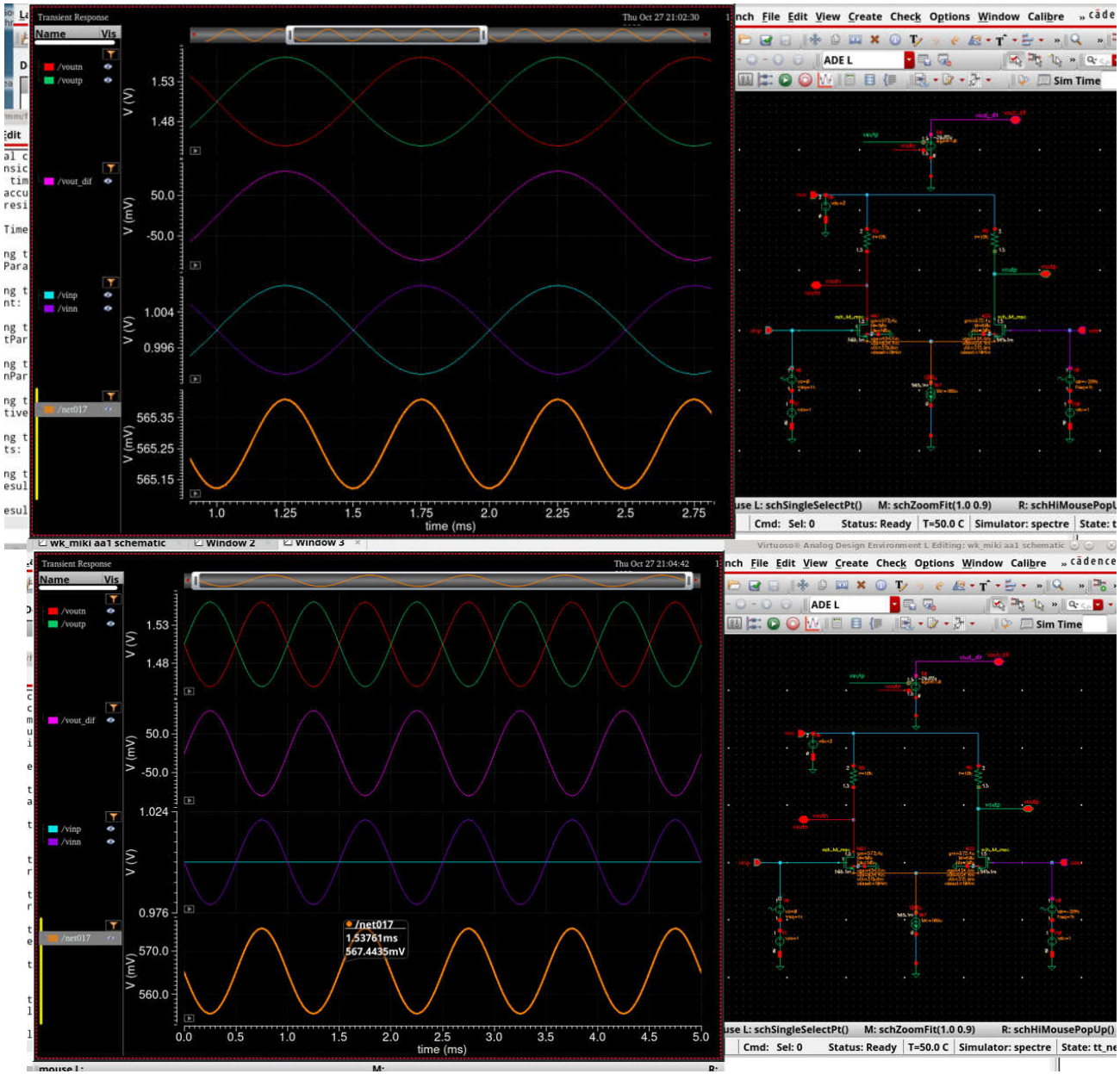
Few words..

The CTLE

Few important analog circuits: basic in class analysis



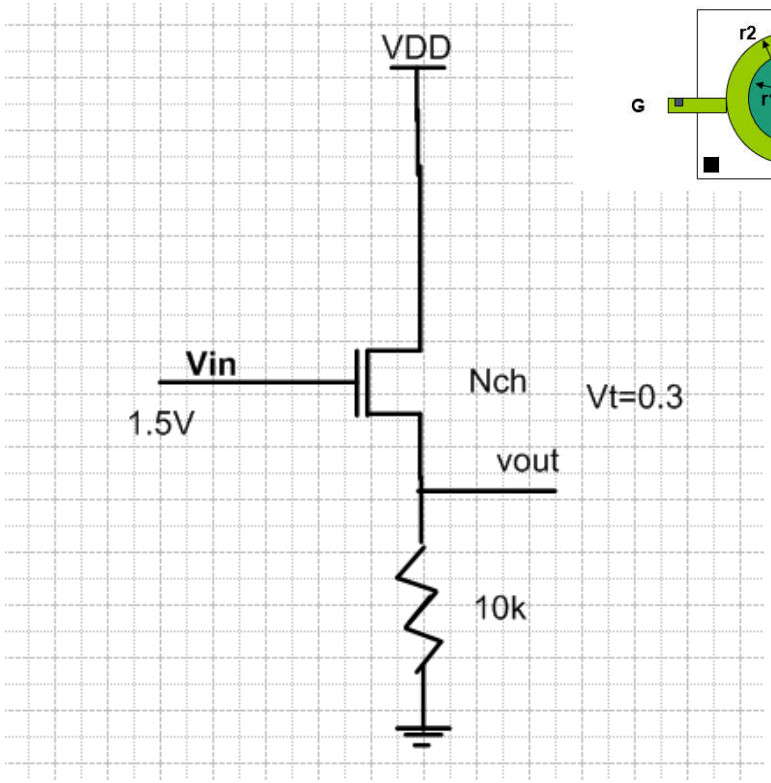
Vout_diff/Vin_diff ?



Difference between Vinp=-vinn

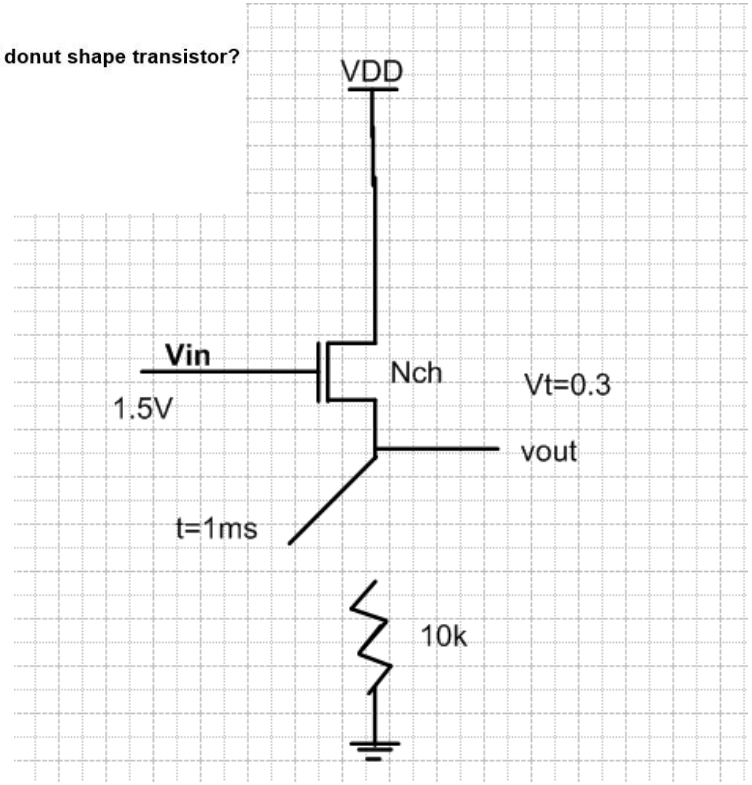
and 2vinn, 0

Few important analog circuits: basic in class analysis



optional

1. **What is W/L of a round donut shape transistor?**
2. **Can you derive it?**
3. **What is it good for?**



What's vout if Vin changed from 1.5-1.6V ?

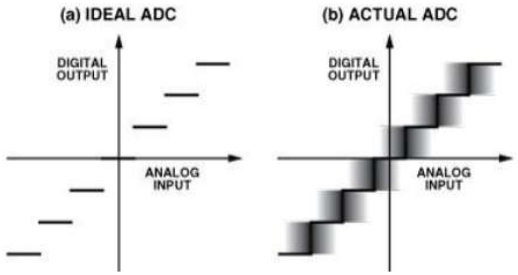
What's vout after long time ? 1Hr.

Time for noise…

Noise In resistors and CMOS transistors

Noise set the fundamental limits of performance

Impact of Noise



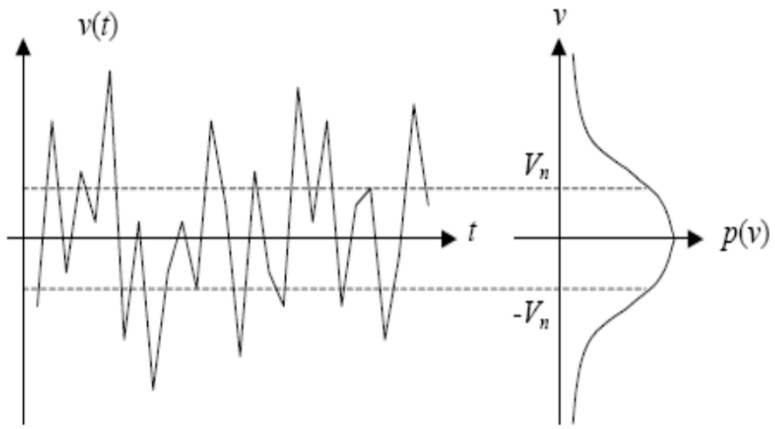
[W. Kester, "ADC Input Noise: The Good, The Bad, and The Ugly. Is No Noise Good Noise?" Analogue Dialogue, Feb. 2006]

- In essentially all moderate to high-resolution ADCs, the transition levels carry noise that is somewhat comparable to the size of an LSB
  - Noise "smears out" DNL, can hide missing codes
- Especially for converters whose input referred (thermal) noise is larger than an LSB, DNL is a "fairly useless" metric

Basics of Noise- “In time”

- Thermal energy in the device causes random charge carrier fluctuations, called Thermal Noise.
- Thermal Noise is considered a “white” noise source because its Power Spectral Density (PSD) is independent of frequency up to about f_t (or the BW of the device).

we observe Voltage or Current noise in time and construct the PDF function



Source: T.H.Lee

Root mean square is a way to quantify noise and as density in nV (mV) per square root Hz.

Example: Resistor thermal noise

The Model

Wait.. what is the noise if there is no current ?
Input referred ? Output referred ??

coulomb (symbol: C) is the **unit of electric charge**

- Take KT = 26mv x $1.6e^{-19}$ C = 41.6 e^{-22} v^2/ohm Hz
- **The model is a resistor with a voltage source of 4KTR units are V^2/Hz**

Can Take the square root – noise density Sn)

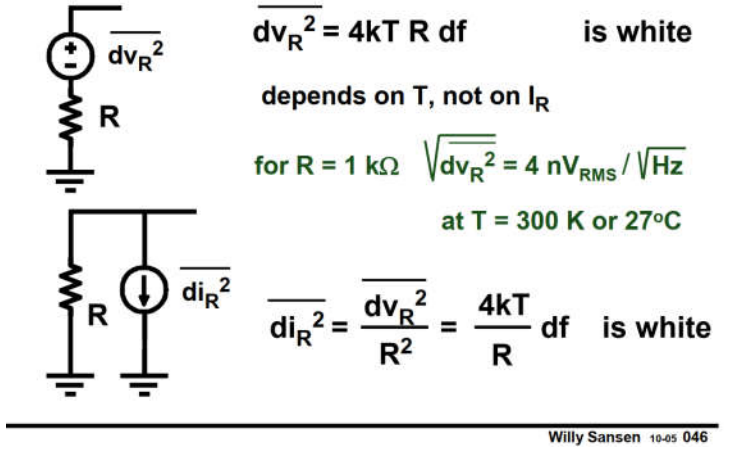
$$V_{\mathrm{T}} = \frac{kT}{q} = \frac{1.38 \times 10^{-23}\ \mathrm{J{\cdot}K^{-1}} \times 300\ \mathrm{K}}{1.6 \times 10^{-19}\ \mathrm{C}} \simeq 25.85\ \mathrm{mV}$$

$$V_{noise}^2 = 4 \cdot k \cdot T \cdot R \cdot \Delta f$$

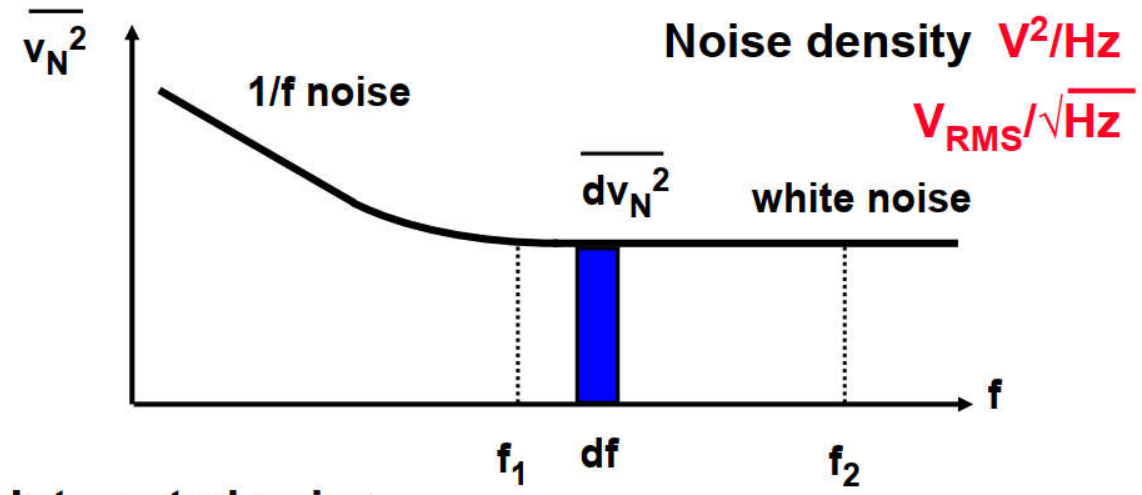
$$1K\Omega \gg 4.09(\frac{nV}{\sqrt{Hz}})$$

can think the Vnoise is **rms voltage**(its in a “bin”, density)

In class example TIA



Noise versus frequency



Integrated noise

V_{RMS}

$$\overline{v_{12}} = \sqrt{\overline{v_N^2}} = \sqrt{\int_{f_1}^{f_2} \overline{dv_N^2}\, df} = \sqrt{(f_2 - f_1)\, \overline{dv_N^2}}$$

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I always take the density and multiply by the squar root of the freqency rang: for 100Hz-10M = squre root of(10,000000-100)

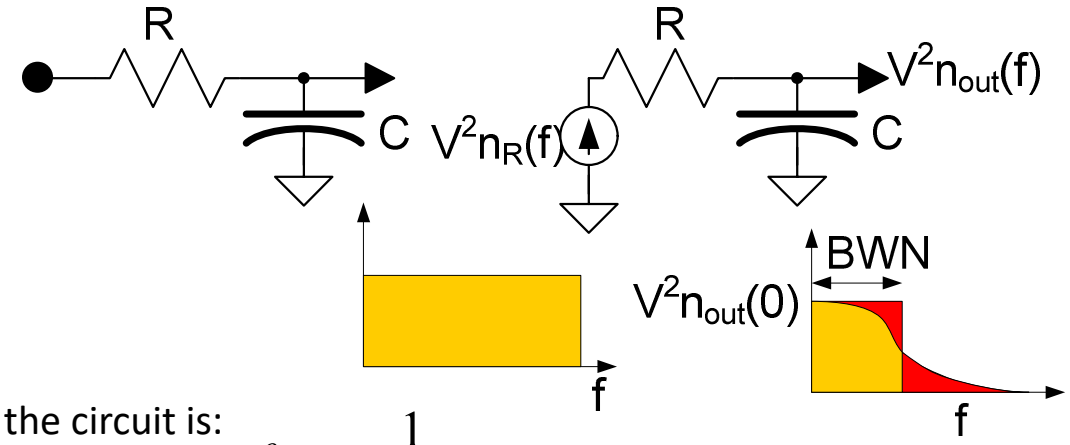
Next: what if we have a filter ?

Thermal Noise Basics – Noise at the output of an RC LPF

The thermal noise of a resistor is given by:

$$Vn_R^2(f) = 4kTR$$

The noise equivalent circuit of an RC LPF is:



The pole of the circuit is:

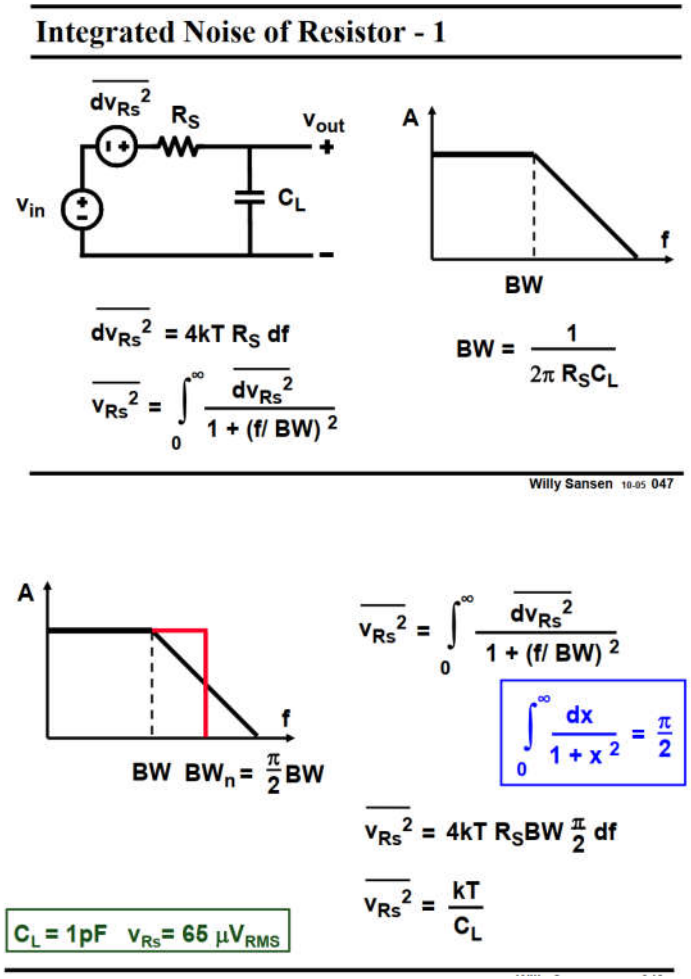
$$f_p = \frac{1}{2\pi RC}$$

We can now calculate the output noise power as:

$$\overline{Vn_{out}^2} = Vn_R^2(0) \cdot BWR = 4kTR\frac{\pi}{2}f_p = 4kTR\frac{\pi}{2}\cdot\frac{1}{2\pi RC} = \frac{kT}{C}$$

The noise charge on the capacitor has the variance:

$$\overline{Qn^2} = \overline{Vn^2}\cdot C^2 = kTC$$



Summary noise in R

Noise density (vsquare/Hz) depend on Temp and R

$$Vn_R^2(f) = 4kTR$$

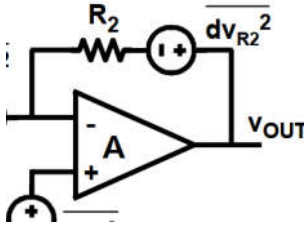
Total noise Vrms=(integrated) depend on Temp and 1/C

$$\overline{v_{Rs}^2} = \frac{kT}{C_L}$$

$C_L = 1pF \quad v_{Rs} = 65\ \mu V_{RMS}$

How about 100pF ?

In class example TIA



Noise in CMOS transistors

- For MOS, We define 2 type of noises:

- **Thermal Noise** – White noise up to f_t of the device
- **Flicker Noise** – Low frequency noise (1/f, not so low for NMOS)

It possible that in one mode or another 1/f is almost nulled

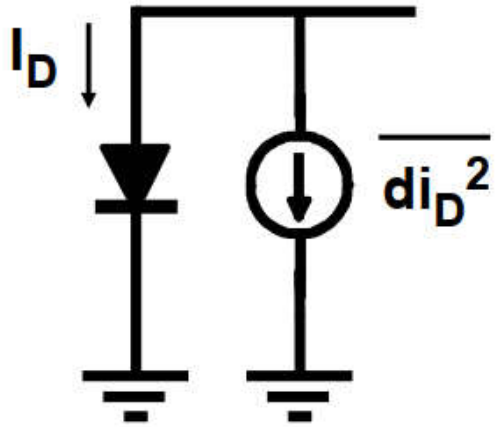
In later lecture we will see that other type of definitions for noises – Phase Noise, Electron Noise (ENC), which are all derivatives or impacted from the basic Flicker and Thermal noise (Mixing)

Thermal noise and Flicker noise

- **Thermal noise:**
  - **Thermal energy in the device causes random charge carrier fluctuations, called Thermal noise.**

- **Flicker noise:**
  - **Results from random motion of charge over potential barrier (need a gate).**

Noise of a diode is shot noise



$\overline{di_D^2} = 2q\, I_D\, df$ is white

$q = 1.6\ 10^{-19}\ C$

depends on I_D, not on T

for $I_D = 50\ \mu A$ $\sqrt{\overline{di_D^2}} = 4\ pA_{RMS} / \sqrt{Hz}$

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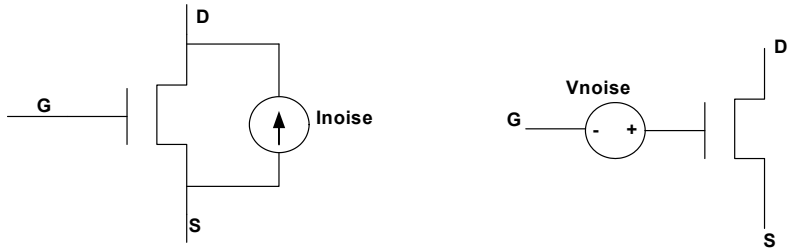
Transistor Thermal and 1/f Noise

Gamma a process number ~1-2)

on class derive I noise



I=300uA =>gm=1e-3
V=2.7nv/sqrtHz

Thermal Noise

$$I_{noise}^2 = \left(\frac{2}{3}\right) 4 \cdot k \cdot T \cdot \gamma \cdot g_m \cdot \Delta f$$

$$V_{in\_noise}^2 = \frac{\left(\frac{2}{3}\right) 4 \cdot k \cdot T \cdot \gamma}{g_m} \Delta f$$

1/f Noise

$$I_{noise}^2 = \frac{k_0 \cdot k \cdot T \cdot g_m^2}{W \cdot L \cdot f} \Delta f \sim \frac{1}{L^2 f} \Delta f$$

function of L^2 not W

$$V_{in\_noise}^2 = \frac{K_0 \cdot k \cdot T}{W \cdot L \cdot f} \Delta f$$

function of g_m (sqrt W/L)

Models:

- For a ***Voltage*** Mode device (input referred noise)
- For a ***Current*** Mode device (a current source)

Noise and frequency

$$V_{in\_noise}^2 = \frac{\left(\frac{2}{3}\right) 4 \cdot k \cdot T \cdot \gamma}{g_m} \Delta f$$

- The total noise (input referred) is always the area under the density noise curve the integral from f=0 to f="what you like"

- Example: the total thermal noise from 1KHz-10MHz noise is:

$$V_{total-1-10MHz\_noise} = \sqrt{\frac{\left(\frac{2}{3}\right) 4 \cdot k \cdot T \cdot \gamma}{g_m}} \cdot \sqrt{9.999}$$

Noise in not always flat in all frequency

Noise as W ,L , g_m

Voltage Mode:

- Thermal noise:

$$\frac{V_n^2}{\Delta f} = \frac{8KT}{3g_m}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_{ds}}$$

use Large W/L (g_m) → for low noise

- 1/f noise:

$$\frac{V_n^2}{\Delta f} = \frac{K_0 KT}{fWL}$$

use Large area WxL → Lower noise

But it could be a loosing game spend a lot of gm to reduce the noise a little..

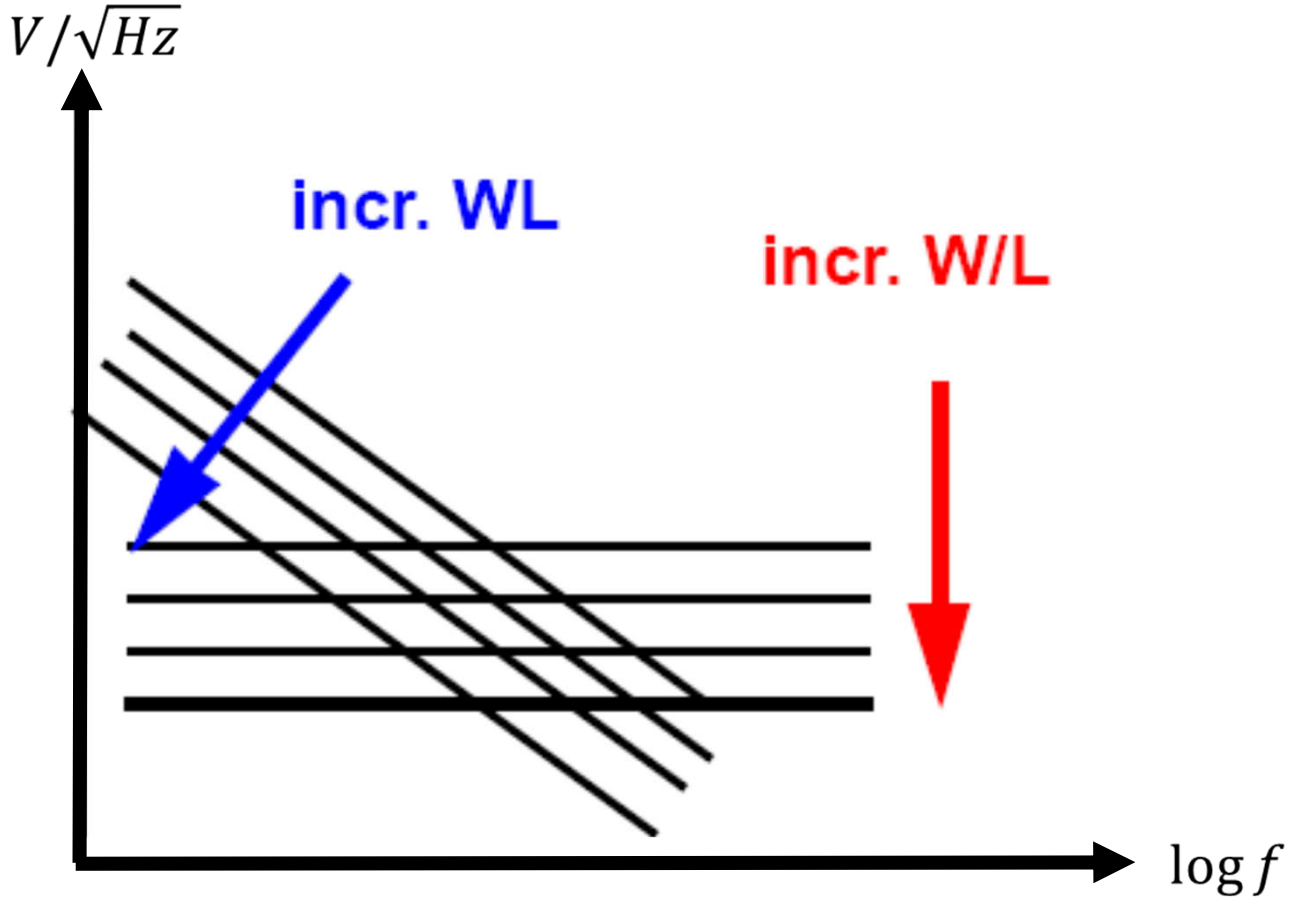
Why ? I and C

Drain Current Mode:

$$\frac{I_n^2}{\Delta f} = \frac{8KT\,g_m}{3}$$ Function of g_m (sqrt W/L)

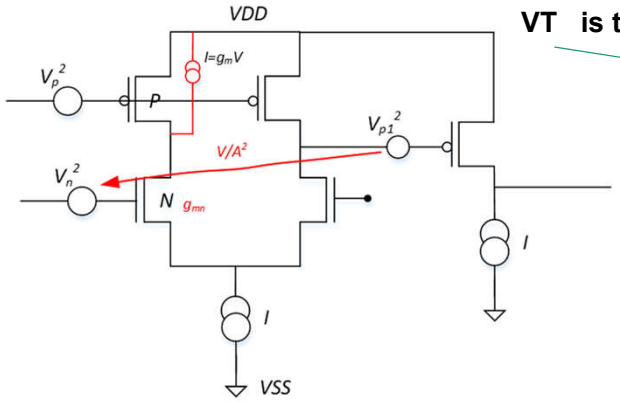
$$\frac{I_n^2}{\Delta f} = \frac{K_0 KT\,g_m^2}{fWL}$$ Function of L^2 not W

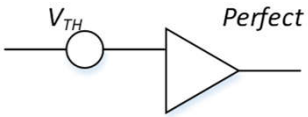
For fixed I_{ds} in strong inversion (voltage mode)



Flicker and thermal noises Interactions

Example circuit noise of 2 Gain Stages On Board





$$v_n^2 = \frac{8}{3}\frac{kT}{g_{m_n}}$$

$$v_p^2 = \frac{8}{3}\frac{kT}{g_{m_p}}$$

$$v_{p1} = \frac{8}{3}\frac{kT}{g_{m_{p1}}}$$

Effect of Thermal Noise

VT is the **input referred noise**

$$V_T^2 = V_n^2 + \frac{V_{P_1}^2}{\left(g_{m_n}R_o\right)^2} + \frac{g_{m_p}^2}{g_{m_n}^2}V_P^2$$

$$V_T = \sqrt{\frac{8}{3}\frac{kT}{g_{m_n}} + \frac{\frac{8}{3}\frac{kT}{g_{m_{p1}}}}{g_{m_n}^2 R_o^2} + \left(\frac{g_{m_p}^2}{g_{m_n}^2}\right)\cdot\frac{8}{3}\frac{kT}{g_{m_{p1}}}}$$

$$= \sqrt{\frac{8}{3}\frac{kT}{g_{m_n}} + Small + g_{m_p}\cdot\frac{8}{3}kT\cdot\frac{1}{g_{m_n}^2}}$$

Make g_{mn} Large W↑ and L↓

Make g_{mp} Low W↓ and L↑

For Converter

$$INL = \frac{1}{2}LSB \gg \frac{V_F^2}{2^n - 1} \approx \frac{1}{2}V_T$$

Limit V_T

Use Large L for Loads and Large W/L for Input Pair

Mismatch

Passives: resistors and capacitors in silicon

- One of the most critical parameters in mixes signal design.
- Mostly ignored with normal simulators

Polysilicon

Silicon Passive elements used in Mixed Signal

Silicon Resistors: R=v/i

- In Silicon
  R = Sheet Resistance x Number of square.

Made of Si doped material.(poly and N+ or P+ or both)

- Problems:
  They have parasitic capacitances, (BW limitation) and temperature variations :

Grown from pyrolytic decomposition of silane (SiH_4) at about 600°C.

The polycrystalline structure is made of monocrystal grains size in the range of 0.1 - 1 µm.

The typical layer are 200 - 600 nm thick with long term standard deviation in the 2% range.

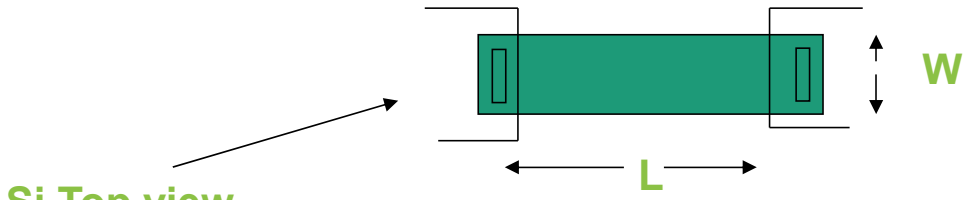
The mobility is low because of the grain border resistance (30-40 cm^2/Vs).

In order to have a low sheet resistance the polysilicon must be strongly doped (10^{20}-10^{21} cm^{-3}). Part of the doping saturates the localized levels due to the grain border. The sheet resistance is in the range 20 - 40 Ω/□.

The sheet resistance can be reduced by using sandwich layers (polysilicide) made of 200 nm of polysilicon covered with a film of refractory metal silicide (WSi_2, $MoSi_2$, $TiSi_2$). The sheet resistance is reduced to 1 - 5 Ω/□.

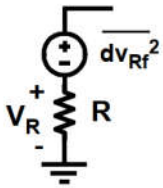
$$R = R_s \cdot squares(1 + \alpha T/T_0)$$

$$R \propto 1/(\mu q N a)$$



In silicon

A resistor also has 1/f noise



$$\overline{dv_{Rf}^2} = V_R^2 \frac{KF_R R_\square}{A_R} \frac{df}{f}$$ is 1/f

$KF_{RSi} \approx 2\ 10^{-21}\ Scm^2$

$KF_{Rpoly} \approx 10\ KF_{RSi}$

for R = 1 kΩ with 20 □'s of 50 Ω/□ and 1 µm wide and V_R= 0.1 V

$\sqrt{\overline{dv_{Rf}^2}} = 16\ nV_{RMS}/\sqrt{Hz}$ at 1 Hz

Ref. Vandamme, ESSDERC '04

Passive Element Tolerance

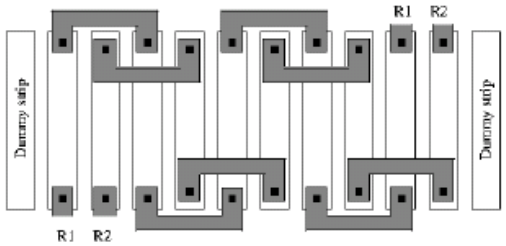
❑ Common type of resistors in IC - silicon

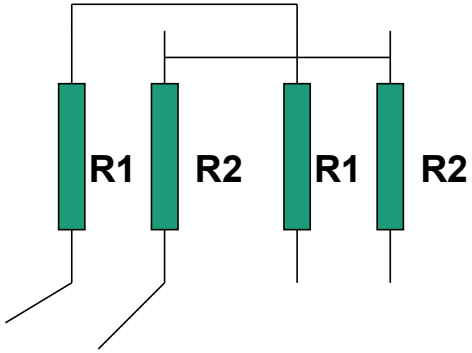
Resistor	Range [%]	Ohm/sq Value	Matching [%] (1x1uu)	ppm/c, ppm/v
Poly W/O Siliside With Siliside	± 15	 200 – 1k 6	 2 -	 0-400 ppm/c -
N+/P+	± 20	20-100	-	3000 ppm/c, large v
N well	± 20	2k-4k	--	Large
1 contact	± 50	1-3	---	----

Tolerance is not mismatch…

Layout of resistors on Silicon

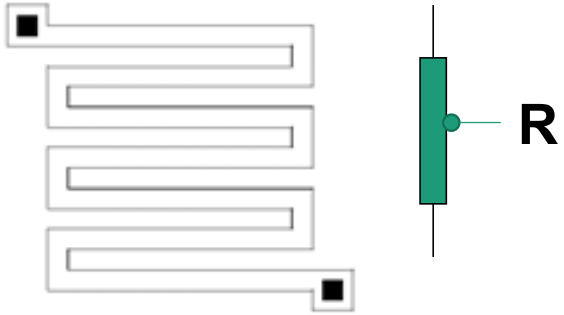
Interdigitized structure :





Good matching

symbol



$$R = R_s \cdot length/width$$

$$R_{total} = R + 0.5 \cdot R_s(number_{turns}) + contact\_resistance$$

Basic partial derivatives

$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

$$y = \frac{x_1 x_2}{x_3}$$

$$\frac{\partial y}{y} = ?$$

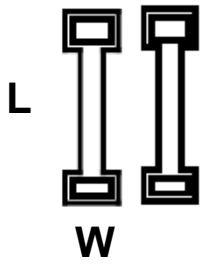
$$\left.\frac{\partial y}{y}\right|_{x_1} = \frac{\left(\frac{x_1}{x_3}\right) \partial x_2}{\left(\frac{x_1}{x_3}\right) x_2} = \frac{\partial x_2}{x_2}$$

$$\left.\frac{\partial y}{y}\right|_{x_2} = \frac{\partial x_2}{x_2}$$

$$\left.\frac{\partial y}{y}\right|_{x_3} = \frac{x_1 x_2 x_3^{-2} \partial x_3 (-1)}{\left(\frac{x_1 x_2}{x_3}\right)} \frac{-1}{x_3} \partial x_3$$

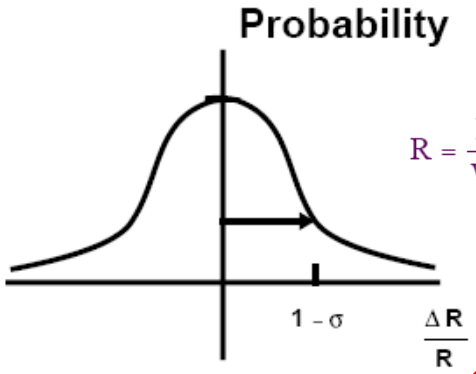
$$\left[\frac{\partial y}{y}\right]^2 = \left[\frac{\partial x_1}{x_1}\right]^2 + \left[\frac{\partial x_2}{x_2}\right]^2 + \left[\frac{\partial x_3}{x_3}\right]^2$$

Mismatches



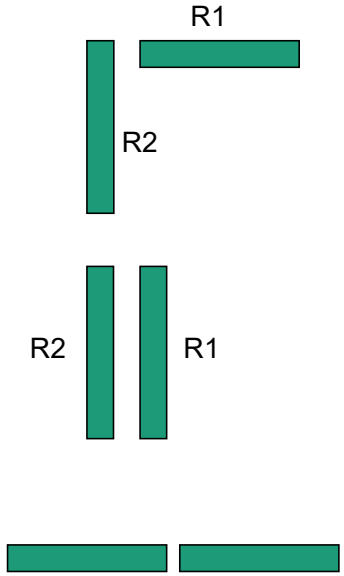
$$R = \frac{R_1 + R_2}{2}$$

$$\Delta R = R_1 - R_2$$



$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$

$$\left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)^2 + \left(\frac{\Delta X_j}{X_j}\right)^2$$



Layout position can destroy/improve mismatches

$\left(\frac{\Delta X_j}{X_j}\right)$

- ❑ Implant dose
- ❑ Side diffusivity
- ❑ Deposition rate

$\left(\frac{\Delta L}{L}\right)\left(\frac{\Delta W}{W}\right)$

- ❑ Etching
- ❑ Boundary
- ❑ Side diffusivity

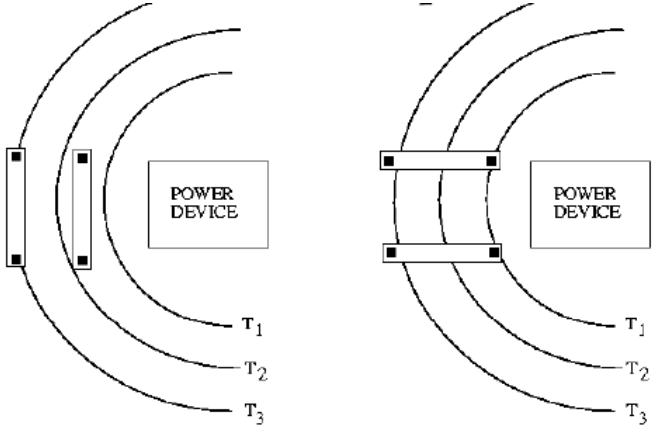
$\left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)$

- ❑ Polysilicon grain size
- ❑ Doping dose
- ❑ Crystal defects
- ❑ Stress
- ❑ Temperature

source: F. Maloberti

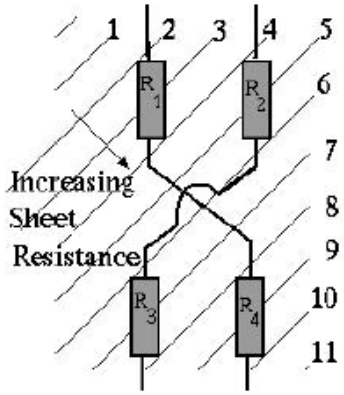
Improve Mismatch (Accuracy) Errors : “Good to Do”

A – Temperature:



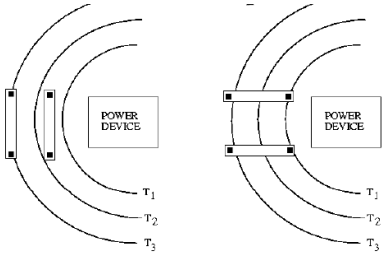
source: F. Maloberti

B – Sheet resistance



"James C. Daly et al."

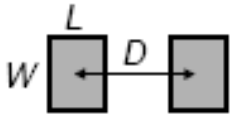
C – Stress: away from edges..



Mismatches – Modelling – ”Pelgrom Rule”

MISMATCHING
In Current-Steering D/A Converters

M.J.M Pelgrom, *et al* (1989): mismatching parameter for two equal transistor of dimensions *W* x *L* separated a distance *D*.



‘Random’ mismatch

Transistor sizing

‘Systematic’ mismatch

Layout techniques

$$\sigma_{V_T} = \frac{A_{V_T}}{\sqrt{WL}} + S_{V_T}^2 D^2$$

$$\frac{\sigma_\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}} + S_\beta^2 D^2$$

$$\frac{\sigma_\gamma}{\gamma} = \frac{A_\gamma}{\sqrt{WL}} + S_\gamma^2 D^2$$

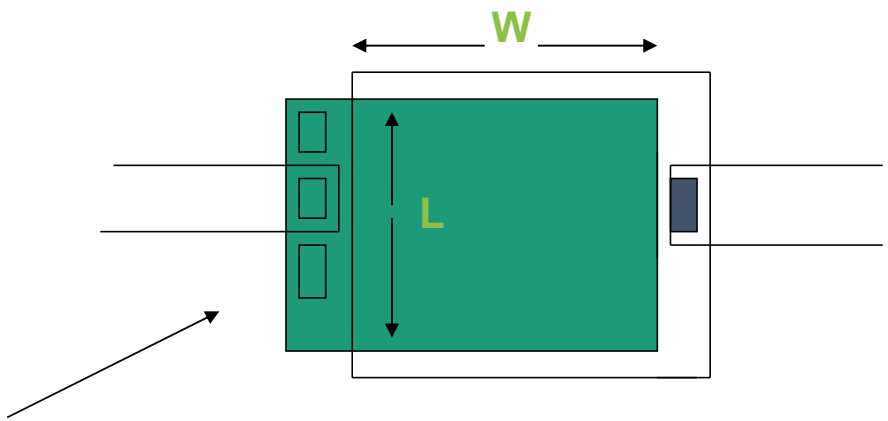
Capacitors layout and mismatched

Plated Capacitors

C= Ca x Area = Ca x W x L (W and L are dimension of plates)

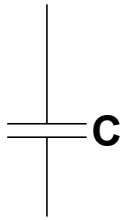
1-4 ff/uu, 20pF is already a large capacitors for silicon application.

“Core Oxide caps”- will be reviewed later lectures.



Si Top view

I=C dv/dt



Symbol

Capacitors

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

From here to here..

$$y = \frac{x_1 x_2}{x_3}$$

$$\frac{\partial y}{y} = ?$$

$$\left.\frac{\partial y}{y}\right|_{x_1} = \frac{\left(\frac{x_1}{x_3}\right)\partial x_2}{\left(\frac{x_1}{x_3}\right)x_2} = \frac{\partial x_2}{x_2}$$

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

$$\left.\frac{\partial y}{y}\right|_{x_2} = \frac{\partial x_2}{x_2}$$

$$\left.\frac{\partial y}{y}\right|_{x_3} = \frac{x_1 x_2 x_3^{-2} \partial x_3 (-1)}{\left(\frac{x_1 x_2}{x_3}\right)} \frac{-1}{x_3} \partial x_3$$

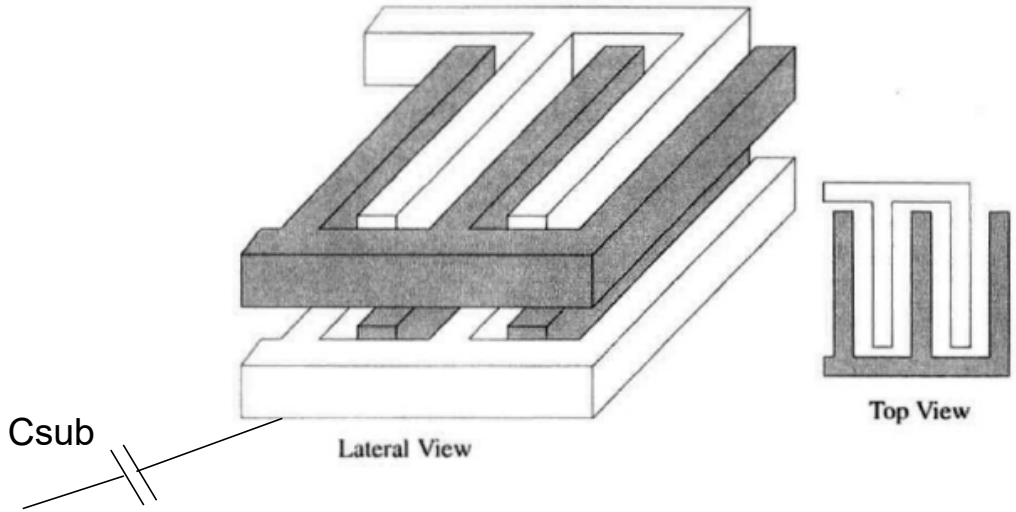
Insulator ~Si02

$$\left[\frac{\partial y}{y}\right]^2 = \left[\frac{\partial x_1}{x_1}\right]^2 + \left[\frac{\partial x_2}{x_2}\right]^2 + \left[\frac{\partial x_3}{x_3}\right]^2$$

- Mismatch model: should know but **ignore the above and use pelgrom rule !**
- Given mismatch for certain area everything and 4 time the area means double the matching

Metal capacitors

Metal thickness ~ 2000-5000A (A=Angstrom)



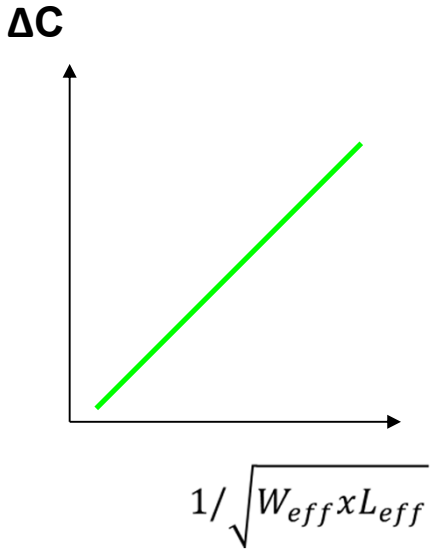
Example :

C= 2 e-^{3} pF/uu Variations = +/- 20%

If for a Given 2ff=2% mismatch - process number.

Then for a 100ff capacitor we will ger

Matching dc/c→ 100ff => 2/7 = 0.28%



More parameters:

Temco~0 C to C_{sub} (parasitic) ~ 10:1→ 30:1Variations = +/- 20%

Noise = 192uV..

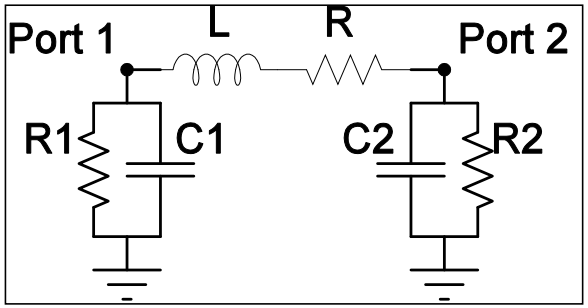
In reality we characterize a process capacitor and resistors in silicon mismatch as

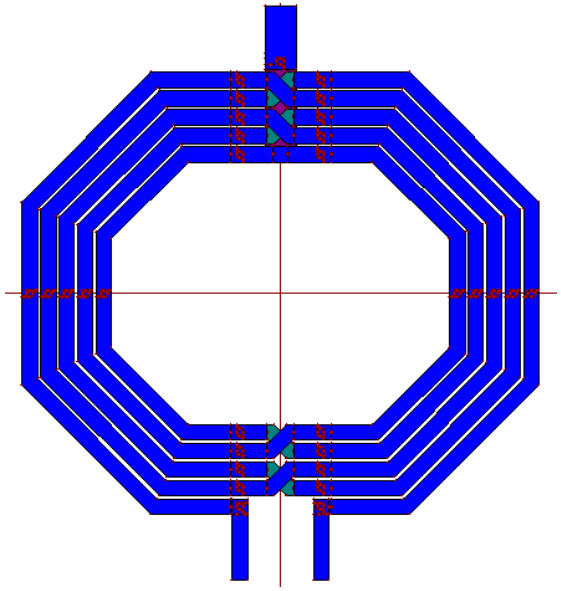
Smallest 1 square = x%
from than on we can deduce the mismatch to any value

Inductors

Inductors are also becoming a common elements- we will not go over the detail of inductor design in this course (only the basics once we go over PLLs lecture)

$$L_{self} = \frac{\mu_0}{2\pi}\left[l \ln\left(\frac{2l}{w+t}\right) + \frac{l}{2} + 0.2235(w+t)\right] \quad (1)$$





Source: Stanford,synopsys, and HP paper on L modelling

Mismatches in transistors

First test:

- Is it a current source mode?
- Is it a voltage mode device?
- Is it a switch?

Mixed signal design must address:

- Can we live with that?
- If not can we “calibrate” or fix this error?

Mismatches- V_{th}.

- Process deviation:
  - Threshold voltage is highly process dependent:

Vth=VFB - Qss/Cox + Vsub +2|Φp| + |Qd|/Cox,

$$V_{th} = V_{FB} - \frac{Q_{ss}}{C_{ox}} + V_{sub} + 2|\phi_p| + \frac{|Q_d|}{C_{ox}}$$

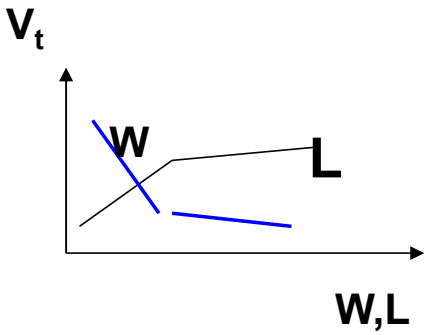
Where:

V_{FB} – Flat Band Voltage,
Q_{ss} – Surface Charge per unit area,
V_{sub} – Substrate Voltage,
$2_{|\Phi p|}$ – Voltage required for strong inversion, doping gradients
Q_d – Depletion charge per unit area in the depletion region
C_{ox} – Oxide Capacitance per um2, depends on oxide thickness

- All of them except V_{sub} are process dependent and randomly or graded distributed
- Layout mismatch: Voltage drop on along power line can cause graded error

Mismatches- history

- First belief was based on measured data:
- Very L dependent and Very W dependent

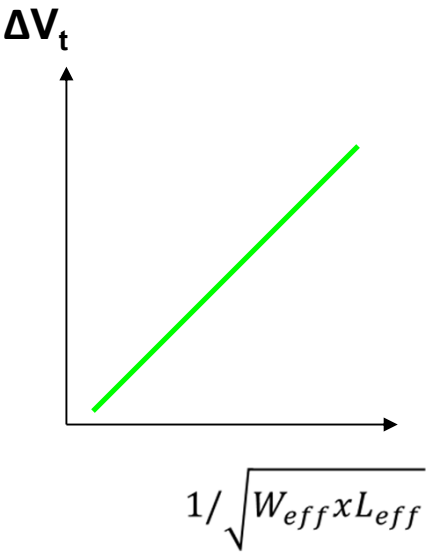


- Low L Vt. goes down – so variations is large
- Low W Vt. goes up – so variation is large

- Today Pelgrom law define most mismatches as function of area WxL

- And simulators namely monte carlo do the job of finding the sigma mismatch of large blocks

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}}$$



Note on C1 from last page

- C1 is in today design 2-10 mV for W x L =1
- C1 has a strong dependency on manufacturing – we do not have much control
- C1 follow ~ 1.5 t_{ox} (in nm -> mv) as a “rule of thumb” – use thin oxide devices
- C1 can be different for different layouts – we have control

Example for C1.

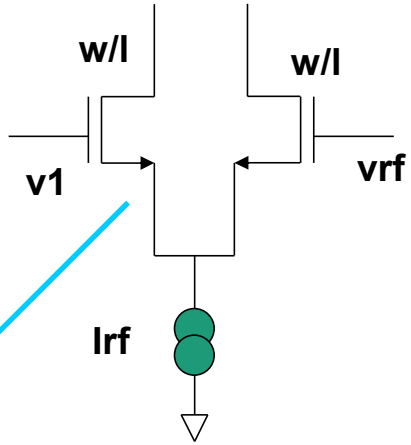
~ 3nm tox -- 90nm process ~ 4.5mv um
0.18um process tox=4nm ~ 6mv x um
3.3v process, tox~7nm ~ 10mv x um

V Mismatches – saturation region

$$\sigma^2(I_D) = \frac{\beta^2}{2}(V_{GS} - V_T)^2 * \sigma^2(\Delta V_T) + I_D^2 * \sigma^2(\frac{\Delta L}{L})$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L}$$

"never mind" this.. create a design model



amplifiers, comparators offset.

amplifiers, comparators offset.

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}} \rightarrow \propto \frac{1}{\sqrt{W_{eff} \times L_{eff}}}$$

increase area for better results
What happen to input cap ?

Current mismatches in saturation – first method

$$I = k\frac{W}{2L}(V_{GS}-V_T)^2 = \alpha(V_{GS}-V_T)^2$$

$$\Delta I + I = k\frac{W}{2L}(V_{GS}+\Delta V-V_T)^2 = \alpha(V_{GS}-\Delta V-V_T)^2$$

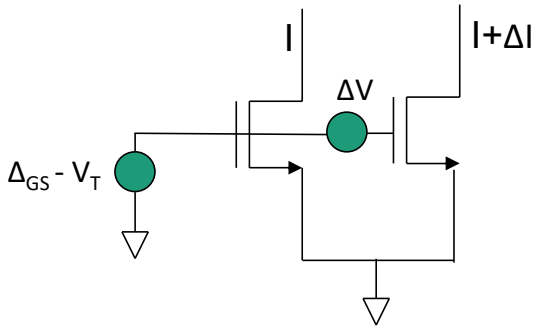
$$\Delta I = \alpha[(V_{GS}-\Delta V-V_T)^2-(V_{GS}-V_T)^2]$$
$$= \alpha[(V_{GS}-V_T)^2+\Delta V^2+2(V_{GS}-V_T)\Delta V-(V_{GS}-V_T)^2]$$

$$\Delta I = \alpha\cdot 2(V_{GS}-V_T)$$

$$\frac{\Delta I}{I} = \frac{\alpha\cdot 2(V_{GS}-V_T)\Delta V}{\alpha(V_{GS}-V_T)^2} = \frac{2}{V_{GS}-V_T}\cdot\Delta V = \left[\frac{2}{V_{GS}-V_T}\right]\cdot\frac{\sigma_{(V_T)}}{\sqrt{W\times L}}$$

$$\left(\frac{\Delta I}{I}\right)^2 = \left(\frac{C_1}{\sqrt{W\times L}}\right)^2\frac{4}{(V_{GS}-V_T)^2}$$

One Way



$$\frac{\sigma^2(I_D)}{I_D^2} = \left\{\frac{\beta}{I_D}\sigma^2(\Delta V_T)+\sigma^2\left(\frac{\Delta L}{L}\right)\right\} = \left\{\frac{2}{(V_{GS}-V_T)^2}\sigma^2(\Delta V_T)+\sigma^2\left(\frac{\Delta L}{L}\right)\right\}$$

Current mismatches in saturation – second method use C1

$$\frac{\Delta I}{I} = \frac{g_m \cdot \Delta V}{I} = \frac{\sqrt{2k\frac{W}{L}I}}{I}\Delta V \qquad \Delta I = g_m \cdot \Delta V$$

$$= \frac{2k\frac{W}{L}}{\sqrt{I}}\Delta V = \frac{\sqrt{2k\frac{W}{L}}}{\sqrt{k\frac{W}{2L}(V_{GS}-V_T)}}\Delta V = \frac{2}{V_{GS}-V_T}\Delta V$$

$$\boxed{\frac{\Delta I}{I} = \frac{2}{V_{GS}-V_T} \cdot \frac{C_1}{\sqrt{W \times L}}}$$

Second Way- same results..

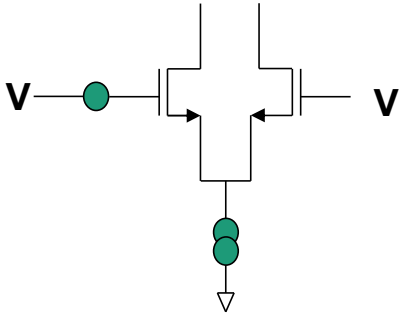
Large V_{GS}!

Added W and L mismatches

$$\frac{\Delta I_D}{I_D} = \left[\left\{\frac{\Delta\frac{W}{L}}{\frac{W}{L}}\right\} + \left\{\frac{2\Delta V_T}{V_{GS}-V_T}\right\}\right]$$

Mismatches/Offset V_s, L, W,

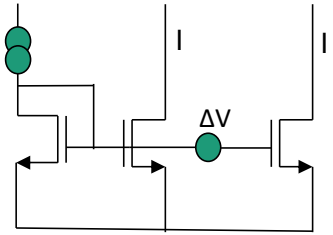
Amplifiers, comparators minimize Offset (mismatches)



$$\Delta V = \frac{C}{\sqrt{W \times L}} => Increase\ W \times L\ area$$

Proportional to $\boxed{\frac{1}{\sqrt{W \times L}}}$

Current source minimize I Offset Mismatch

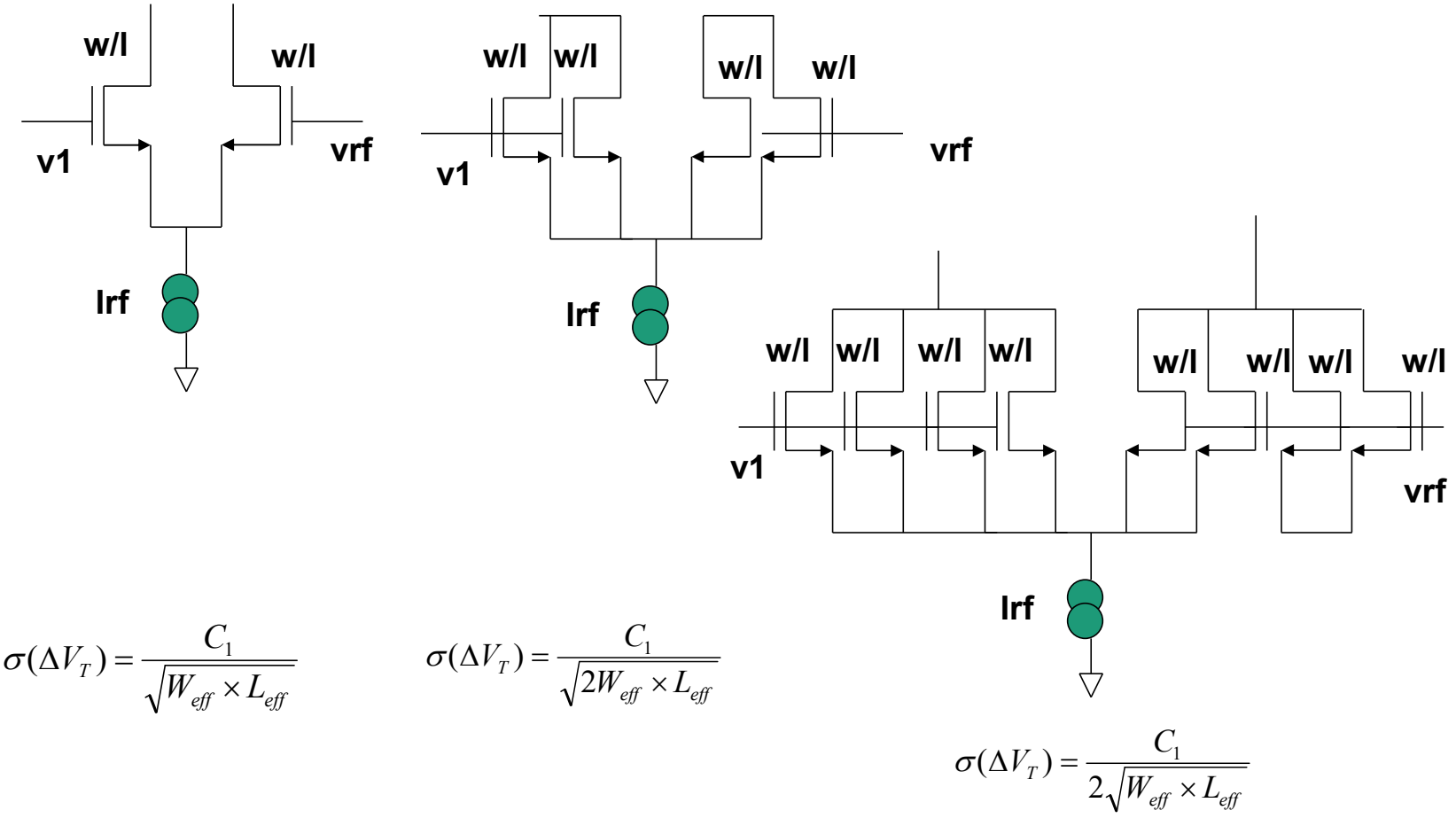


no ΔV → I+ΔI

$$\Delta I = g_m \cdot \Delta V = \frac{g_{mC_1}}{\sqrt{W \times L}} = \frac{\sqrt{\left(k\frac{W}{L}2I\right)}}{\sqrt{W \times L}} \cdot C_1$$

$$\Delta I = \frac{C\sqrt{2I\mu_0 C_{ox}}}{L} \sim \frac{1}{L} \quad \gg\gg Large\ L$$

Example: mismatches/Offset



$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{W_{eff} \times L_{eff}}}$$

$$\sigma(\Delta V_T) = \frac{C_1}{\sqrt{2W_{eff} \times L_{eff}}}$$

$$\sigma(\Delta V_T) = \frac{C_1}{2\sqrt{W_{eff} \times L_{eff}}}$$

4x transistor area = ½ offset improvement

End of lecture 02