Welcome to

0510.7720.01 Winter semester 2021

Mixed Signal Electronic Circuits

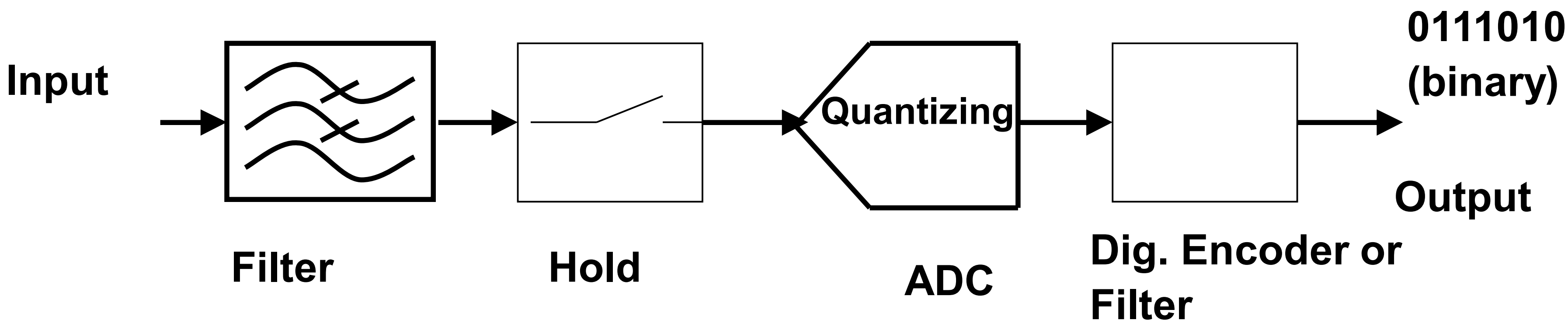
Instructor: Dr. M. Moyal

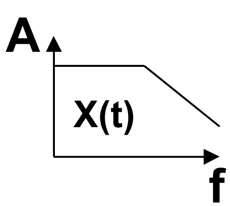
Lecture 02

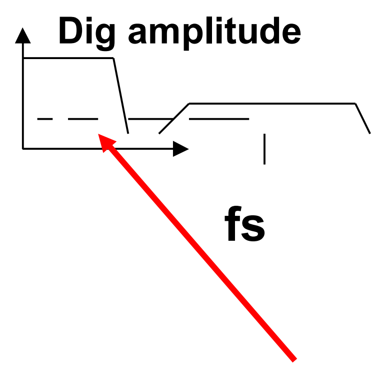
Converters Basic Theory and Definitions

1. System applications, Rate,
2. Definitions/terms- SNR, ENOBs, DNL, INL..

ADC Converter Building Blocks







Noise: random
systematic

The Output Rate: “MS/s” definition

- ❑ **It’s the Rate of digital bits are coming out**

- ❑ Depends on signal input maximum BW
  Mostly it’s the clock rate (non over sampled system).

- ❑ The maximum data frequency is ½ of this.

An Example:

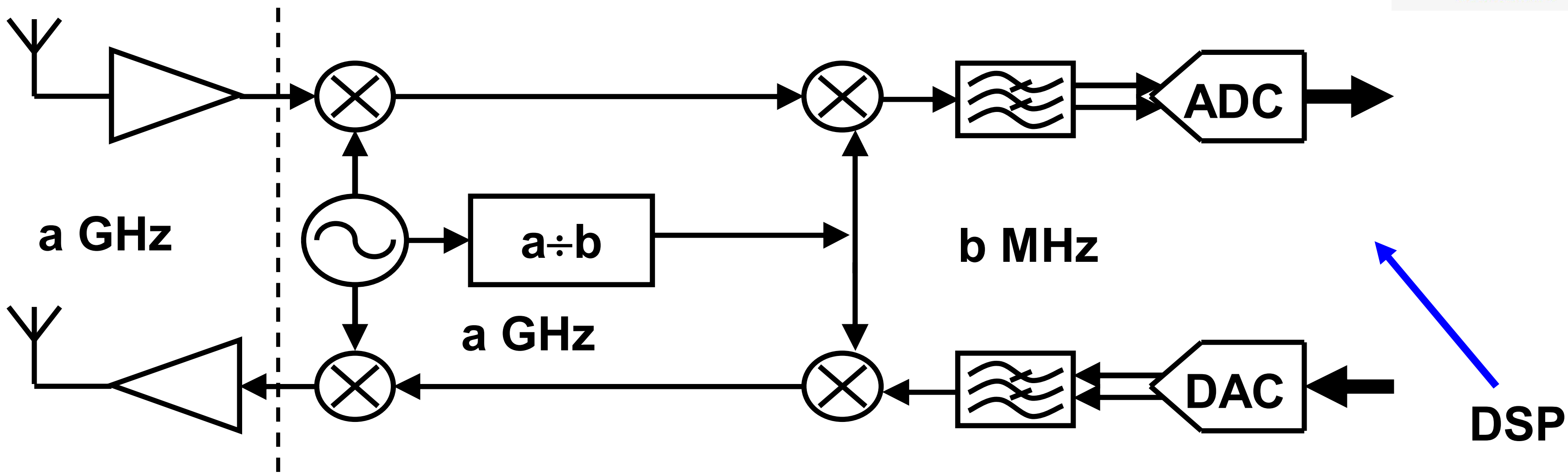
500MS/s → means maximum input signal is half of this about 250MHz

Output clock rate is 500MHz

Some Mixed Signal Applications

✓ Wireless LAN	– 1-100MS/s, 6b-11b
✓ Magnetic storage	– 0.2 – 1GS/s , 6b-8b
✓ xDSL	– 1MS/s – 100MS/s 11b-14b (30 MHz ADC)
✓ Ultrasound	– 40MS/s 8b-12b (20 MHz ADC)
✓ Digital TV	– 20MS/s 8b-10b (base band)
✓ Handy- GSM	– 400MS/s 12b (base band)
✓ CATV decoder	–10-20MS/s 8b-10b (modem ADC)
✓ HDTV	– 50-100MS/s 10b
✓ 1-10GbaseT	– 130MS/s-840MS/s 7b-9b
✓ Videos, Audios…etc.. etc..	

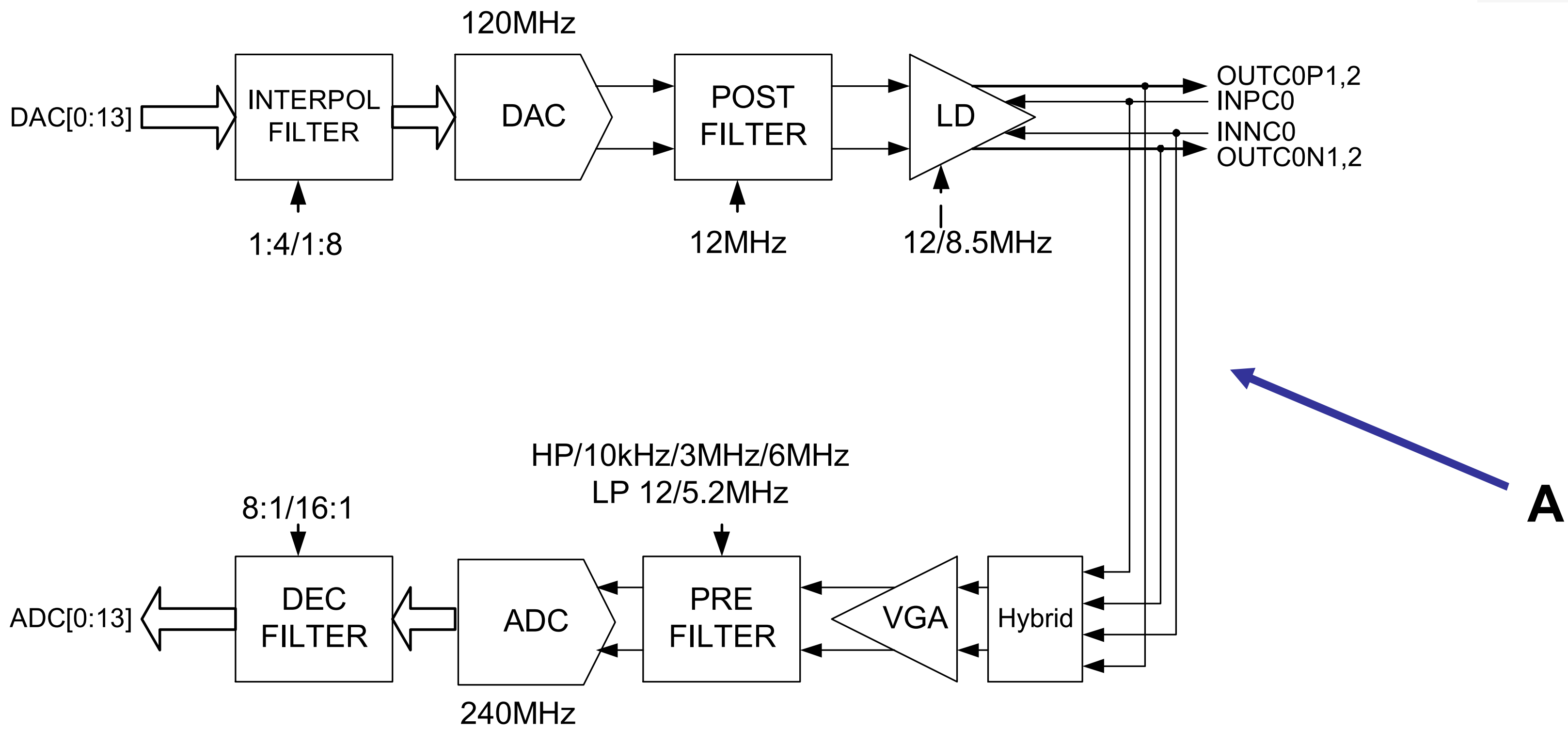
An Example: ADC DAC in Wireless System

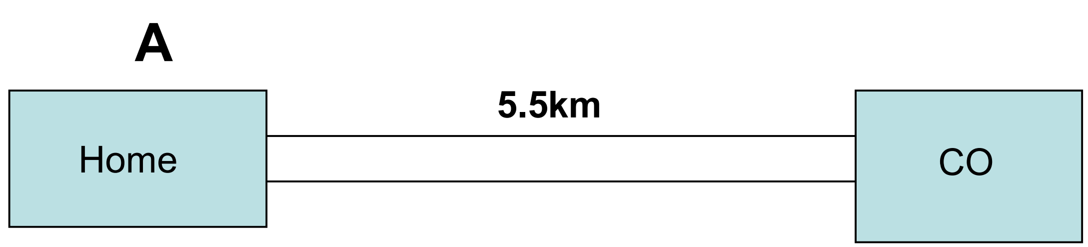


- Antenna length forces high frequency mod.

Old codecs, voice music..
DSL front ends – multi bit , one bit(CDRs)
Wirless   ADCs
Sensing : X ray detection ultrasounds..

An Example: DSL AFE Architecture



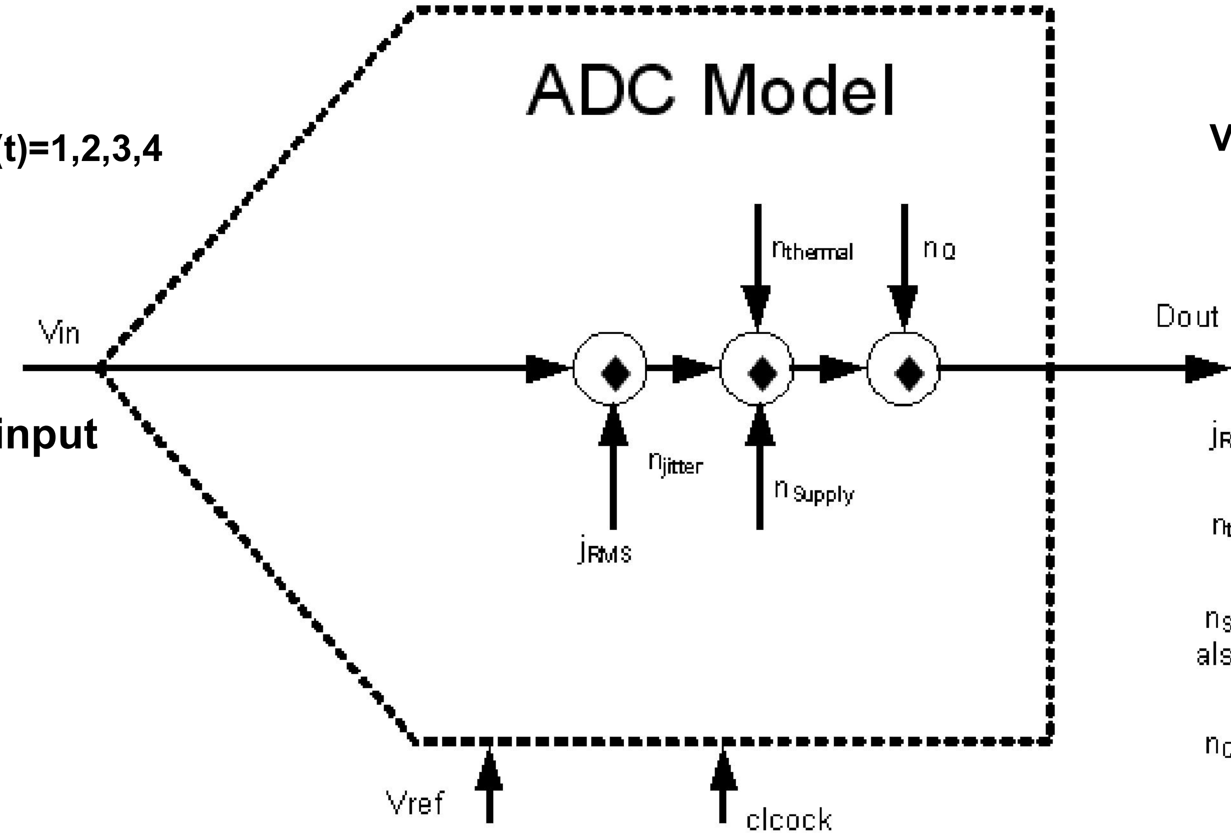


Basics definitions

- Quantization noise (Qn) and Harmonics
  - Qn for Dual Tones
- SNR – Signal to Noise
- DR – Dynamic Range
- Distortions:
  - DNL
  - INL
  - Missing codes
- SNRD – Signal to Noise + Distortions
- ENOBs – Effective Number of Bits
- SFDR – Spurious Frequency Dynamic Range
- Clock Phase Noise – Jitter
- FOM – Figure of Merit

V(t)=1,2,3,4

V (nT)=0001,0100,1100,1000



j_{RMS} = clock jitter (RMS cycle to cycle)

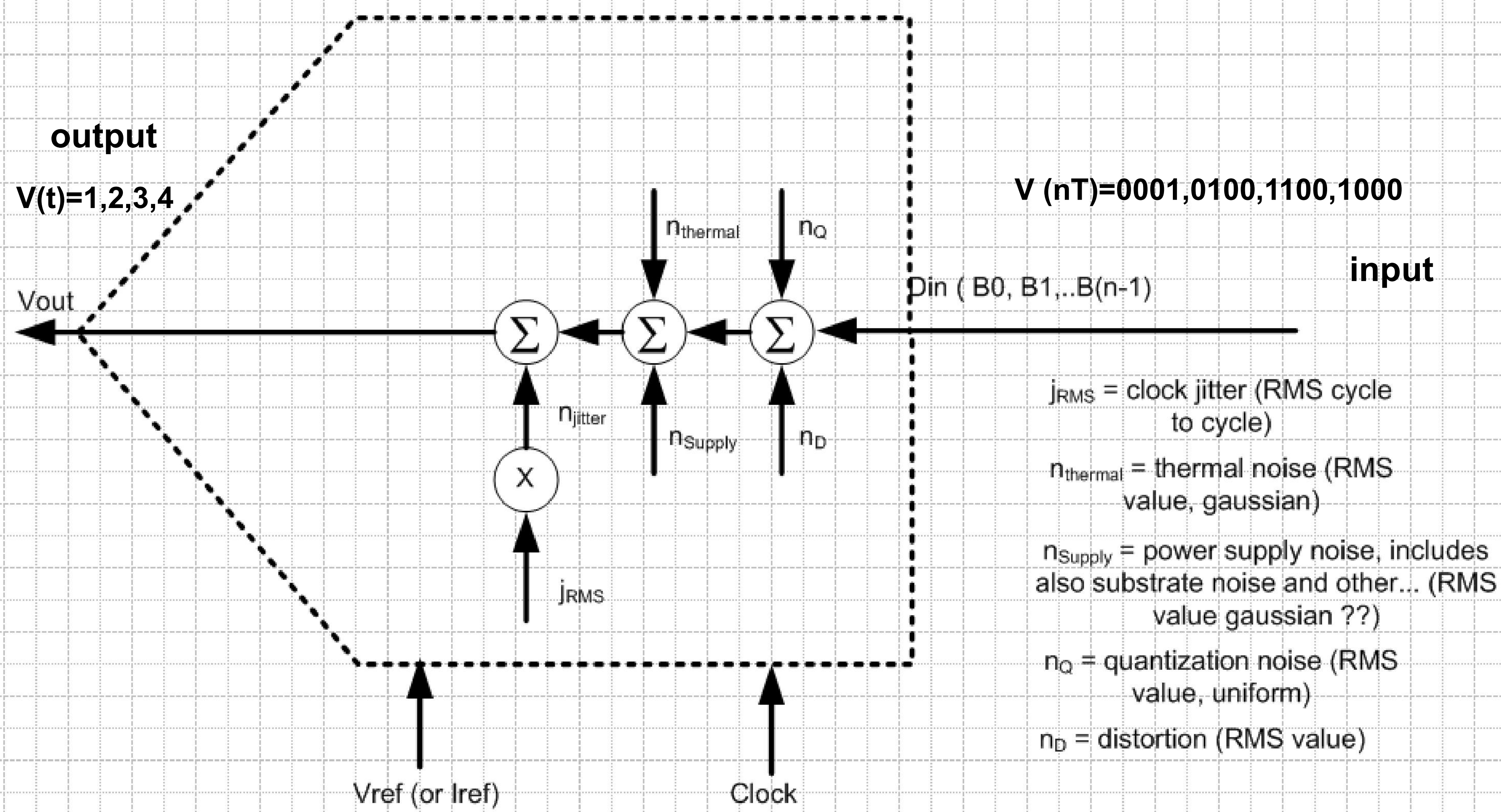
$n_{thermal}$ = thermal noise (RMS value, gaussian)

n_{Supply} = power supply noise, includes also substrate noise and other... (RMS value gaussian ??)

n_Q = quantization noise (RMS value, uniform)

Basic Model

And.. Non linearity


output
V(t)=1,2,3,4
V (nT)=0001,0100,1100,1000
input
Din (B0, B1,..B(n-1)
Vout
Σ
Σ
Σ
X
$n_{thermal}$
n_Q
n_{jitter}
n_{Supply}
n_D
j_{RMS}
Vref (or Iref)
Clock
j_{RMS} = clock jitter (RMS cycle to cycle)
$n_{thermal}$ = thermal noise (RMS value, gaussian)
n_{Supply} = power supply noise, includes also substrate noise and other... (RMS value gaussian ??)
n_Q = quantization noise (RMS value, uniform)
n_D = distortion (RMS value)

Conventional ADC

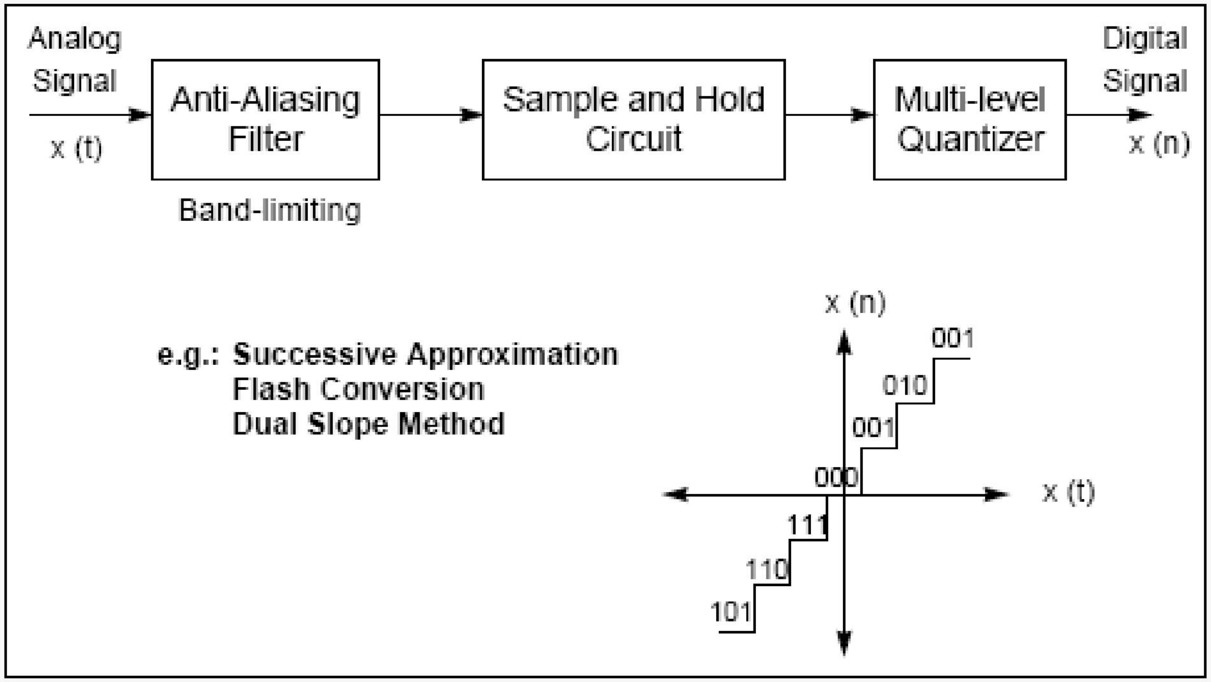
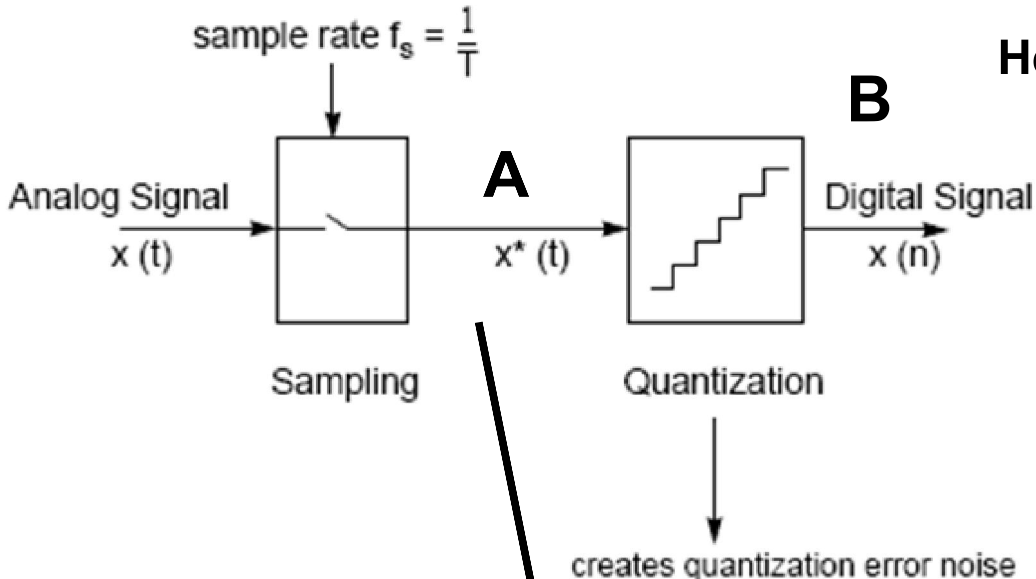


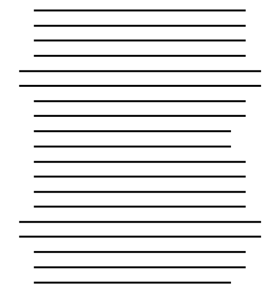
Figure 2-2 *Conventional Analog-to-Digital Conversion Process*

- ADC deals with 2 signals analog inputs and digital outputs.
  - X(t) is continuous time input signal
  - X(n) is discrete time signal. Defined by sampling interval T.

X*(t) is a discrete signal output

Here fixed levels





$$x^*(t) = \sum_{n=-\infty}^{\infty} x(t)\delta(t - nT)$$

Where:

$$\delta(t) = \begin{cases} 1, & t = 0 \\ 0, & elsewhere \end{cases}$$

Math. model

What is the difference at point A and B ? …(Nq)

Sampling- A Step Back At Fourier Transform

Fourier Series

If x(t) periodic $(f_0 = \frac{1}{T_0})$

$$C_x(nf_0) = \frac{1}{T_0}\int_{-\frac{T_0}{2}}^{\frac{T_0}{2}} x(t)e^{-j2\pi nf_0 t}\,dt$$

x(t) can be written as:

$$\sum_{n=-\infty}^{\infty} C_x(nf_0)\, e^{j2\pi nf_0 t} \quad -\infty < t < \infty$$

$$=A_0 + \sum_{n=1}^{\infty} A_n cos2\pi nf_0 t + \sum_{n=1}^{\infty} B_n sin2\pi nf_0 t$$

$$C_x(nf_0) = A_n - jB_n$$

Any periodic signal can be constructed from sum of Sin waves.

The power (or PSD) density is:

$$S_x = \int_{-\infty}^{\infty} |C_x(nf_0|^2 \delta(f - f_0)\,df \quad = \text{Power}$$

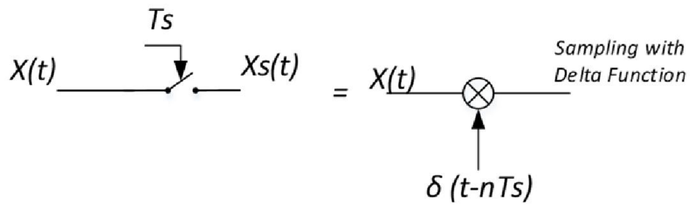
Any periodic signal can be constructed from sum of Sin waves.

The power (or PSD) density is:

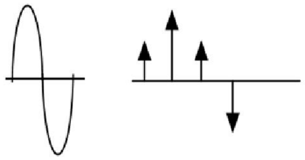
$$S_x = \int_{-\infty}^{\infty} \underbrace{|C_x(nf_0|^2 \delta(f - f_0)}_{G_x(p)} \, df \quad = \text{Power}$$

Also the power in t domain

$$\frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} (x^2(t))^2 \, dt$$



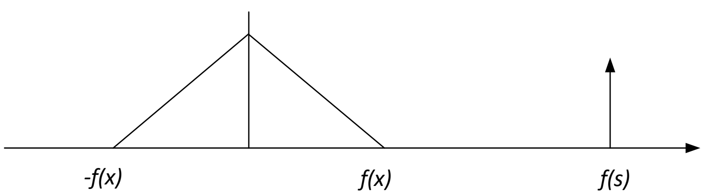
POINT A !

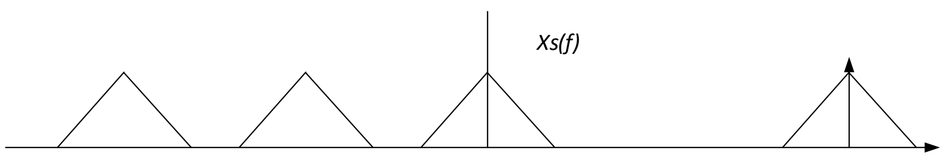


$$X_s(t) = X(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nTs), \qquad \int_{-\infty}^{\infty} \delta(t)dt = 1$$

Also, since δ(t)=0 everywhere, except at t=0

$$X_s(t) = X(t) \cdot \sum_{n=-\infty}^{\infty} X(nTs)\delta(t - nTs)$$





F[•] » Defined as Fourier operation

$$F[X_s(t)] = X_s(f) = X(f) * F\left[\sum_{n=-\infty}^{\infty} \delta(t - nTs)\right]$$

Need to be prove

$$f(s) \cdot \sum_{n=-\infty}^{\infty} \delta(f - nfs)$$

$$X_s(f) = f_s \cdot \sum_{n=-\infty}^{\infty} X(f - nfs)$$

$$f_sX(f) + f_sX(f - f_s) + f_sX(f - 2f_s) + f_sX(f - 3f_s) + \cdots$$

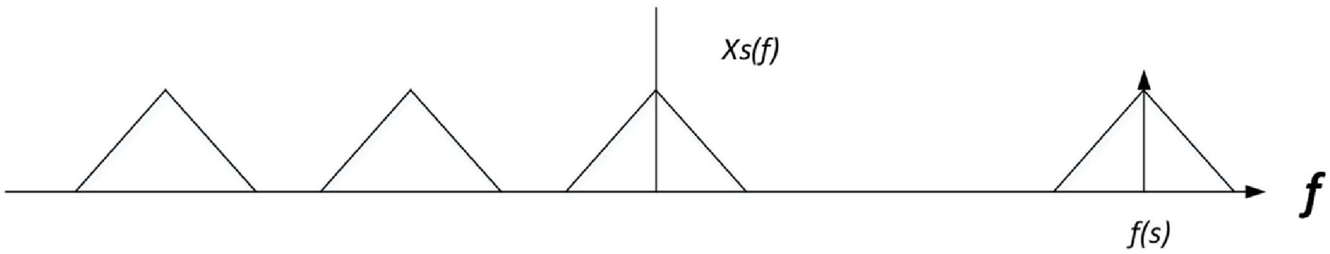
$$f_sX(f + f_s) + f_sX(f + 2f_s) + f_sX(f + 3f_s) + \cdots$$

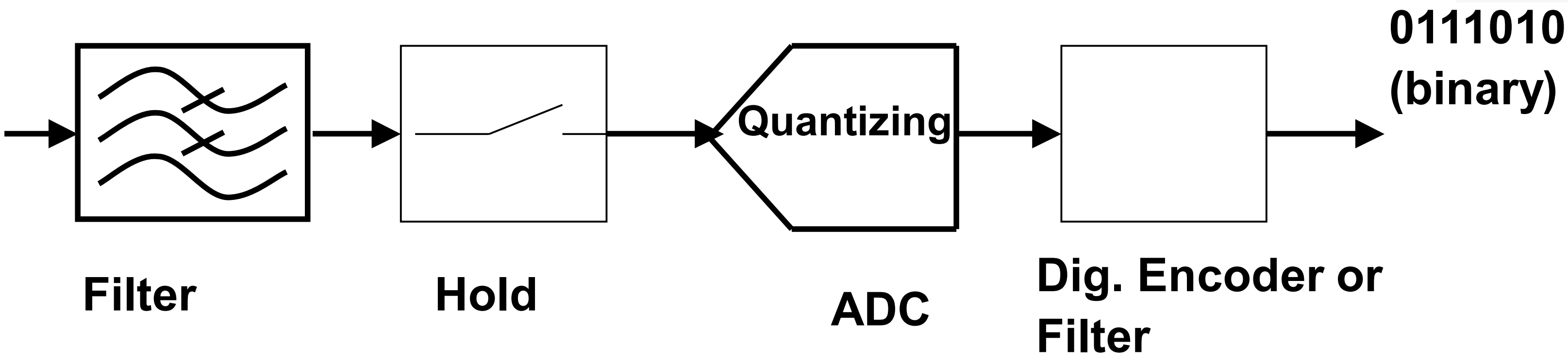
The Shannon Theorem says:
"If a signal x(t) has a Limited Bandwidth (-BW, BW), it can be univocally determined by its samples x(nT) if the Sampling Frequency is at least twice the Bandwidth:

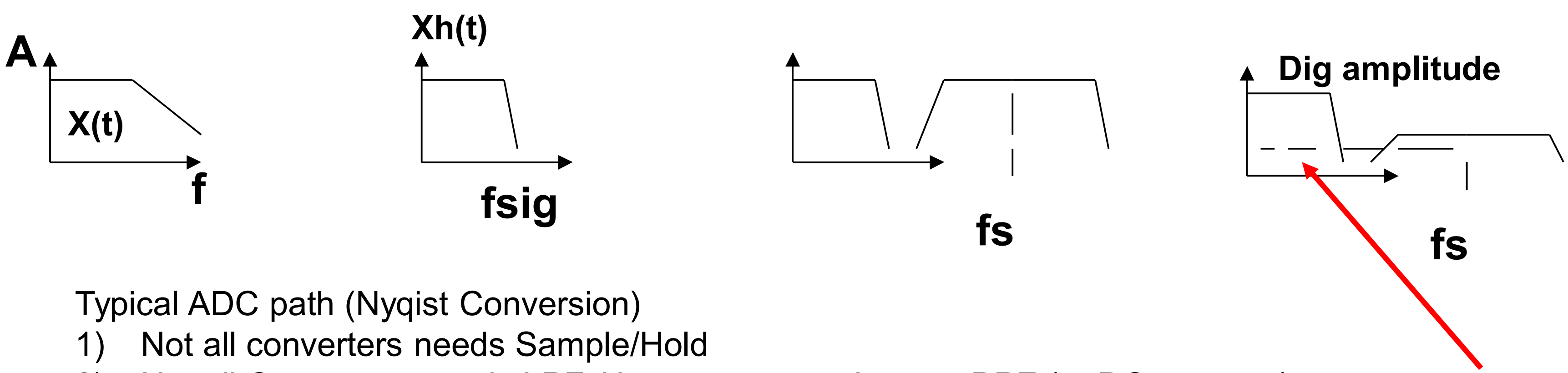
$$f_s = \frac{1}{T} \geq 2BW$$

Shannon
1949

Note:
- Limited Bandwidth is a Necessary but not Sufficient condition
- 1/T ≥ 2BW is only a Sufficient but not Necessary condition







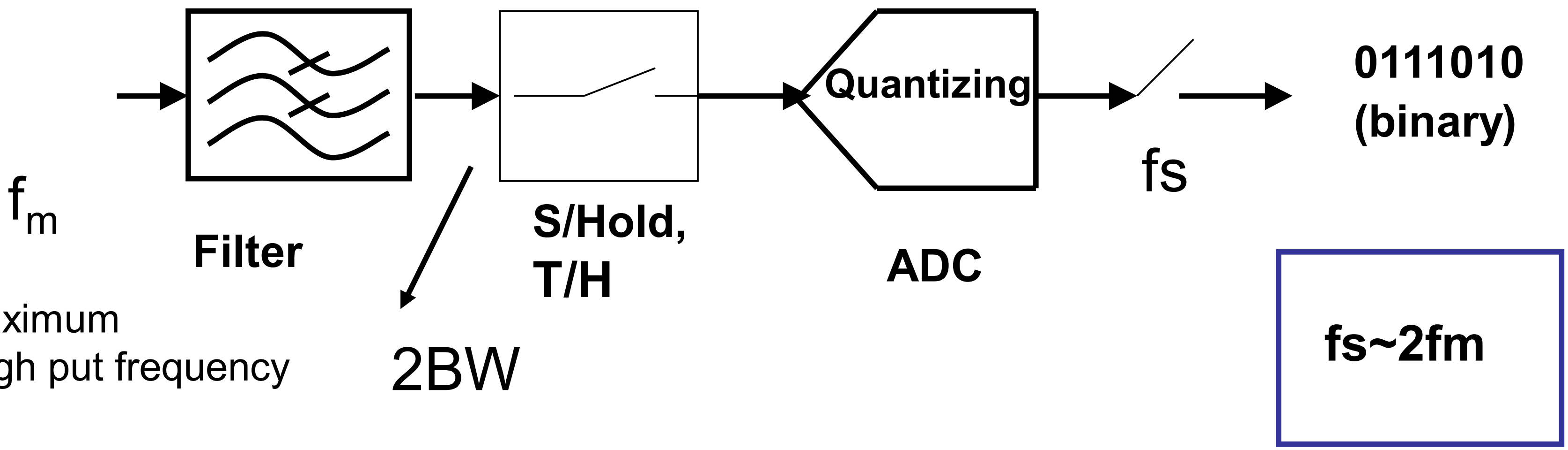
Typical ADC path (Nyqist Conversion)

1) Not all converters needs Sample/Hold
2) Not all Converters needs LPF, However some also use BPF (or DC remover)
3) F_{signal} coming to the converter is Bounded.
4) ADC output may or may not have reduced folding – but it has noise

Noise: random
systematic, lin

KEY: How each component works, its transfer function, what is the optimum ?
first to the definitions ! (lect. 2)

CLASS OF CONVERTERS



f_m=maximum
Through put frequency

Nyquist converter: max speed lowest clock

2fm(2xBW) < fs **2fm very close to fs.**

Nyquist
1928

Remember:

S&H not always needed

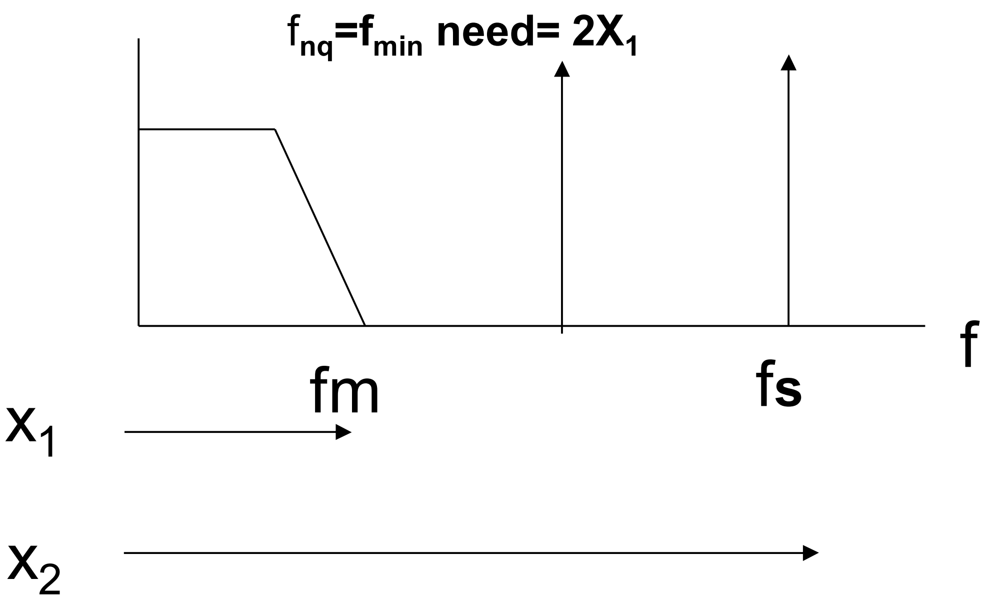
LPF: Not always needed

Over sample converter:

max speed lowest clock 2fm < fs

$x_2 >> 2x_1$

fs>>2fm



Lecture 7,8,9

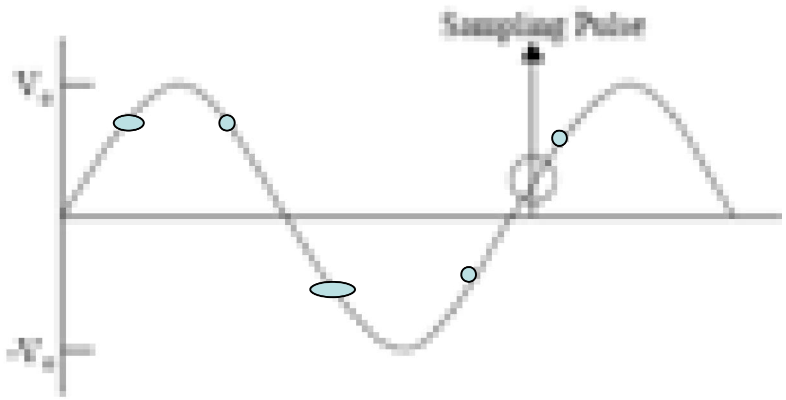
2fm <u>much lower → fs</u>.

We sample many time over (16x..1024x..)

And…Under sampling Converter

Exception to the rule ?

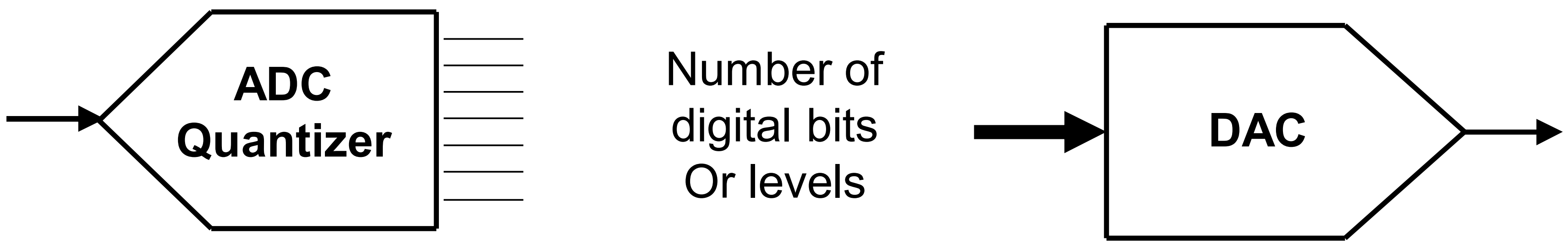
- But… when is Nq random, sampling at exact points..



- Sample of rate not repeated close to signal frequency or Nq. will not have enough information..

- ✓ Resolution
- ✓ Quantization Noise (Qn) and Harmonics
- ✓ Qn for Dual tones
- ✓ SNR
- ✓ Distortion:
    - ✓ Missing Codes
    - ✓ INL/DNL
- ✓ ENOBs and SFDR Definitions
- ✓ Clock Jitter
- ✓ Thermal and 1/f Noise
- ✓ Supply Noise and Substrate Noise
- ✓ Mismatches

- It's the measure of number of digital bit at the output of the converter (ADC).



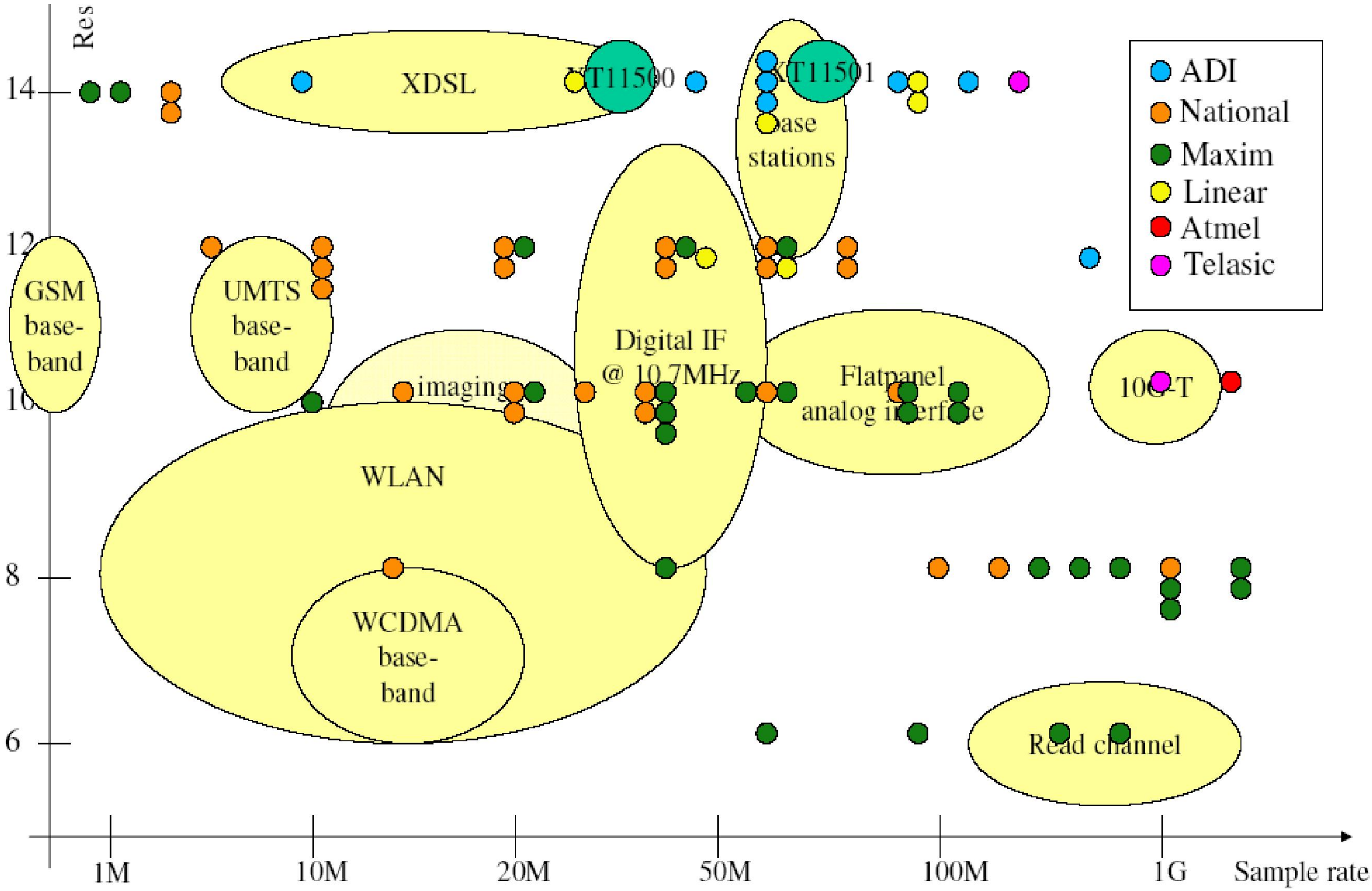
- Its not an indication of the quality of the converter (bits may or may not move).

  - The number of bits of the digital code is finite, namely n.

For n bit we have 2^n Possible levels
and 2^n-1 Possible steps

Application Data Rate and Resolution/Rate

Resolutions



Rate

Quantization Noise

- The number of bits of the digital code is finite, namely n.
- For n bit we have 2^n possible codes each code represent a given ***Quantization Level***.
- The error due to the Quantization is called the ***Quantization Error*** and ranges between $\pm$ half Quantization Level (LSB).

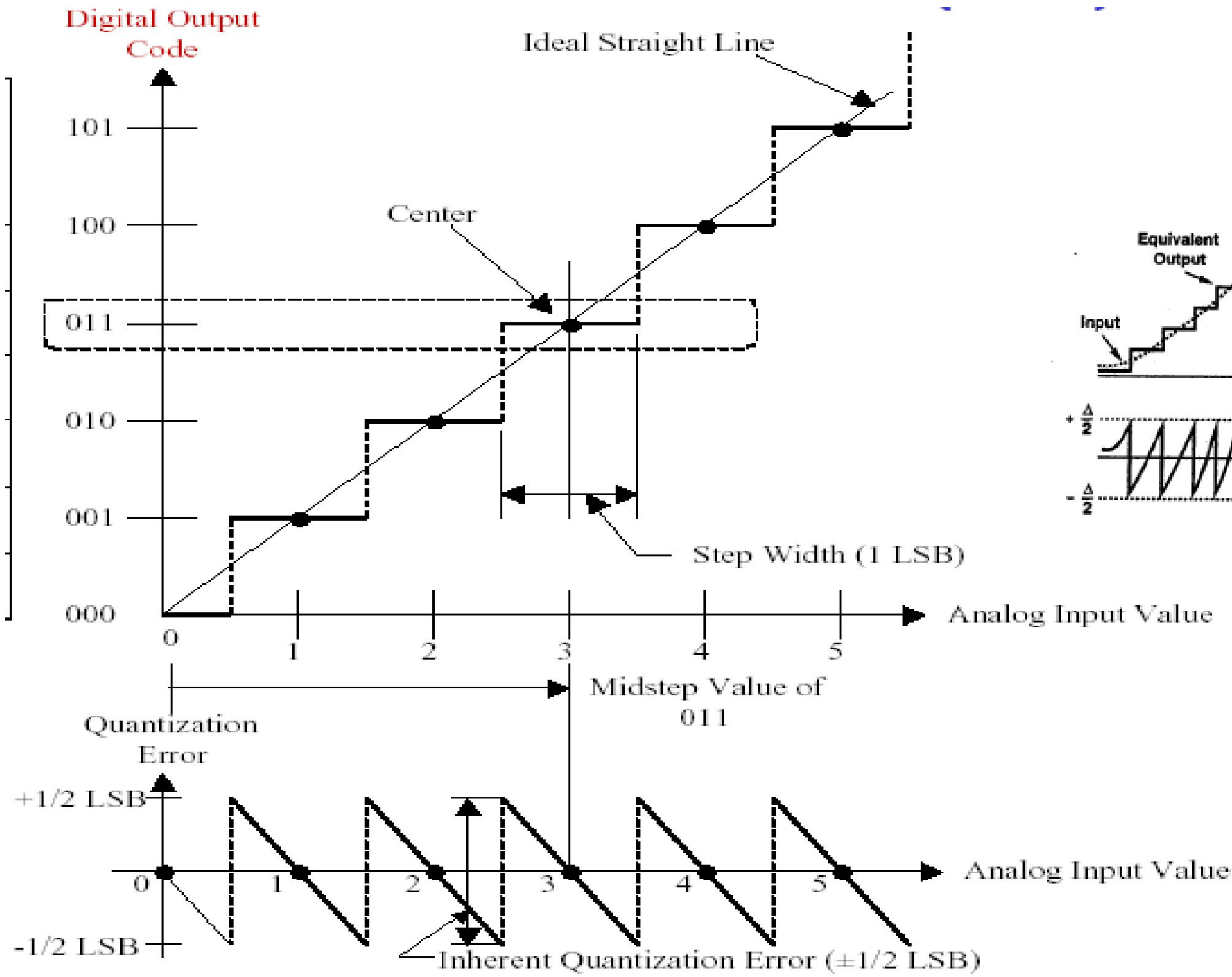
- This error is a consequence and a measure of the finite ADC resolution.

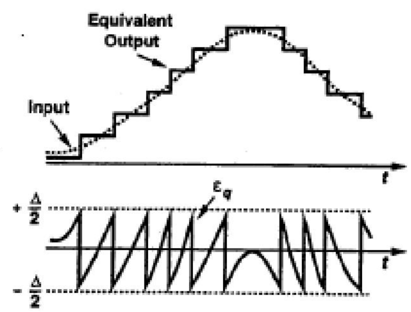
Possible Codes = 2^n

- ***Digital bits are limited: 9, 10, 16 etc..***
- ***Therefore can't represent the input signal perfectly: error***

- Quantization LSB error can't be higher then the resolution vice versa is possible

Quantization Noise





- ***Input minus output after gain and offset errors are nulled***

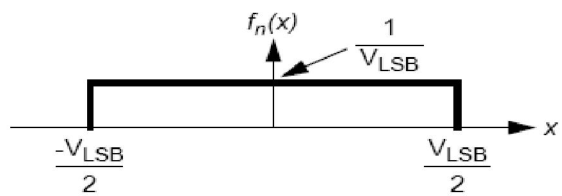
- *Assuming the input signal has uniform density function over each code bin then quantization noise is well approximated by uniform distribution and white spectrum*

Quantization Noise Power

— **deterministic approach (assume input is a ramp)**

— **stochastic approach (assume rapidly varying input)**

probability density function



$$\int_{-\infty}^{\infty} f_n(x)\,dx = 1$$

rms value of quantization noise is (noise has zero-mean):

$$V_{n(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_n(x)\,dx\right]^{1/2} = \left[\frac{1}{V_{LSB}}\int_{-\frac{V_{LSB}}{2}}^{\frac{V_{LSB}}{2}} x^2\,dx\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

quantization noise power is:

$$\frac{(V_{LSB})^2}{12}$$

- **this noise power is spread between -$f_s/2$ and $f_s/2$**

$$Nq = \frac{V_{LSB}}{\sqrt{12}}$$

$$V_{n(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_n(x)\,dx\right]^{1/2} = \left[\frac{1}{V_{LSB}}\int_{-\frac{V_{LSB}}{2}}^{\frac{V_{LSB}}{2}} x^2\,dx\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

approximately 1/3 of an LSB !

Quantization Noise Calculation – Cont. (in terms of full scale)

- *Full scale voltage is the parameter we're interested in.*
- *To maximize or distribute all the available codes we split the full scale (V_{pk}) to all the possible codes.*

$$V_{fs} = V_{LSB} \cdot 2^n - 1$$

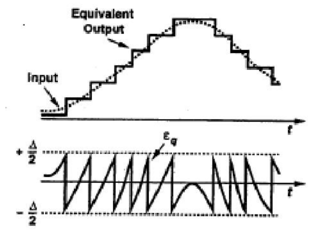
Substitute into the quantization noise Eq.

$$Nq = \frac{V_{LSB}}{\sqrt{12}}$$

Quantization Noise

$$n_Q^2 = \frac{VFS^2}{12 \cdot 2^{2 \cdot Nbit} - 1}$$

- ***A Sine wave for example at the end point (slowly moving input) may not be uniform enough over the code bin.***



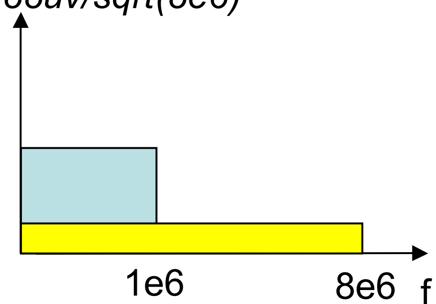
Quantization Noise Density – An Example

How far does it spread and how does it depend on frequency?

The quantization noise spreads to the half of the clock frequency. (+/- fs/2)
That is to say we can define quantization noise per root hertz. And now get the Total noise for a fixed BW that we operate in. (a must for non nyquist converters)

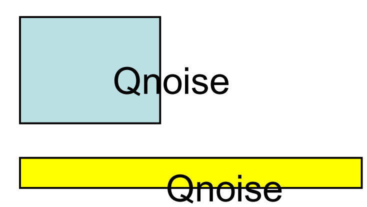
*Example*1 :
a) If LSB is 1 mV and we sample at 2 MHz: 288uV is spread over 1 MHz. which means 0.288uV/sqrtHz--→ 288uV/sqrt(1e6) (Qnoise)

b) If we sample at 16 MHz the quantization noise density is : 0.101 uV/sqrHz→288uv/sqrt(8e6)



Conclusion
Good to increase the sampling clock we profit: (in density)
Is we define 10 log (fs/ fsignal BW) we gain = 3dB/octave !

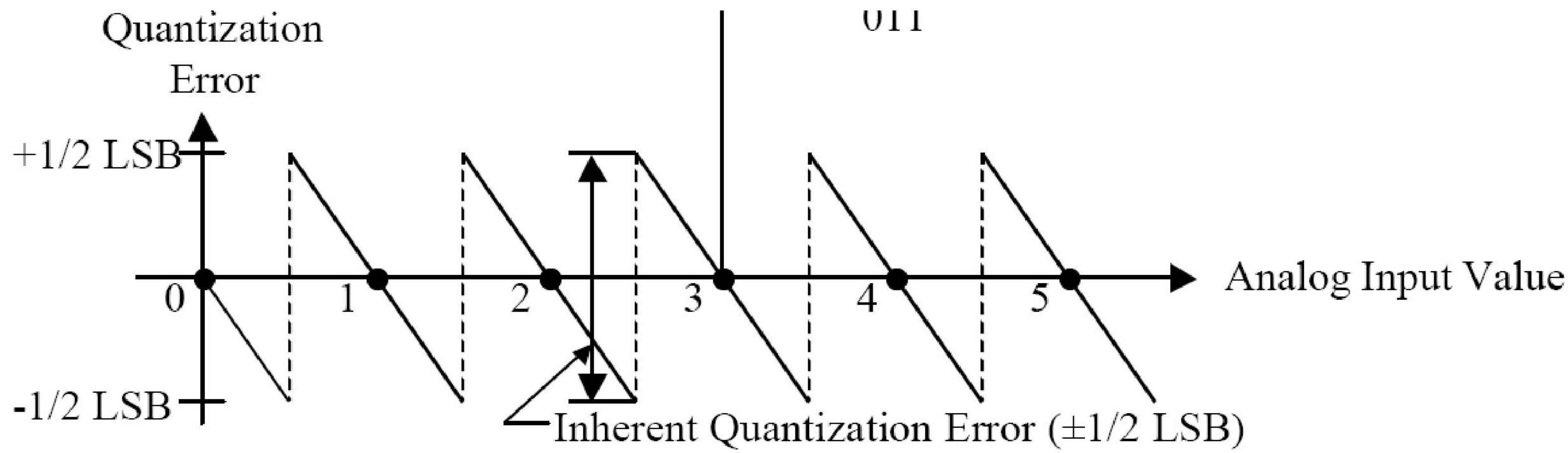
Example2 lets say we only look at 1MHz band (we have magic filter)
10 bit ADC with BW=1MHz and 2MHz sampler quantization noise is: ~288uV (1volt)
10 bit ADC with BW=1MHz and 16MHz sampler quantization noise is: ~288uV/2.82



10log8

Can quantization produce non linear output signal? – Yes.- in advance notes

We measure its Harmonics ? Non linearity's ?



Elements of Transfer Diagram for an Ideal Linear ADC

SNR

SNR Definition

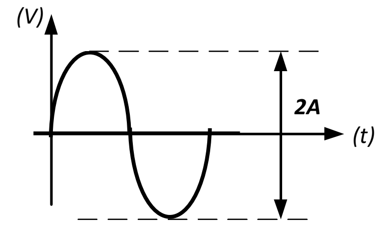
- *In telecommunication the output quality is measured in term of Signal to Noise Ratio (SNR)*

- *Definition: SNR is defined as the ratio of output signal, so power to the base band noise power at the output No. Including Quantization, Harmonics (sometime not), and all Flicker Thermal Jitter noises.*

$$SNR = 20log\frac{V_{in(rms)}}{V_{q(rms)}}$$

- ***What are the units ?***

SINE Wave – SNR due to Quantization



$$Sin\ Wave, \qquad V_{in} = A \sin \omega t$$

Signal Power = Mean Square Root

$$v_{in}^2 = \frac{1}{2\pi}\int_0^{2\pi} A^2 \sin(\omega t)^2 dt = \frac{A^2}{2}$$

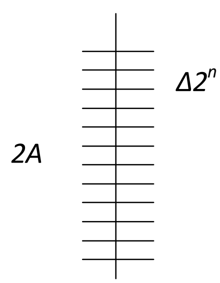
out

How is A related to LSB? Δ

Δ = LSB

$$N_q^2 = \frac{\Delta^2}{12}$$

$$\Delta = \frac{2A}{2^n - 1}$$



SINE Wave – SNR due to Quantization cont.

$$SNR = 10log\frac{A^2/2}{A^2/12} = \frac{A^2 \cdot 12 \cdot 2^{2n}}{2(2A)^2}$$

$$= \frac{12}{8} \cdot (2^n)^2$$

$$20log2^n + 10log(3/2)$$

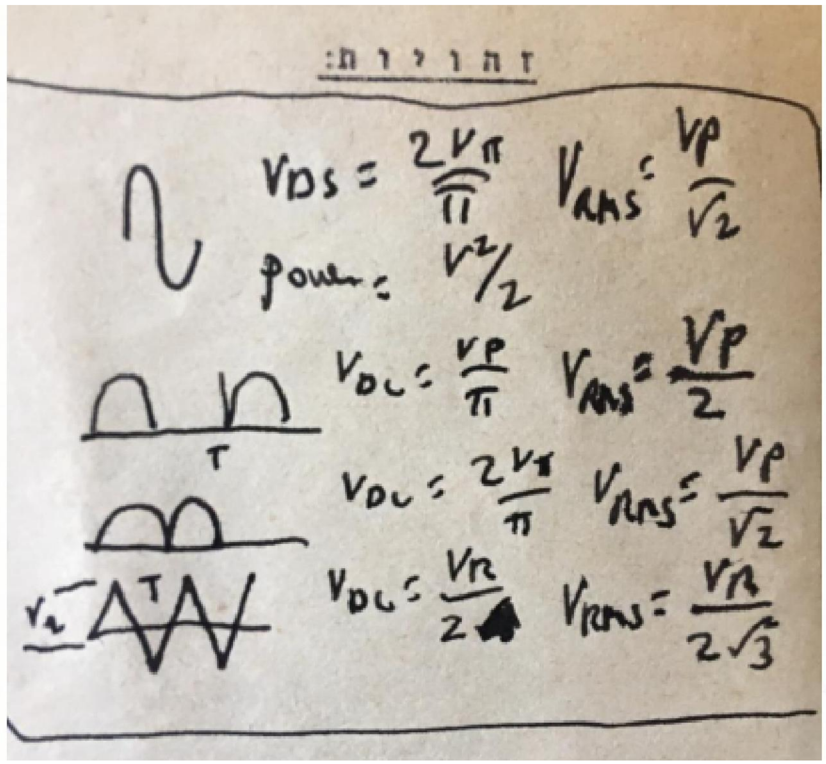
$$SNR = [6.02 \cdot n + 1.76]dB$$

From Bits — From 3/2

❑ *Key: The noise is spread: to +/- fs/2*

Remember:

- ❑ ***But it is not exact for 1-4 bit there is some deviation (1bit: 6.31dB instead of 7.78 dB)***
- ❑ ***Above 4 bits the error is in the second digit point of the SNR***


זהירות:
VDS = 2Vπ/π
VRMS = Vp/√2
power = V²/2
VDC = Vp/π
VRMS = Vp/2
VDC = 2Vπ/π
VRMS = Vp/√2
VDC = VR/2
VRMS = VR/2√3

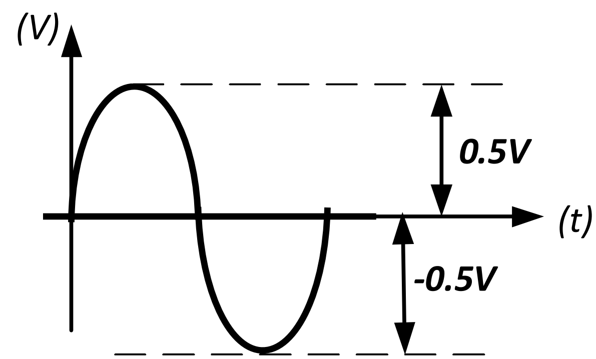
An Example

Example:
100mV sine wave is applied to an Ideal 12b converter which has its maximum range at 1V.
Find the SNR of the digitized output, plot it *(remember n = converter number of bits)*

$$LSB = \frac{1}{2^{12}-1}$$

$$SNR = [6.02 \cdot n + 1.76] = 74dB$$

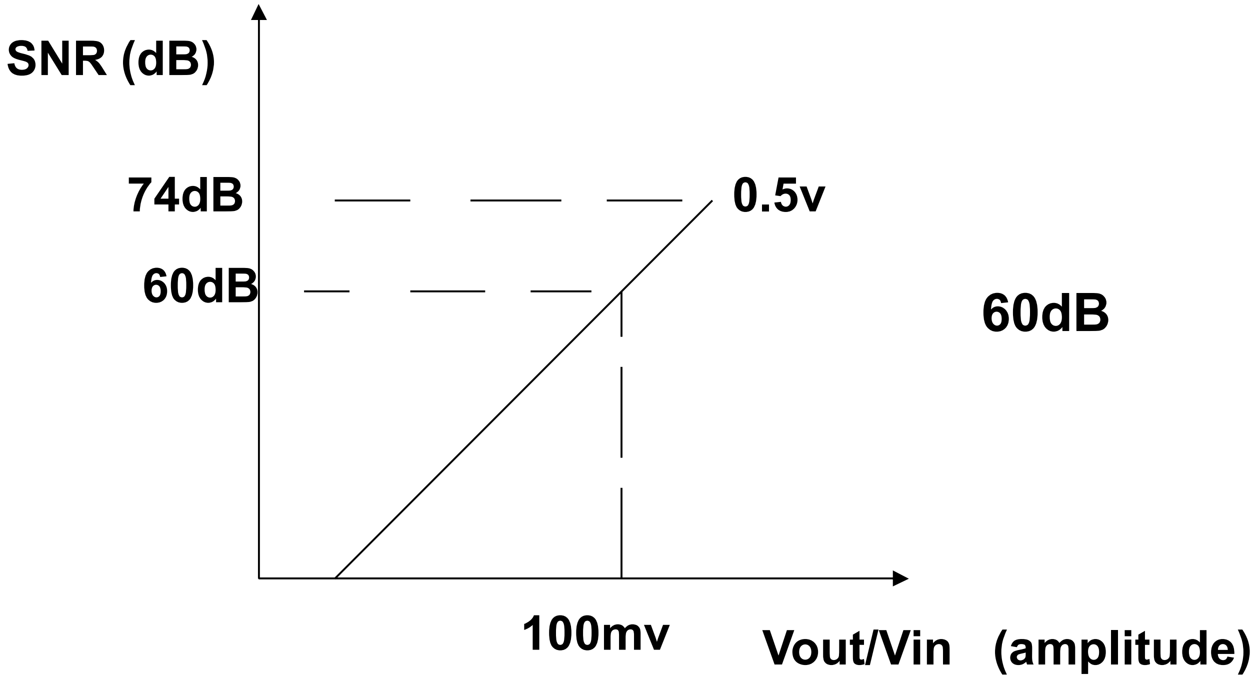
$$SNR = 10log \frac{\left(\frac{0.1}{2}\right)^2 12}{\frac{1}{2^{12 \cdot 2}}} = 60dB \Rightarrow 10log \frac{A^2/2}{A^2/12}$$



OR:
100mV is 14dB below 0.5V (20log5)

= 74 – 14= 60dB

An Example cont.

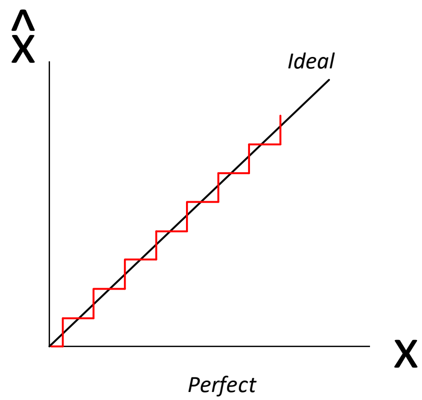


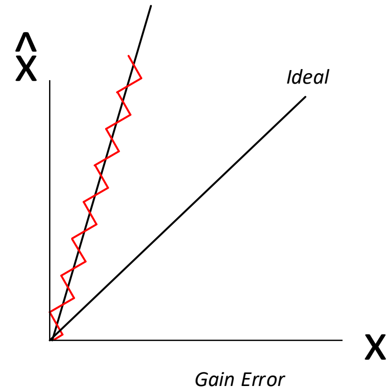
Some input are not sine waves but a which have much higher signal peak to RMS value. complex waveform QAM
In that case SNRpk represent the peak value to the RMS noise..

DISTORTIONS IN CONVERTERS

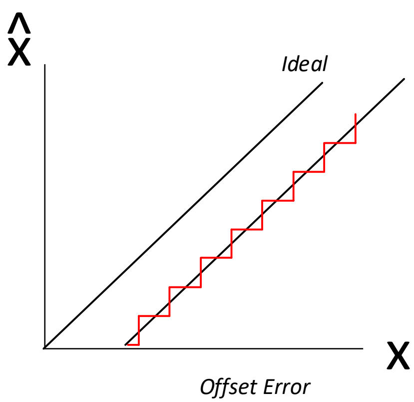
Some of Errors Graphically

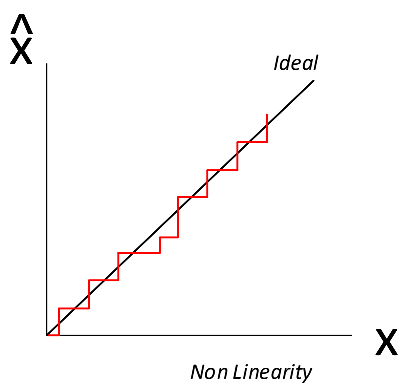
Errors in Converter





Trim V_{ref} or Code α

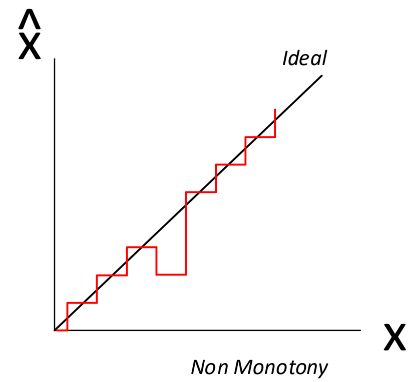


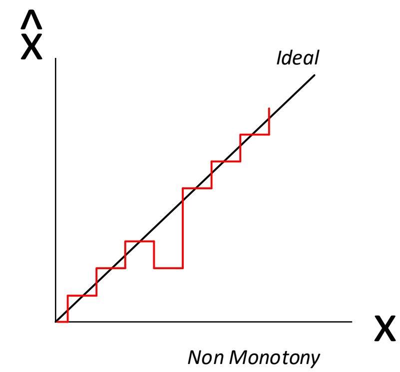


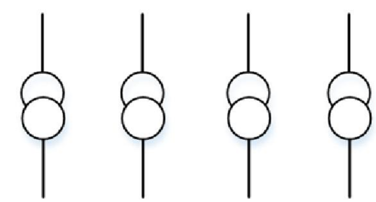
For ADC X Produces Code $\hat{X}$

For ADC $\hat{X}$ Produces Code X

Extreme Linearity Errors







$8I_{x4}$	$4I_{x3}$	$2I_{x2}$	I_{x1}
0	*1*	*1*	*1 = 7I*
1	*0*	*0*	*0 = 8I*

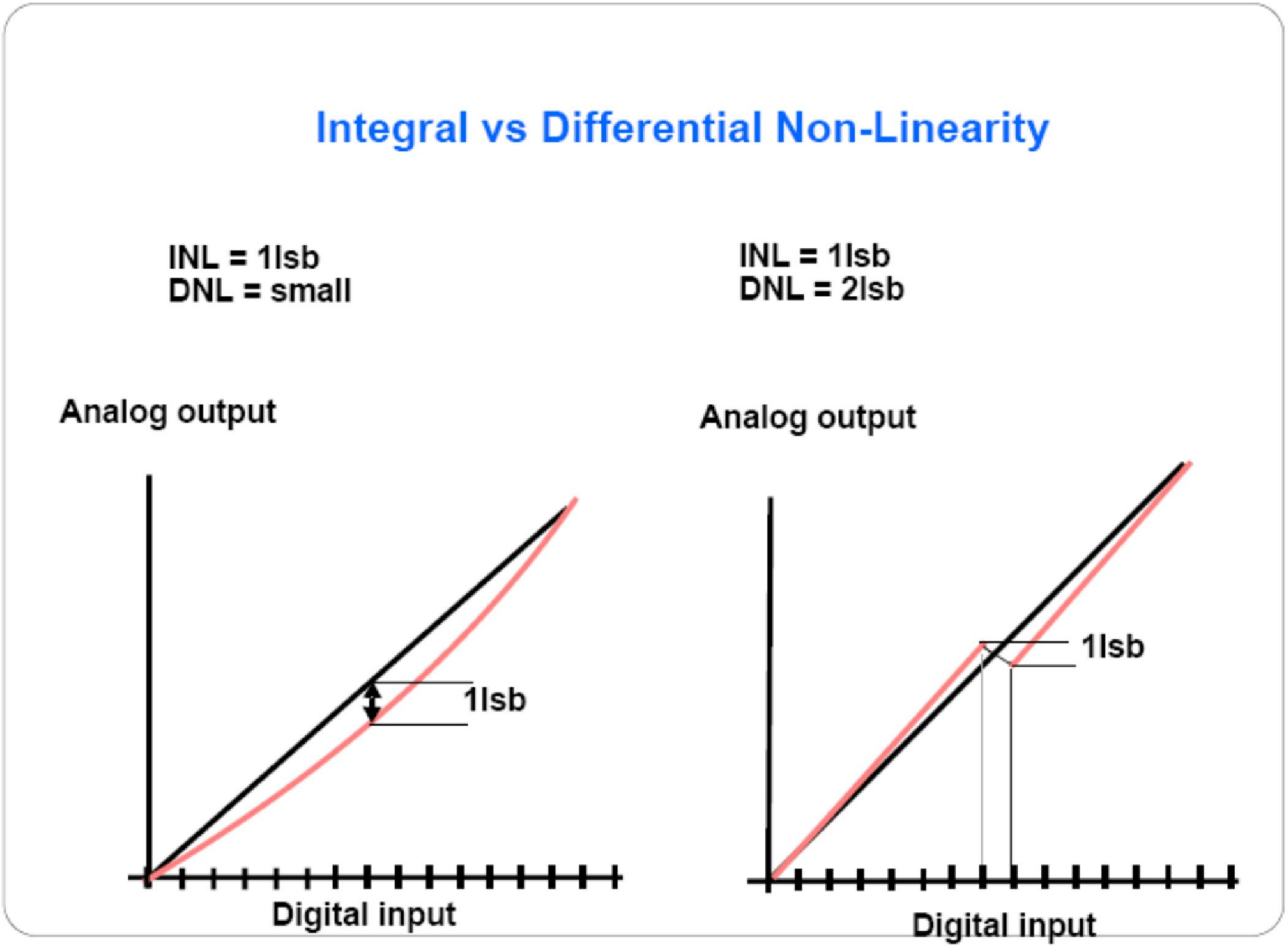
8I does not use the current elements from the 7I sections therefore the 8I can be lower or higher and become a missing codes

Methods

- Fourier transform of the output points
- Evaluate with Numerical Polynomial of the data point
- Evaluate the INL (and DNL) – make sensible decision.

Results

- Most accurate
- Accurate but tedious (need to look at the errors
- Very quick feeling on what's going on (worse case only)



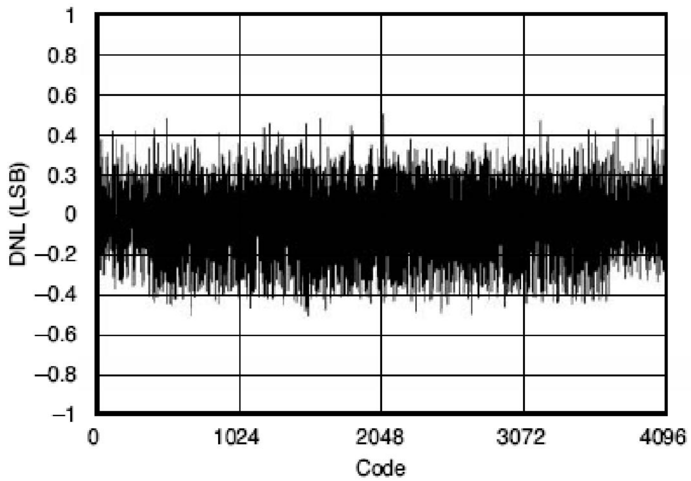
<1 LSB DNL does not implies less than 1 LSB INL

DNL Definition

- ❑ **Differences between two adjacent output digital or analog compared to a step size of LSB weight.**

Mathematically Definition of DNL

$$DNL_i \triangleq \frac{V_{i+1} - V_i}{VLSB} - 1 = INL_{i+1} - INL_i$$



INL – DACs and ADCs Errors (systematic)

Distortion:
Missing Codes, (INL/DNL)

INL Definition

- **The Deviation of output code or output signal from straight line drawn from 0 and full scale**

Once Gain and Offset are corrected is called Integral Non Linearity (INL)
INL leads to Harmonic distortions !

Monotonic:

- The output never decreases with increase of code or signal if INL<1 LSB the converter is monotonic - no missing codes.

Mathematically Definition of DNL

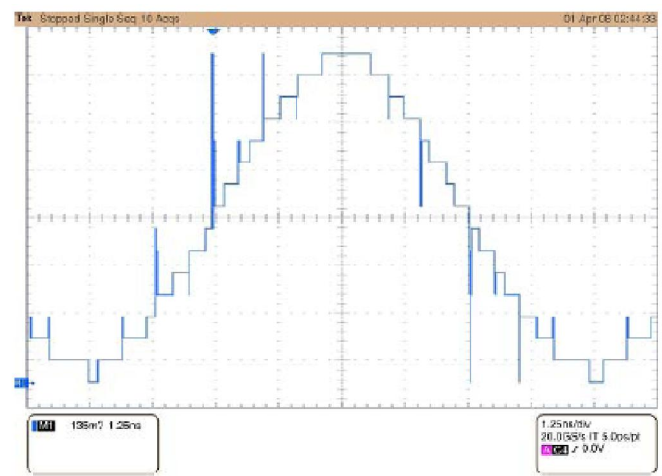
$$INL_i \triangleq \frac{V_i - V_{off}}{VLSB} - i + \frac{1}{2}$$

INL is measure of worst case distortion

However,
We do not know how and were the DNL/INL is corrupted therefore only FFT is accurate.

INL is a close call indication of linearity (THD) (remember should we extent the INL/DNL to AC)?

<1 LSB INL implies less than 1 LSB DNL
<1 LSB DNL does not implies less than 1 LSB INL



INL Related to DNL – YIELD

The Relationship Between the 2:

$$INL_i = \sum_{k=-N_{out\,Max}}^{i-1} DNL_k$$

$$DNL_i \triangleq \frac{V_{i+1} - V_i}{VLSB} - 1 = INL_{i+1} - INL_i$$

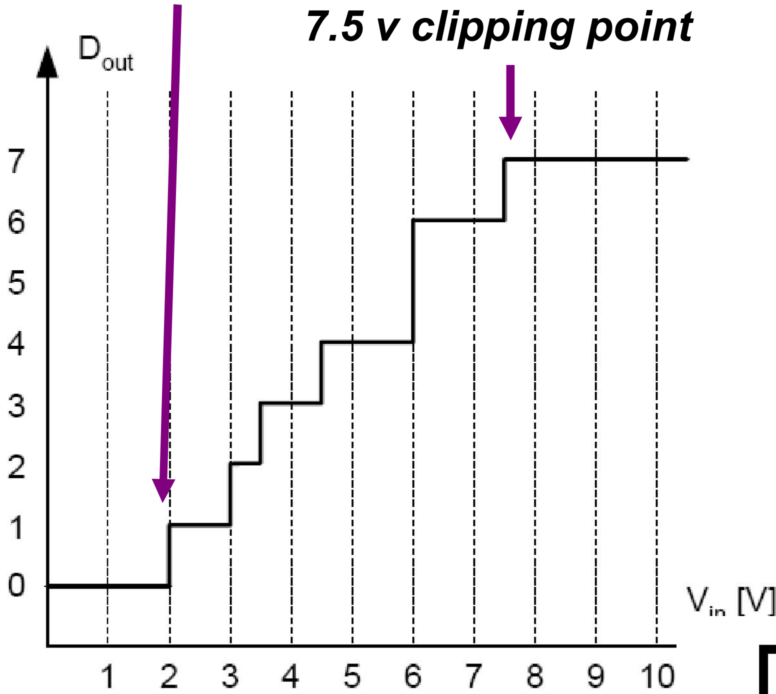
If INL/DNL are not linear/equal, due to elements in the analog blocks, they are systematic, we made a mistake either in the design or mismatch in silicon (resistors/current source)

→ YIELD IS EFFECTED – calculate it

INL/DNL- in class example

2v min point point

7.5 v clipping point



Delta=0.91v

0	undefined
1	1
2	0.5
3	1
4	1.5
5	0
6	1.5
7	undefined

We have 6 steps and 7.5 v clipping point

Use example from (Source: B.Murmann Stanford)

Code (k)	DNL [LSB]	INL (LSB
1	0.09	0
2	-0.45	0.09
3	0.09	-0.36
4	0.64	-0.27
5	-1.00	0.36
6	0.64	-0.64
7	undefined	0

SNRD= signal / Total Noise can now be defined:
SNR + SND + all noises (jitter)..etc..

ENOBs

Definition of ENOBs

Linearity test:

- ***With a Line set by end points (on occasion is best fit) - DC measure – can we extend to AC?***
- ***FFT the output – will tell it all.***

ENOB is the Effective Number of Bits

$$ENOBs(bit) \equiv \frac{SNDR\ (effective) - 1.76}{6.02}$$

SNDR is the measured value

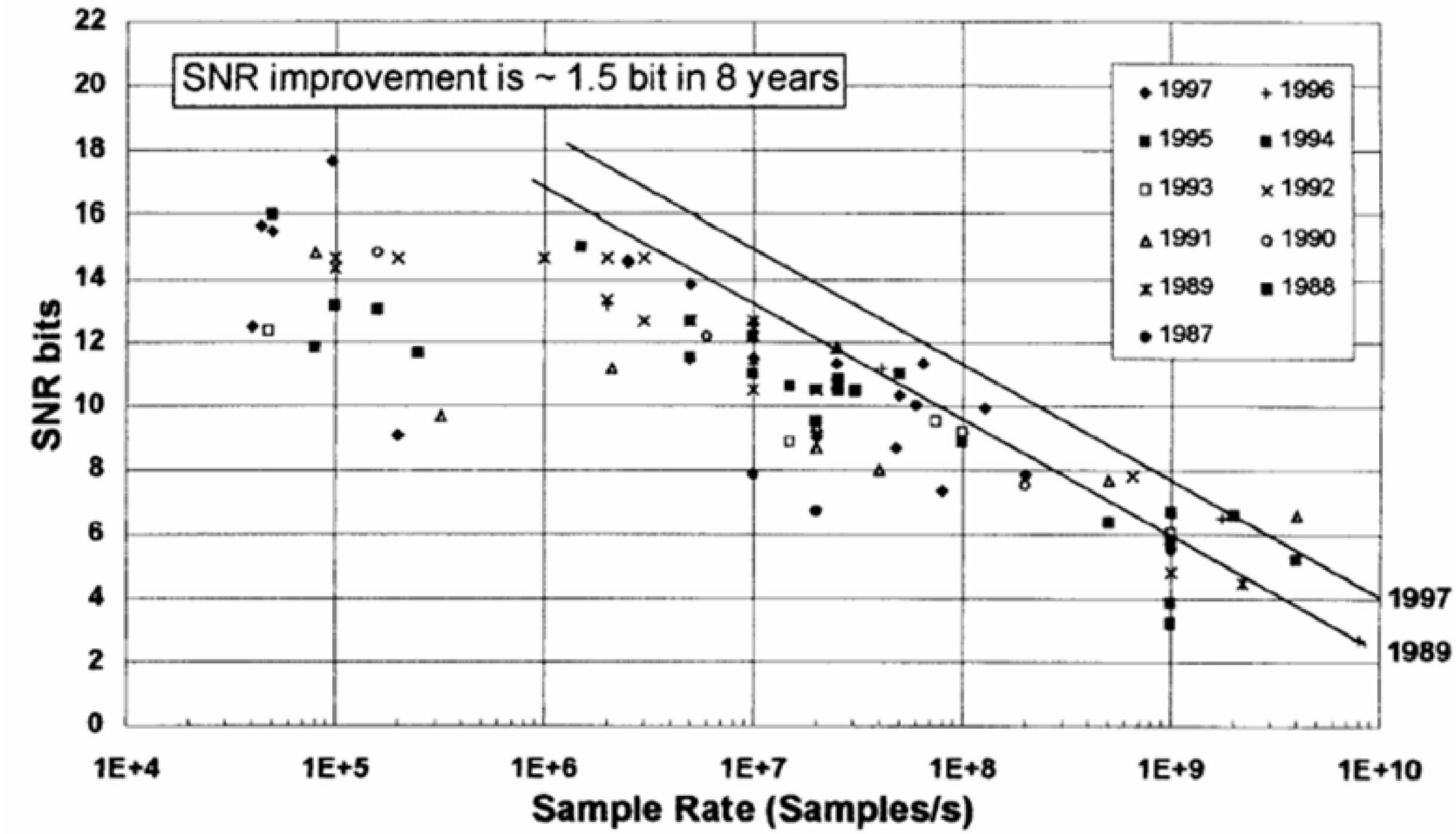
SNDR is measure of effective resolution ("real" of the converter)

++Thermal Noises..

N- Quantization
D- Harmonics

$$ENOB = \frac{S}{N + N_{INL}} = \frac{S}{N} \cdot \frac{N}{N + N_{INL}}$$

ENOBs Improvements..

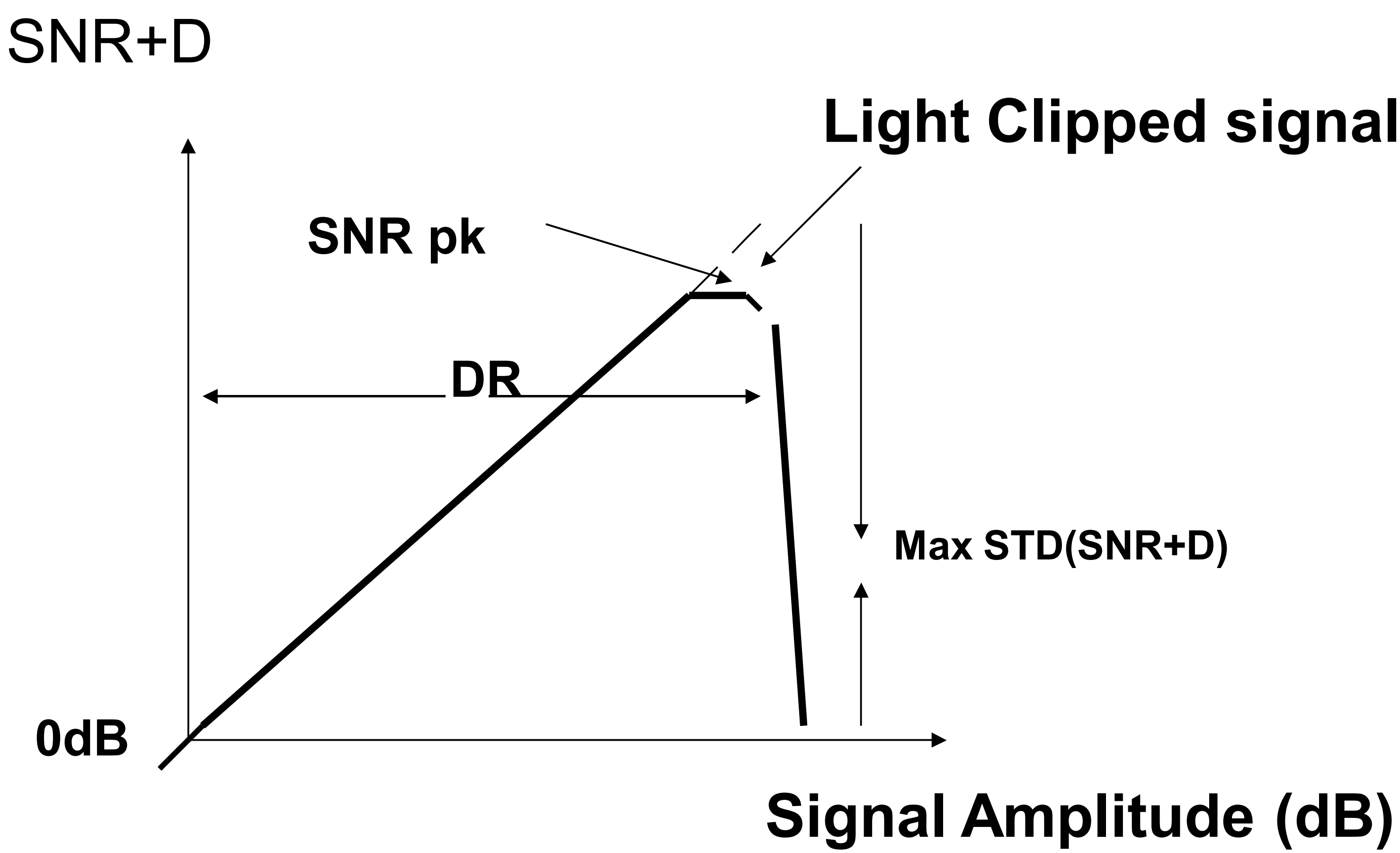


R.H. Walden, "Analog-to-digital converter survey and analysis," IEEE Journal on Selected Areas in Communications, vol. 17, no. 4, pp. 539-550, April 1999.

1.5bit/8yrs – slow improvement..

Dynamic Range DR and SNR, SNRD

DR definition = Maximum signal/min signal(were its berried in noise) in power.



DR may be bigger than SNR Pk
DR $\neq$ SNRpk

FOM

- How To Define a Good?
- Figure of Merit (F.O.M)
- It combines “all“ parameters in one. !

Energy per conversion step! (Pico joules/conversion)

- **Definition 1:**
  How to measure how good is a converter or the inverse (usually for DACs)

- **Definition 2.**

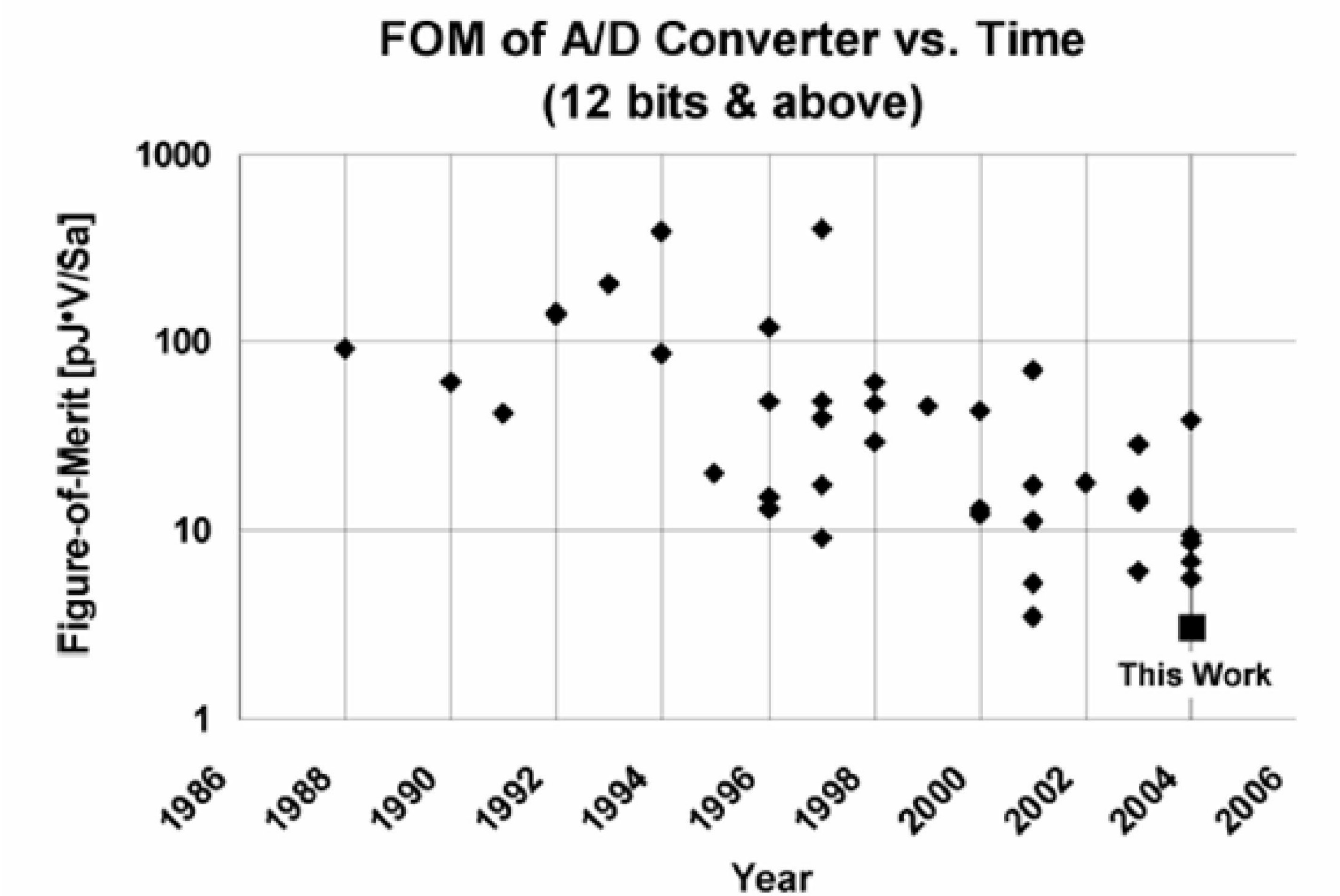
$$FOM = \frac{P}{2^{ENOB} \times 2 \times ERBW}$$

$$Energy\ over\ Decision = \frac{Power}{SamplingRate \cdot 2^{Nbit}}$$

- Energy per conversion step! (Pico joules/conversion)
  - P = Power (does Added element included PLL?)
  - ENOB = Effective number of bits but at full BW or DC?
- No Area? (Sometime you multiply by Vcc)
- Grain of salt: Because of technology and specs are different factor
- **Number below 1 are good**! (..12b/40Mw/5MHz)…

	All designs		High Frequency ((above 500 MHz	
	Average	Median	Average	Median
Energy per decision [pJ]	1.65	0.84	1.71	1.73
Figure of Merit [pJ*V]	7.40	5.48	5.55	5.58

FOM – An Example



Xun Chiu; Gray, P.R.; Nikolic, B.,"A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR", IEEE Journal of Solid-State Circuits, , Volume: 39 , Issue: 12 , Dec. 2004

SFDR (vs. INL)

Definition of SFDR

- ***Spurious Free Dynamic Range of a converter.***
- *Is the ratio of the largest Harmonic component to the signal component*
- *It's a good measure for differential structures and to evaluate mismatches DNL INL effect on ADCs*
- *Can be done AC to be even closer to reality (max BW operation)*
- *How Harmonics and INL do depend on each other?*

$$SFDR(dB) = -20log(|INL|2^{-Nbits} + 2^{-1.5Nbits})$$

Source: R.V. Plassche

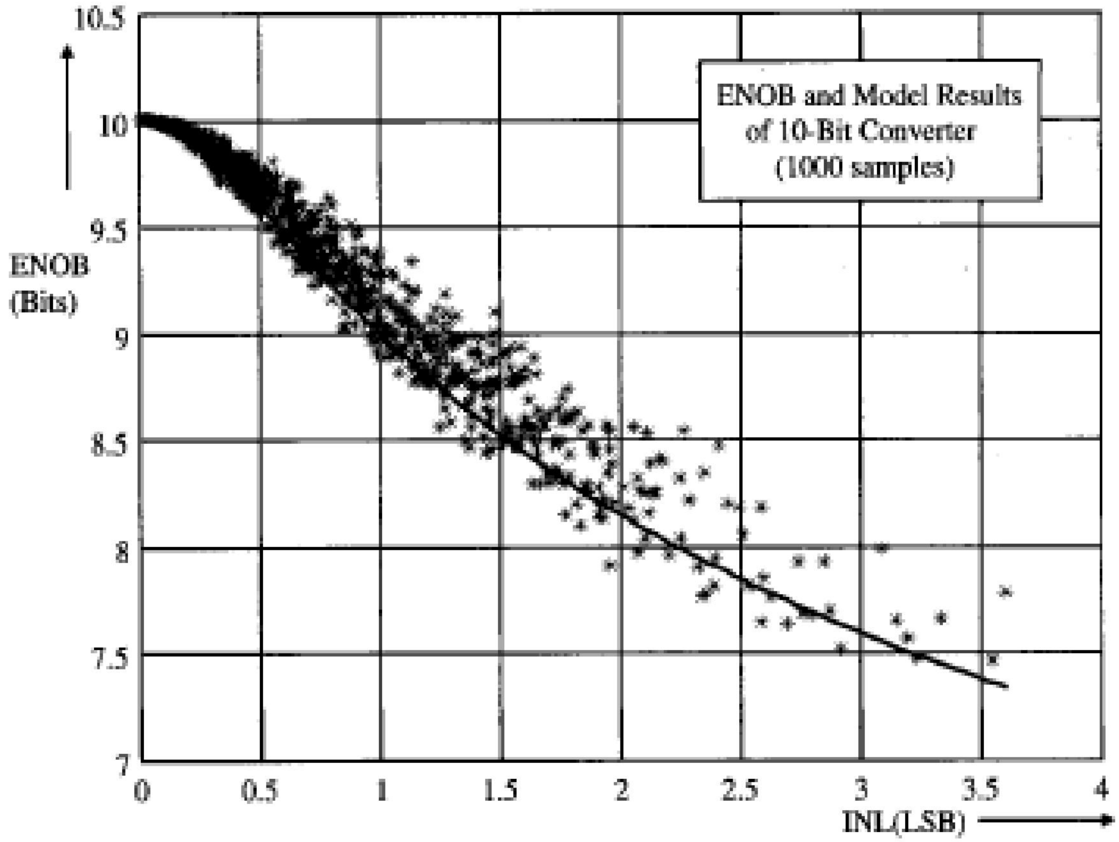
Remember:

- ***The 1.5 comes from the "perfect" converter.***

In general we will try to keep all mismatches to below +/-1/2LSB

ENOB SFDR Vs. INL model

In reality since the converter is not accurate the INL/DNL can be inside the +/-lsb but the converter is not n bit converter !



$$V_{out} = V_{in}(\mathbf{1} + \boldsymbol{INL(LSB)})$$

$$n_{reduction} = \frac{\log\left(1 + 3 * |INL|^2\right)}{2\log 2}.$$

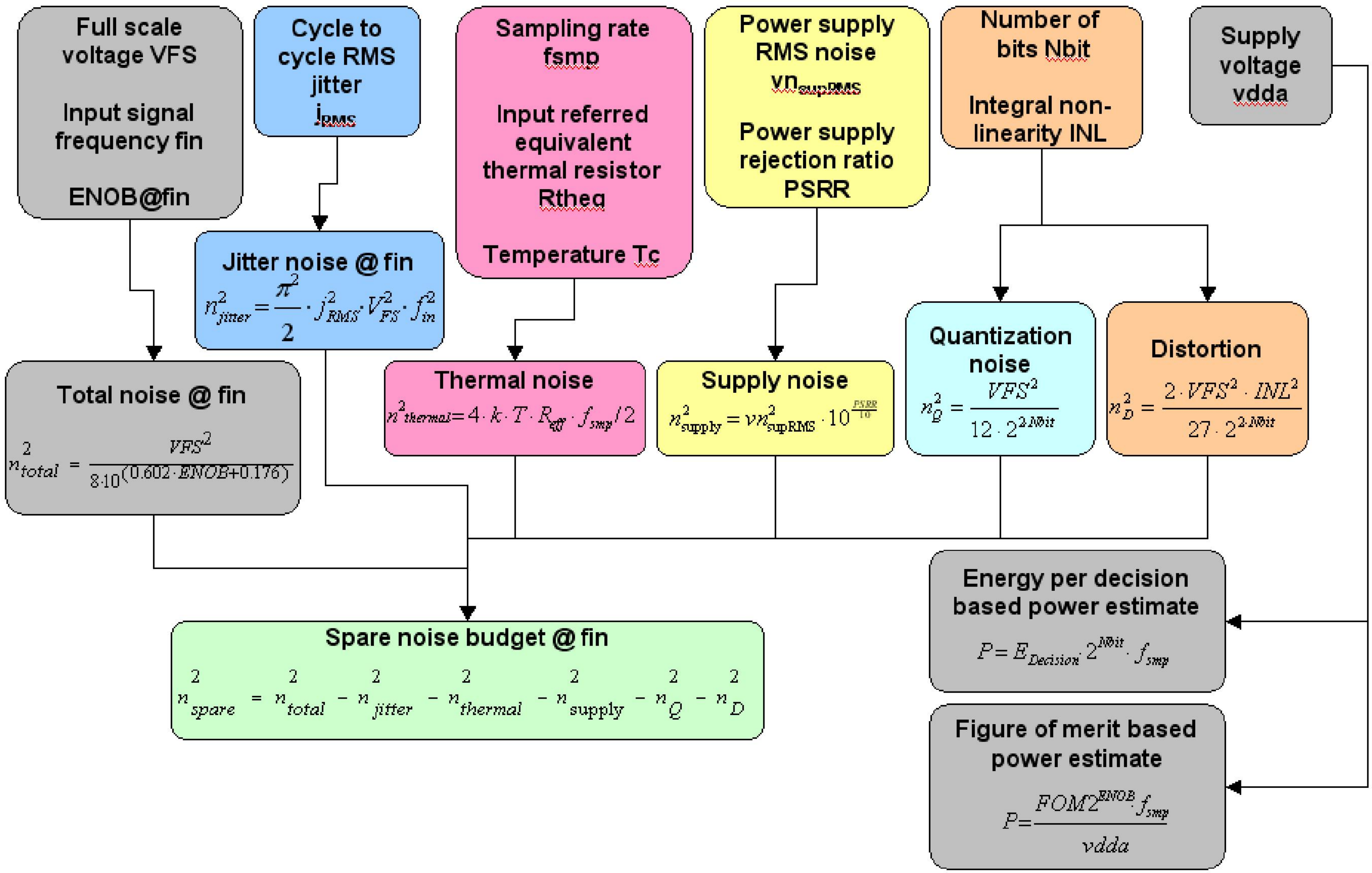
Source: R.V. Plassche

The “INL +1” Needs.

In reality INL of LSB does not means the converter in n bit but more like ~ n-1.

Error	Possible Contributor
Quantization Noise	Design decision – how many bits
Distortions: DNL, INL, missing codes	Mismatches in the design including gnd Maybe power supply or substrate noises
SNR SNRD	Design decision – how many bits; Thermal noises 1/f noises, clock jitter
FOM	**Chosen architecture to meet all the above, and optimum design**

Architecture Independent Calculation Flow



- ***What is the output (WAVE FORM) of an ADC converter sampling at 1MHz clock an input sine wave with 1MHz?***

- ***What is the SNR of triangle input wave form?***

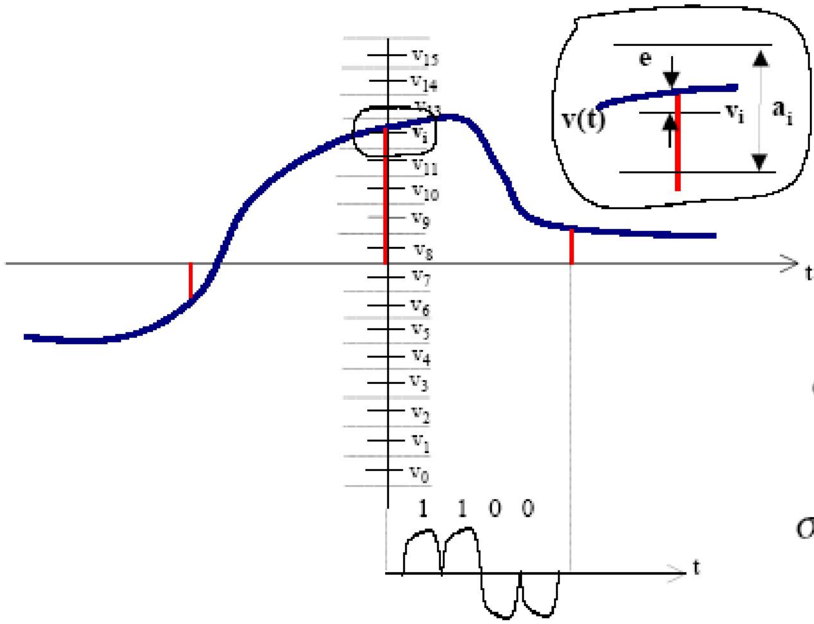
QUESTION # 2 (20

WILL BE PUBLISHED IN LECT 6

End of Lecture #02
Below:
ADVANCED TECHNIQUES

ATMEL ROUSSET — ESSCIRC 2000 Workshop on Embedded Data Converters

Quantization Noise: general analysis



$e = v - v_i$ = Quantization Noise

$$\sigma_i^2 = \int_{vi-ai/2}^{vi+ai/2} (v - v_i)^2 f_v(v / v_{in} i) dv$$

With the change of variable $e = v - v_i$,

$$\sigma_i^2 = \int_{-ai/2}^{+ai/2} (v - v_i)^2 f_{v-vi}(v - v_i / v_{in} i) d(v - v_i)$$

$$\sigma_i^2 = \int_{-ai/2}^{ai/2} e^2 f_e(e / v_{in} i) de = \int_{-ai/2}^{ai/2} e^2 \; {}^1\!/_{a_i} \; de = \frac{a_i^2}{12}$$

$\sigma^2 i$ = Variance = Quantization Noise Power (mean square) = **$a_i^2/12$**

σi = Standard deviation = Quantization Noise rms value = **a_i/sqr(12)**

(assuming that statistical averages equal temporal averages for ergodic processes)

Numerical Polynomial of the Data Point

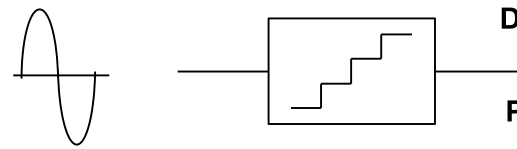
Numerical Polynomial

$$y = f(x) \qquad P_n(x) = f(x)$$

$$P_n(x) = \sum L_n(x) f(x)$$

Where:

$$L(x) = \prod_{\substack{L=k \\ i=0}}^{n} \frac{x - x_i}{x_k - x_i} \qquad Error = \frac{p^{n+1}}{(n+1)!} \prod (x - x_i)$$



Build a polyn from Data

Construct:

$$f(x) = 1 + \alpha_0 x + \alpha_1 x^2 + \alpha_2 x^3 \ldots$$
$$x = \cos \omega t$$

Generate the outputs for each code. You construct a polynomial using the numerical data you look at the Coefficient of the polynomial with x=cos(ωt).

Lagrange Polynomial

$$f(x) = f(x_0) + f(x_0, x_1)(x - x_0) + f(x_0, x_1, x_2)(x - x_0)(x - x_1) \ldots$$

$$f(x_0, x_1) = \frac{f(x_1) - f(x_0)}{x_1 - x_0} \qquad \textit{Newton Form}$$

Quantization Noise Harmonic Derivations

Quantization Error Spectra

$$Error\ (x) = \frac{T_s}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin[n\omega_x Y_{in}(x)]$$

$$Y_{in} = \cos\omega_{in} t$$

$$Error\ (t) = \frac{T_s}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin[n\omega_x cos\omega_{in}(t)]$$

Use Fourier Transform

$$= \frac{T_s}{\pi}\sum_{k=1}^{\infty} a_{2k+1}\cos[(2k+1)\omega_n t]$$

$$a_{2k+1} = \frac{2T_s}{\pi}(-1)^k\sum_{n=1}^{\infty}\frac{J_{2k+1}(n\omega_x)}{n}$$

$$a_{2k+1} = \frac{2T_s}{\pi}(-1)^k \ldots \quad Harmonic\ Level$$

$$J_{2k+1} = Bent\ Function$$

Result

$$\boxed{a_3 = 2^{-n3/2}}$$

Conclusion

Example

10 bit produces 15 bit harmonic sat, -90dB from full scale.

16 bit converter will have ~24x6.02dB third order distortions

SNR

$$Y(kTs) = X(kTs - kTd) + N_o(kTs)$$

$$N_o = E\{N_o(kTs)\}^2$$

$$S_o = E\{X(kTs)\}^2$$

$$SNR \equiv \left(\frac{S_o}{N_o}\right)$$

$$SNR(dB) \equiv 10log\left(\frac{S_o}{N_o}\right)$$

$$SNR \equiv \frac{S_o}{N_o} = \frac{E\{X^2(kT_s)\}}{E\{n_o^2(kT_s)\}}$$

Source: K.S.Shanmugam

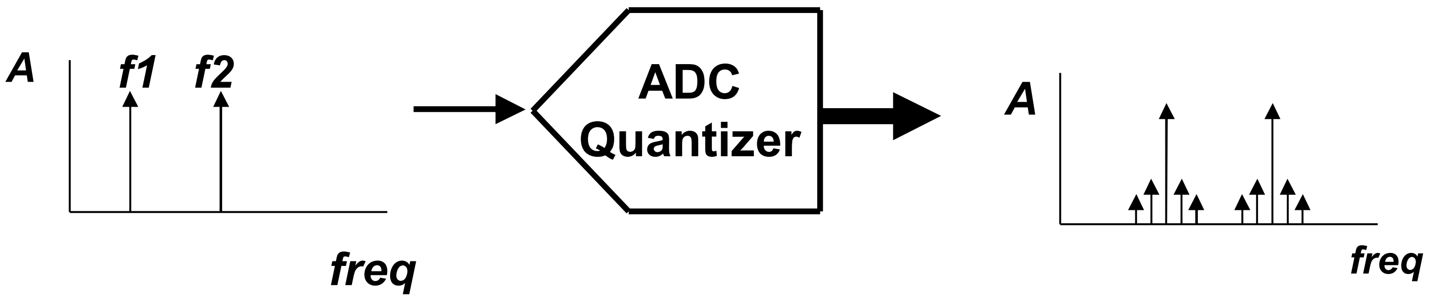
Intermediation Distortions (IMD):

When we apply to a converter two signals f1 and f2 close in frequency.
The amount of distortions due to the converter digitizing the signals is specified as :

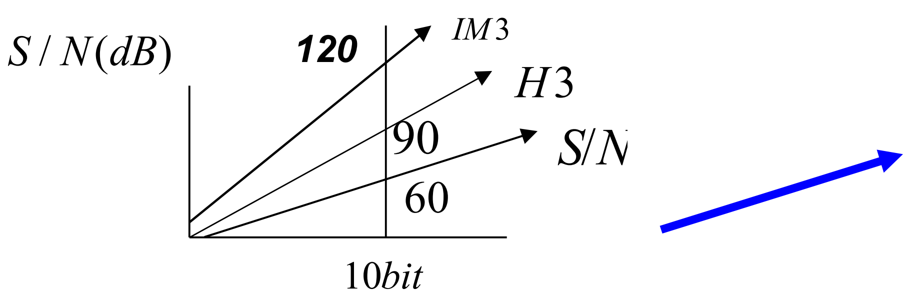
$$\text{IMD} = 20\text{Log}_{(10)} \frac{\text{RMS sum of distortion terms}}{\text{Input (Volts, RMS)}}$$

where the distortion terms are given by

2nd-order terms: - f1 + f2, f1 - f2
3rd-order terms: - 2f1 + f2, 2f1 - f2, f1 + 2f2, f1 - 2f2



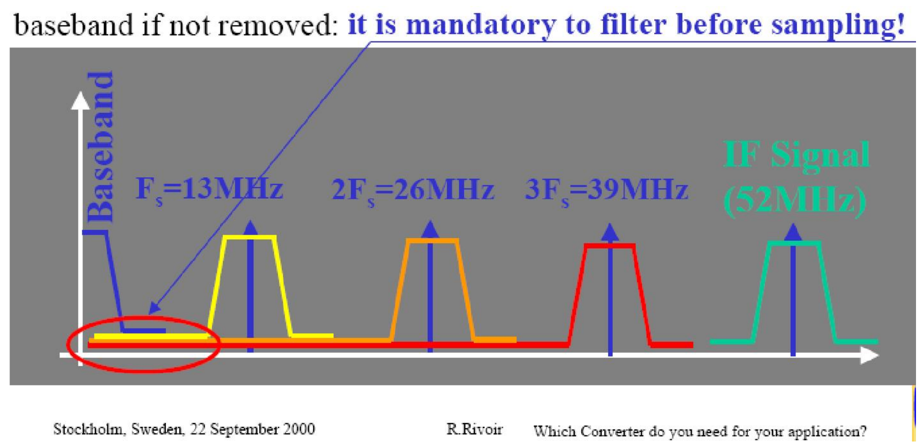
A

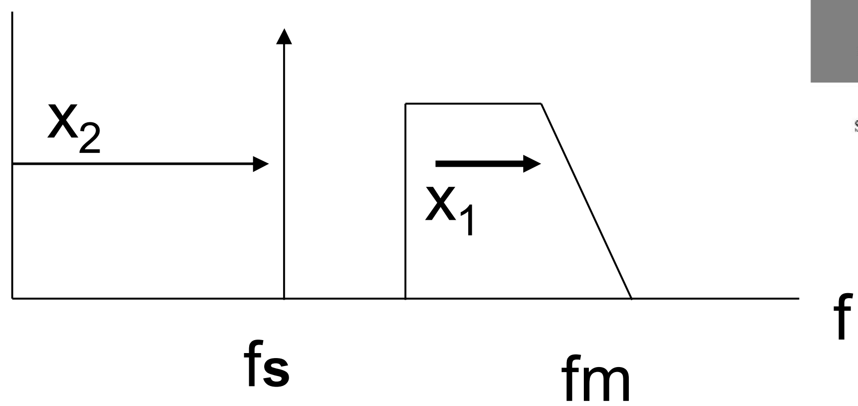


2^{-n} $2^{-1.5n}$ 2^{-2n}

Example
10 bit produces "20 bit IM harmonic" IM3 at -120dB from full scale.
Almost not to worry above 10bit

Sample at low clock converter: max speed lowest clock 2fm < fs





But: Design must take care of the fastest signal (slewing, BW is at f_m

$X_2 > 2x_1$

Signals placed at high frequency with band limitation can be reproduced with low rate clock.
Without contradiction to sampling theory.
The original signal spectrum folds in the base band

BW of signal is the limitation only not location (BPF)

END Lect. 02