X

Welcome to 046188 Winter semester 2013 Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal

Lecture 02...and 03.

Converters Basic Theory and Definitions

Definitions/terms- SNR, ENOBs, DNL, INL.. And Sampling theory..

www.gigalogchip.com

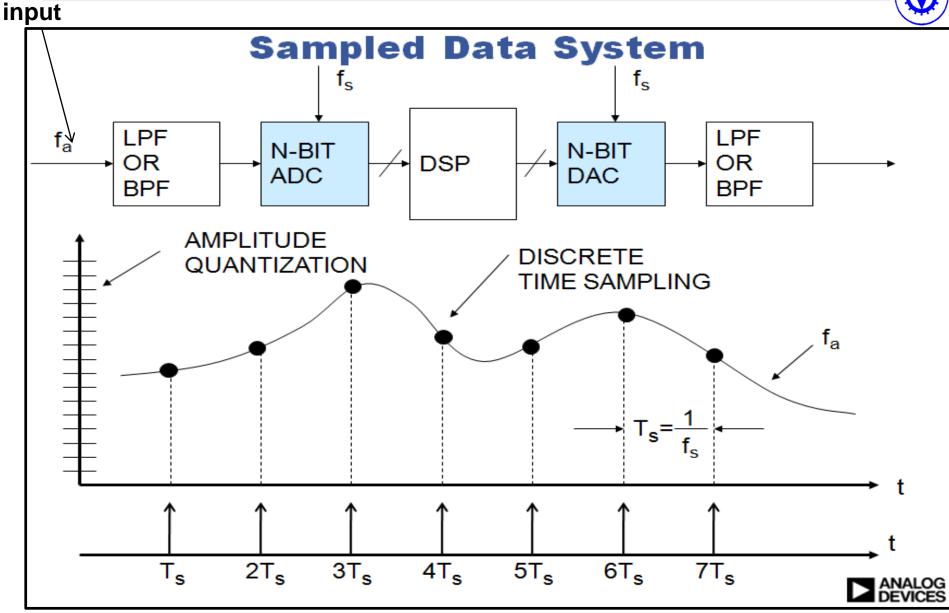
Converters Definitions

X

Sample rate and Resolution Quantization noise (Qn) and Harmonics QN for Dual tones SNR- Signal to Noise DR - Dynamic Range Distortions: DNL, INL, missing codes SNRD- signal to noise + Distortions ENOBs – Effective number of Bits SFDR- Spurious Free Dynamic Range FOM CLOCK Phase Jitter effect on SNR

Top Building Blocks





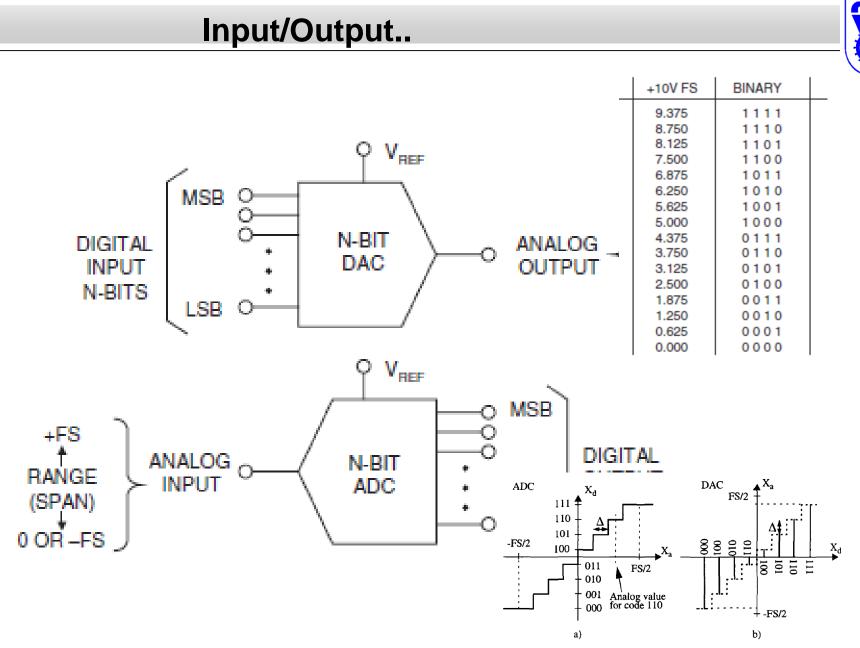


Figure 1-2 The ADC (a) and DAC (b) transfer functions for N = 3.



Definition: It's the Rate of digital bits that are coming out

Mostly it's the clock rate (non over sampled system).

In Many converters the maximum data frequency is 1/2 of this. Depend on signal input maximum BW

Example: a 10 bit ADC runs at 2MS/S means:

2Ms/s \rightarrow Output rate is 2mega sample per second, means Sampling clock rate is 2MHz each of the 10 bits rate maximum is 1MHz. It's the measure of number of digital bit at the output of the converter (ADC).

Its not an indication of the quality of the converter (bits may or may not move).



Number of digital bits or levels



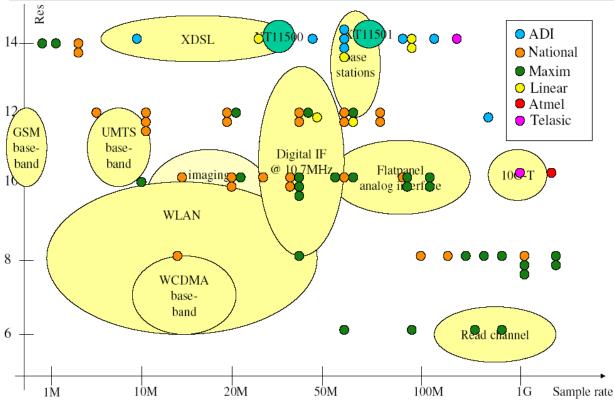
The number of bits of the digital code is finite, namely n.

For n bit we have

 2^n Possible levels 2^n -1 Possible steps

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Application: data rate and resolution



Resolution Rate

SOME Mixes Signal APLICATIONS

U		
Wireless LAN	1-100MS/s, 6-11b	
Magnetic storage	0.2 – 1GS/s , 6-8b	
xDSL	1Ms/s - 100MS/S 11-14b (30 MHz adc)	
Ultrasound	40MS/S 8-12b	
AKG	~ Ks/s 18-22bit	
Digital TV	20MS/s 8-10b (base band)	
Handy- GSM	400MS/s 12b (base band)	
CATV decoder	10-20 MS/s 8-10b (modem ADC)	
HDTV	50-100 MS/s, 10b	
1-10GbaseT	130MS/s-840MS/s 7b-9b	
Videos, Audiose		

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QUANTIZATION NOISE

The number of bits of the digital code is finite, namely n. For n bit we have possible codes each code represent a given quantization level.

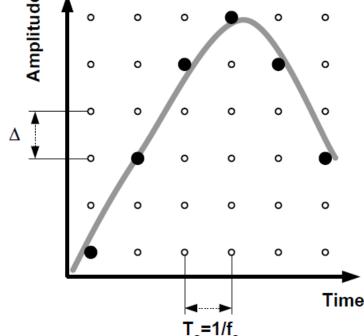
The error due to the quantization is called the *quantization error* and ranges between + and – half quantization level (LSB).

This error is one more measure of the ADC quality

possible codes
$$= 2^{n}$$

- Digital bits are integers: 9, 10, 16 etc..
- Therefore can't represent the
- input signal perfectly: error

Quantization error cant be higher then the resolution, vice versa is possible



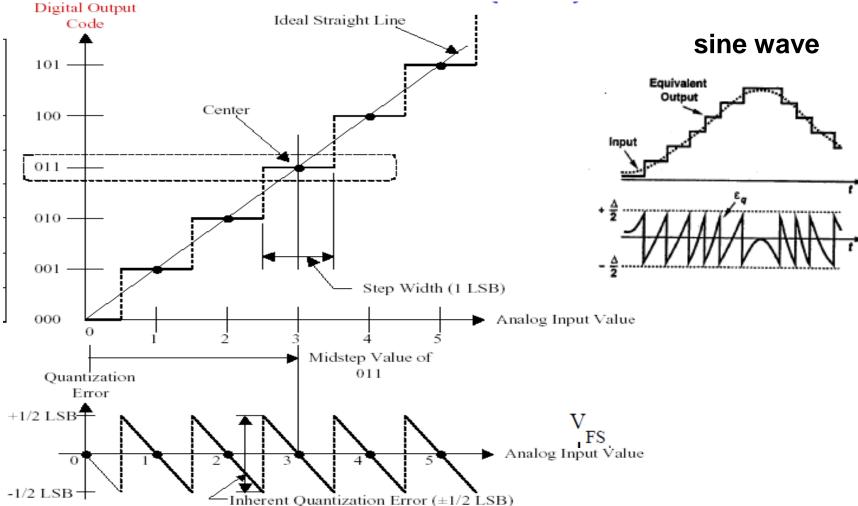


Analog Signal

Discrete time, discrete amplitude representation

QUANTIZATION NOISE

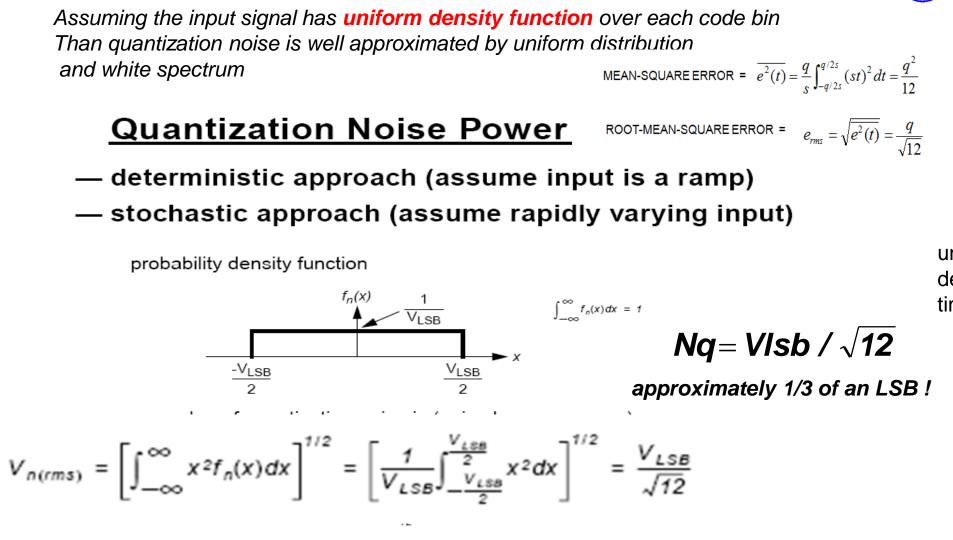




Input minus output after gain and offset errors are nulled

QUANTIZATION NOISE CALCULATION

X



• this noise power is spread between $-f_s/2$ and $f_s/2$

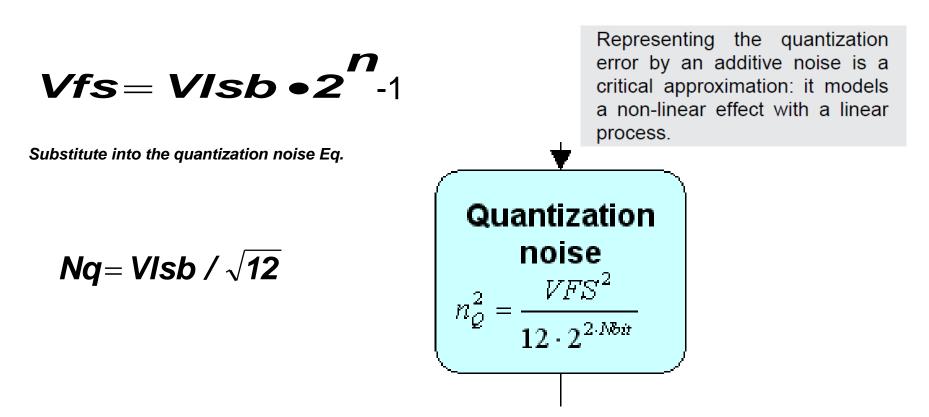
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Nq

QUANTIZATION NOISE- Cont. in term of full scale



Full scale voltage is the parameter we're interested in. To maximize or distribute all the available codes we split the full scale (Vpk) to all the possible codes.



A sine wave for example at the end point (slowly moving input) may not be uniform enough over the code bin.

Sample rate not repeated "close" to signal frequency or Nq. will not have enough information..

SNR

Definition SNR

In telecommunication the output quality is measured in term of Signal to Noise Ratio (SNR)

Definition: SNR is defined as the ratio of output signal So power to the base band noise power at the output No. Including quantization, Harmonics (sometime not), and all flicker thermal jitter noises.

SNR=20log(Vin(rms) / Vq(rms)

$$Y(kTs) = X(kTs-kTd) + No(kTs)$$

$$No = E\{No(kTs)\}^{2}$$

$$SNR = \frac{S_{0}}{N_{o}} = \frac{E\{X^{2}(kT_{s})\}}{E\{n_{o}^{2}(kT_{s})\}}$$

SNR(dB) = 10 • log(So / No) Source: K.S.Shanmugam

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SNR≡(So / No)

SNR



Theoretical Quantization Noiselet : q=VlsbIdeal N-Bit Converter

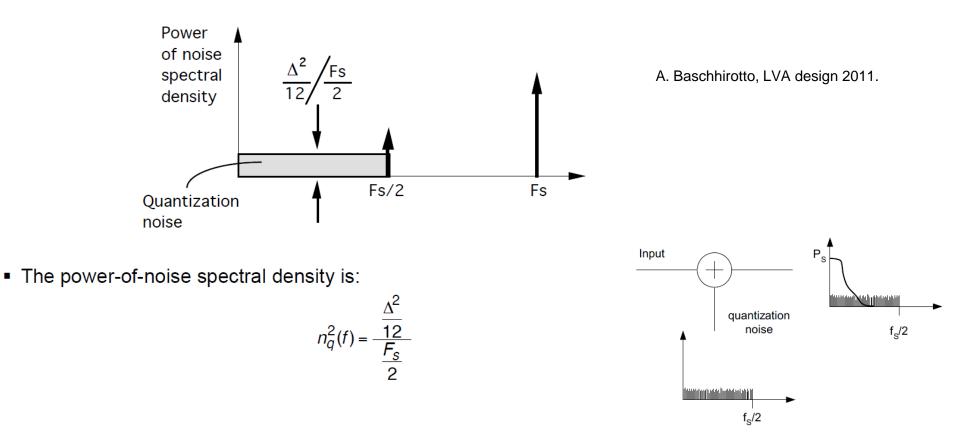
$$SNR = 20 \cdot \log_{10} \left[\frac{Full_Scale_Sinewave_(rms)}{Quantization_Noise_(rms)} \right]$$

Signal power = Acaus 3q uare Airf

$$\frac{1}{2} = \frac{1}{2 \Pi} \int_{0}^{2 \Pi} \int_{0}^{1$$

QUANTIZATION NOISE DENSITY- None reverse process

It is assumed that the quantization noise exhibits a white spectrum



Sample rate not repeated close to signal frequency or Nq. will not have enough information..

Key: The noise is spread: to +/- fs/2 (Nyquist interval) or 0-fs/2 (representation)

QUANTIZATION NOISE DENSITY: EXAMPLE

Key: How far does it spread and how does it depend on frequency?

```
The quantization noise spreads to the half of the clock frequency. (+ / - fs/2 same as 0-fs/2 )
That is to say we can define quantization noise per root hertz. And now get the
Total noise for a fixed BW that we operate in. ( a must for non nyquist converters)
```

EXAMPLE1 :

a) If LSB is 1 mV and we sample at 2 MHz: 288uV is spread over 1 MHz. which means 0.288uV/sqrtHz (288u-6/sqrtHz{(1e6)}

b) If we sample at 16 MHz the quantization density is : 0.101 uV/sqrHz (divide by sqrt(8). 0.288/2.82.

Conclusion

Good to increase the sampling clock we profit: 10 log (fs/ fsignal BW) = 3dB/octave !

Example2 (the dB) 10 bit adc with max input BW=1MHz and 2MHz sampler quantization noise is: ~60 dB 10 bit adc with 1MHz BW and 16MHz sampler quantization noise is: ~69 dB

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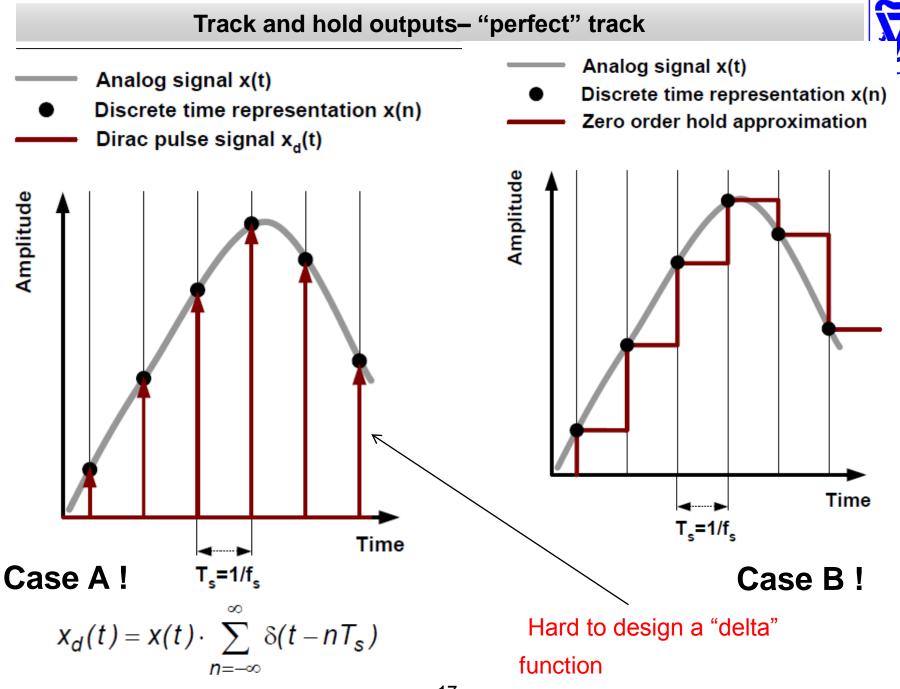
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logð



SAMPLING PROCESS OVERVIEW

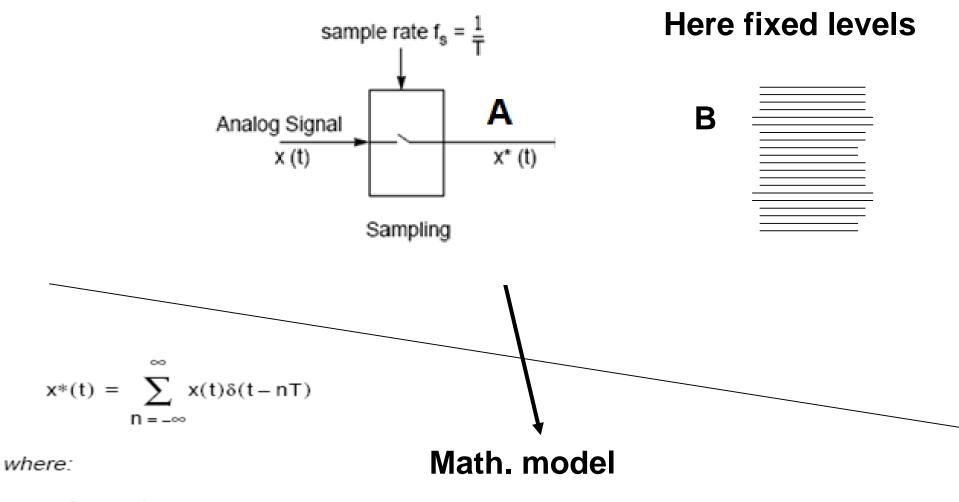
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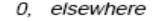
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sampling process



 $\delta(t) = 1, t = 0,$



What is the difference at point A and B ? ... (Nq)

Case A ! SAMPLIN X_5(£) ATIJO S(E-nis) TIME POMA Xs(e) = X(e) · Z S(e-nTs) , (s(e) de = -1 also since Sid = & everywhere exapt @ t= D. $X_{s(t)} = \sum_{i=1}^{\infty} X(nT_s) \cdot S(t-nT_s)$ FE.] =) delined as Fourier openTim. $F(X, \omega) = X(P) = X(P) + F\left[\stackrel{\alpha}{\geq} \int (t - nT_s)\right]$ P. Z. S(t-nb) prove 1 > Xs(P) = B. Z ×(P-nls) Ps X(P) + Ps·X(P-Ps) + Ps X(P-2Ps) + Ps X(P-3Ps) + ls X(P+1s) + Ps X(P+2Ps)+Ps X P+3Ps+ - -7(9) gove Cx. -Px X 5(b) Techriight 040100/2010 Leui 02

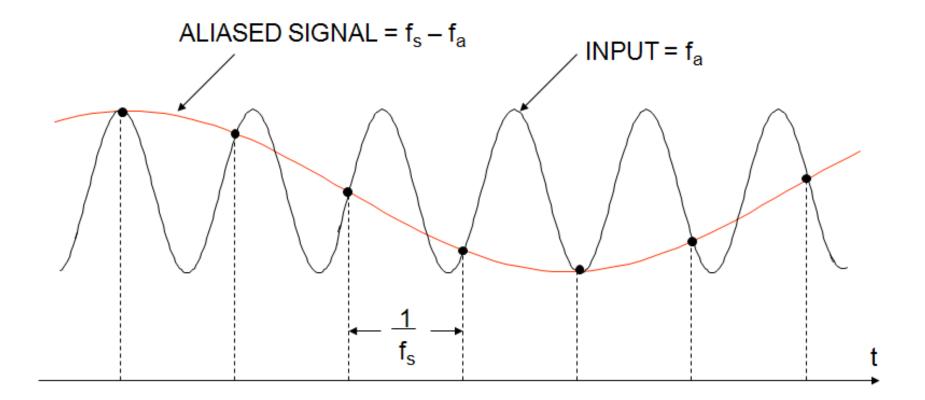


Any pEniodic Signal Cambe constructed from sum of sine waves. The power (on p.S.D) - Density 15 5x = \$ 1Cx(nh) 12 S(P-nh) d P = pour also l- + 1/2 Gx(P) - + 1/2 db

Key: The power of X(t) is the same in f domain= sum of the coefficient



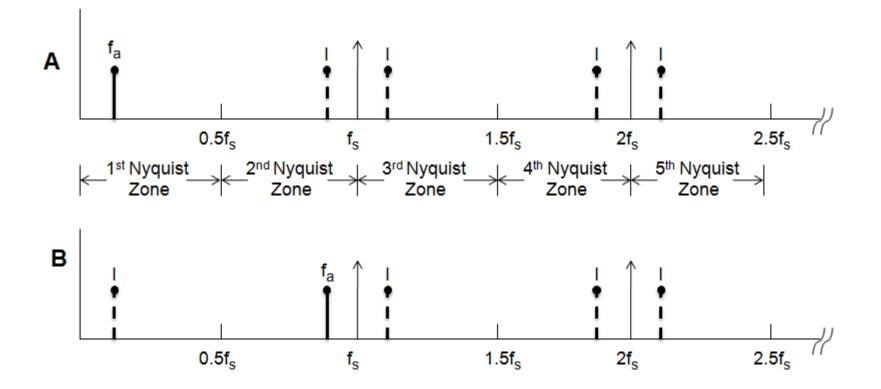
Aliasing in the Time Domain



NOTE: fa IS SLIGHTLY LESS THAN fs



Aliasing in the Frequency Domain



fa is the input signal sampled at fs

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Sampling: the Shannon Theorem

• The Shannon Theorem says: "If a signal x(t) has a Limited Bandwidth (-BW,BW), it can be univocally determined by its samples x(nT) if the Sampling Frequency is at least twice the Bandwidth: $f_s = 1/T \ge 2BW$ "

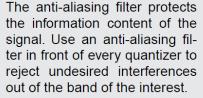
• Note:

1) Limited Bandwidth is a **Necessary but not Sufficient** condition

2) $1/T \ge 2BW$ is only a **Sufficient but not Necessary** condition

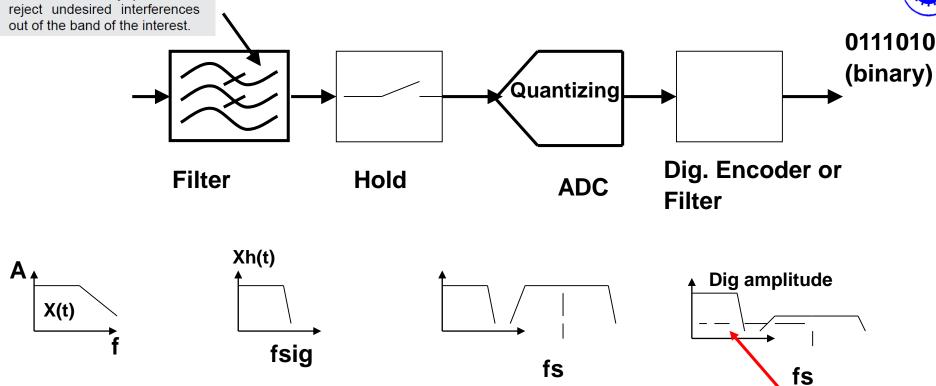


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Converter Building Blocks





Typical ADC path (Nyqist Conversion)

- 1) Not all converters needs Sample/Hold
- 2) Not all Converters needs LPF, However some also use BPF (or DC remover)
- 3) Fsignal coming to the converter is Bounded.
- 4) ADC output may or may not have reduced folding but it has noise

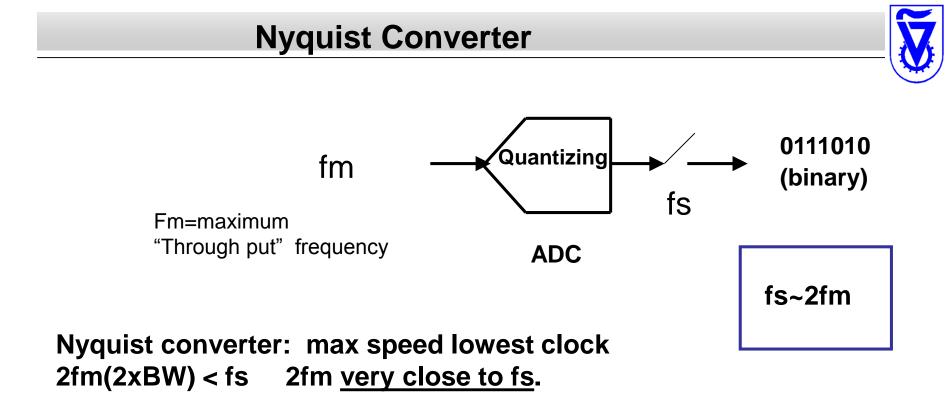
KEY: How each component works, its transfer function, what is the optimum ? first to the definitions ! (lect. 2)

Noise: random

systematic, lin



CLASS OF CONVERTERS

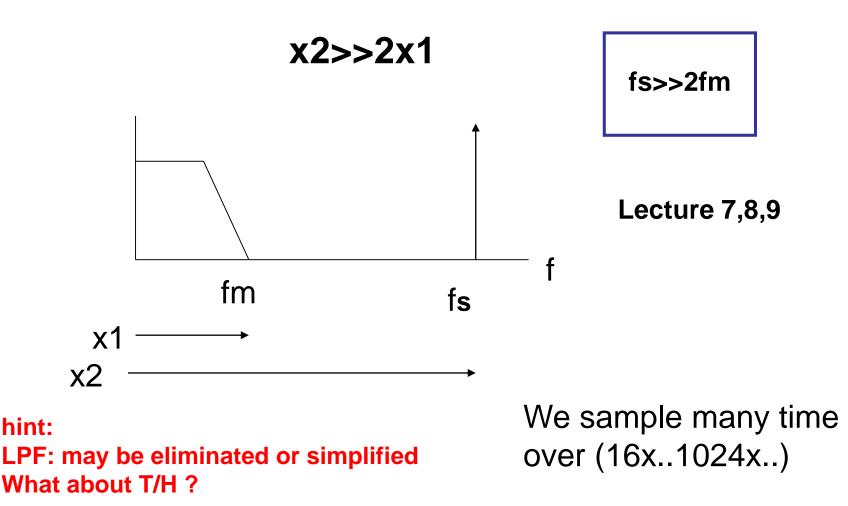


Remember: S&H not always needed LPF: Not always needed





over sample converter: max speed lowest clock 2fm < fs

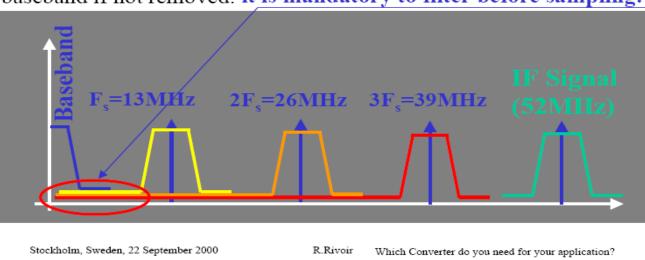


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Under sampling Converter



Sample at low clock converter: max speed lowest clock 2fm < fs



baseband if not removed: it is mandatory to filter before sampling!

signals placed at high frequency with band limitation can be reproduced with low rate clock. Without contradiction to sampling theory. The original signal spectrum folds in the base band

BW of signal is the limitation only, not its location (BPF)

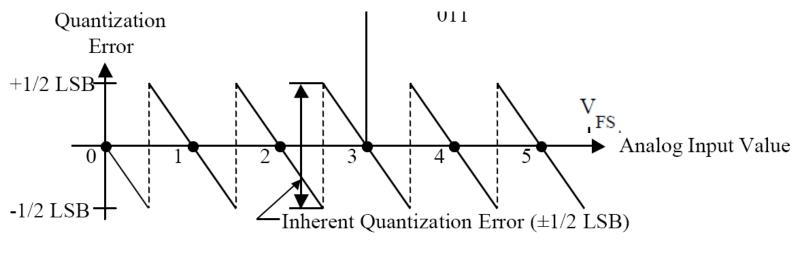
But: Design must take care of the fastest signal (slewing, bw etc..)

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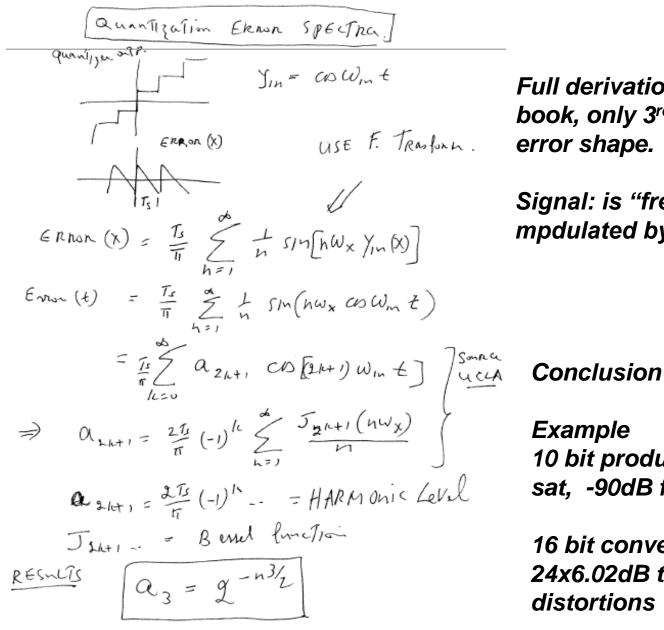
Can quantization produce non linear output signal? – Yes.

We measure its Harmonics ? Non linearity's ?



Elements of Transfer Diagram for an Ideal Linear ADC

QUANTIZATION NOISE HARMONIC DERIVATIONS



Full derivation in page 12 in the book, only 3rd H. due to trangle error shape.

Signal: is "frequency mpdulated by the error"

10 bit produces 15 bit harmonic sat, -90dB from full scale.

16 bit converter will have ~-24x6.02dB third order distortions



Intermediation distortions (IMD):

When we apply to a converter two signals f1 and f2 close in frequency. The amount of distortions due to the converter digitizing the signals is specified as :

Full derivation in page 18-19 in the book, only 3rd H. due to triangle error shape.

 $IMD = 20Log_{(10)} \frac{RMS \text{ sum of distortion terms}}{Local Charles DMS}$

Input (Volts, RMS) Remember the results.

where the distortion terms are given by

2nd-order terms: - f1 + f2, f1 - f2 3rd-order terms: - 2f1 + f2, 2f1 - f2, f1 + 2f2, f1 - 2f2

Called : Cross Modulation...(the IM3)

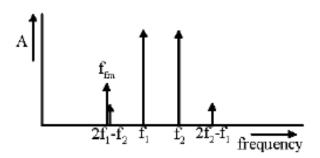
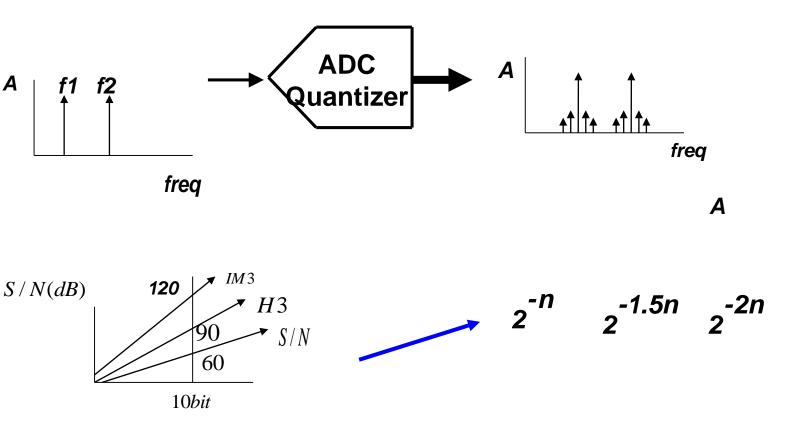


Figure 2: Third-order intermodulation effect

QUANTIZATION NOISE HARMONIC MORE THAN 1 TONE





Example 10 bit ADC produces "20 bit IM harmonic" IM3 at -120dB from full scale. "Almost" ok to ignore.. When using over 10bit converters..



$$SNR_{sine}\Big|_{dB} = (6.02 \cdot n + 1.78)$$
 a

$$SNR_{triang}\Big|_{dB} = (6.02 \cdot n) dB$$

number of bits	S/N Accurate	S/N n 6.02 + 1.76
n	$^{\mathrm{dB}}$	dB
, 1	6.31	7.78
2	13.30	13.80
3	19.52	19.82
4	25.59	25.84
5	31.65	31.86
6	37.70	37.88
7	43.76	43.90
8	49.82	49.92
9	55.87	55.94
10	61.93	61.96
u		

Table 1.1: S/N as a function of the number of bits n

The signal-to-noise of an n-bit converter is accurately modeled with:

$$S/N(n) = \frac{A_1}{A_{quantization}} = \frac{2^{n-1} + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_1(2m\pi 2^{n-1})}{\sqrt{\sum_{q=1}^{\infty} (\sum_{m=1}^{\infty} \frac{2}{m\pi} J_{2q+1}(2m\pi 2^{n-1}))^2}}$$
(1.45)

will prove n=1 later in the course

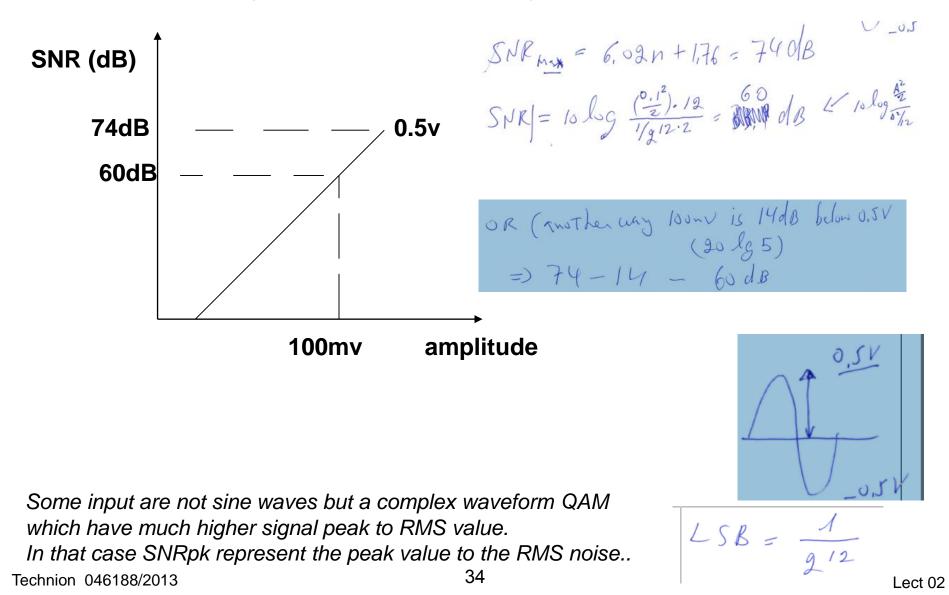
Remember:

But it is not exact for 1-4 bit there is some deviation (1bit: 6.31dB instead of 7.78 dB) Above 4 bits the error is in the second digit point of the SNR

EXAMPLE cont.



Example 100mV sine wave is applied to an Ideal 12b converter which has its maximum range at 1V. Find the SNR of the digitized output, plot it





DISTORTIONS IN CONVERTERS

(beside Quantization Noise)

1.6.4 Total Harmonic Distortion (THD)

The total harmonic distortion (THD) is the ratio of the total harmonic distortion power and the power of the fundamental in a certain frequency band, i.e.

$$THD = 10 \cdot \log\left(\frac{\text{Total Harmonic Distortion Power}}{\text{Signal Power}}\right)$$
$$= 10 \cdot \log\left(\sum_{k=2}^{\infty} X_k^2 / X_1^2\right)$$
(1-56)

where X_1 is the rms value of fundamental and X_k the rms value of the *k*-th harmonic component. Since there is an infinite number of harmonics the THD is usually calculated using the first 10-20 harmonics or until the harmonics can not be distinguished from the noise floor. The THD is sometimes defined as

$$THD = 10 \cdot \log \left(\frac{\text{Signal Power}}{\text{Total Harmonic Distortion Power}} \right)$$
(1-57)

How to calculate distortion noise



Methods

- 1) Fourier transform of the output points this is our project effort.
- 2) Evaluate with Numerical Polynomial of the data point
- 3) Evaluate the INL (and DNL) make sensible decision.

Results

- 1) Most accurate
- 2) Accurate but tedious (need to look at the errors
- 3) Very quick feeling on what's going on (wors case only)

2. Numerical Polynomial of the data point

2. Numerical Polynomial of the data point

$$\frac{Numerical Polynomial of the data point}{
Y = f(x) f(x) = f(x)}$$

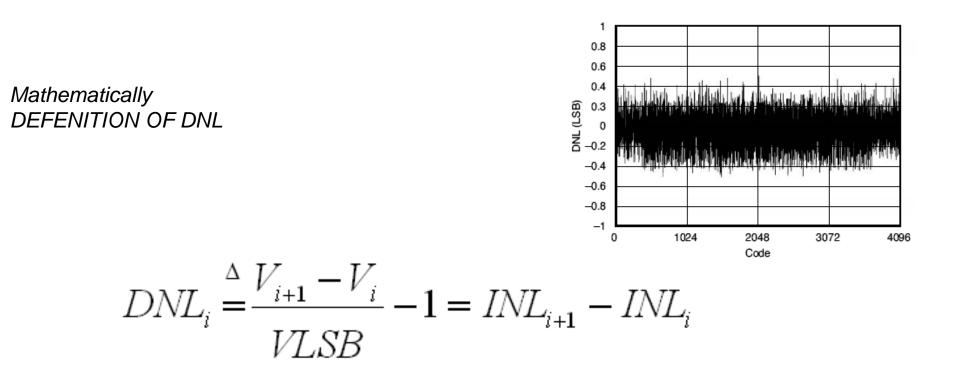
$$f(x) = f(x) f(x) = f(x)$$

$$\int_{k=0}^{\infty} \frac{x - x_{i}}{x_{k} - x_{i}} \quad evon = \frac{f^{n+1}}{(n+1)!} f(x - x_{i})$$

$$\int_{k=0}^{\infty} \frac{x - x_{i}}{x_{k} - x_{i}} \quad evon = \frac{f^{n+1}}{(n+1)!} f(x - x_{i})$$
Generate the outputs for each code.
You construct for each code.
You construct a polynomial using the numerical data you look at the coefficients of the polynomial using the numerical data you look at the coefficients of the polynomial using the numerical data you look at the coefficients of the polynomial with x=cos(wt).

DNL Definition

Differences between two adjacent output digital or analog compared to a step size of LSB weight.



3- cont. INL DACs AND ADCs ERRORS (systematic)



DISTORTION: MISSING CODES, (INL/ DNL)

INL Definition

The Deviation of output code or output signal from straight line drawn from 0 and full scale

after gain and offset are corrected is called Integral Non Linearity (INL) INL leads to Harmonic distortions !

Monotonic: The output never decreases with increase of code or signal if INL<1 LSB the converter is monotonic- no missing codes.

Mathematically DEFENITION OF INL

$$INL_{i} \stackrel{\Delta}{=} \frac{V_{i} - Voff}{VLSB} - i + \frac{1}{2}$$

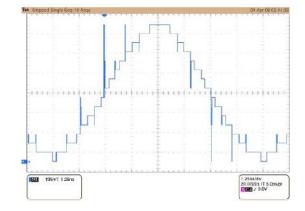
DNL/INL

X

INL is measure of worst case distortion However, we do not know how and were the DNL/INL is corrupted therefore only FFT is accurate.

INL is a close indication of linearity (THD) (remember should we extent the INL/DNL to AC)?

<1 LSB INL implies less than 1 LSB DNL <1 LSB DNL does not implies less than 1 LSB INL



INL related to DNL- YIELD



THE RELATIONSHIP BETWEEN THE 2 :

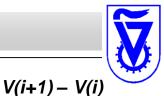
• Means that once we computed DNL, we can easily find INL using a cumulative sum operation on the DNL vector

$$INL_i = \sum_{k=-Nout_{Max}}^{i-1} DNL_k$$

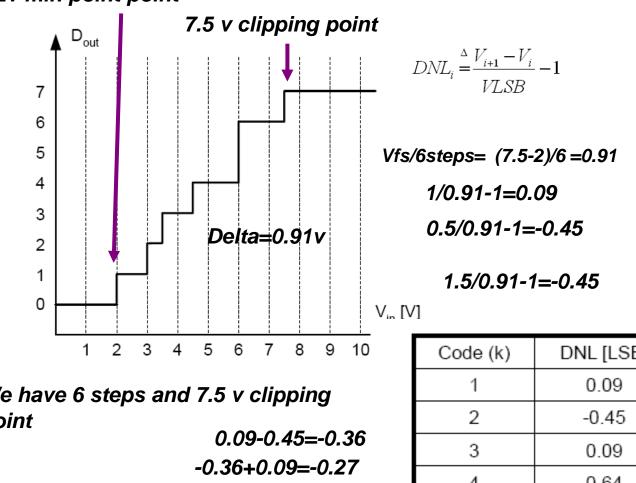
$$DNL_{i} \stackrel{\Delta}{=} \frac{V_{i+1} - V_{i}}{VLSB} - 1 = INL_{i+1} - INL_{i}$$

If INL/DNL are due to elements in the analog blocks not linear/equal they are either systematic we made mistake in the design or mismatch in silicon (resistors/current source) -> YIELD IS EFFECTED – calculate it

INL/DNL- in class example







U			
1	1		
2	0.5		
3	1		
4	1.5 0		
5			
6	1.5		
7	undefined		

0

undefined

We have 6 steps and 7.5 v clipping point

-0.27+0.64=0.37

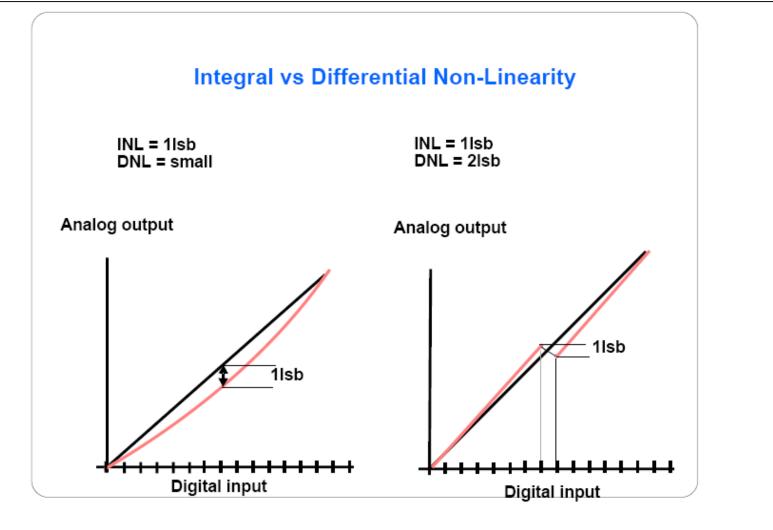
0.37 - 1 = -0.64

example : (Source: B.Murmann Stanford)

			•
Code (k)	DNL [LSB]	INL (LSB	
1	0.09	0	
2	-0.45	0.09	
3	0.09	-0.36	
4	0.64	-0.27	
5	-1.00	0.36	0.37
6	0.64	-0.64	
7	undefined	0	

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Example2



<1 LSB DNL does not implies less than 1 LSB INL

Summary



In general our object is to keep all mismatches to below +/-1/2LSB

ENOBS

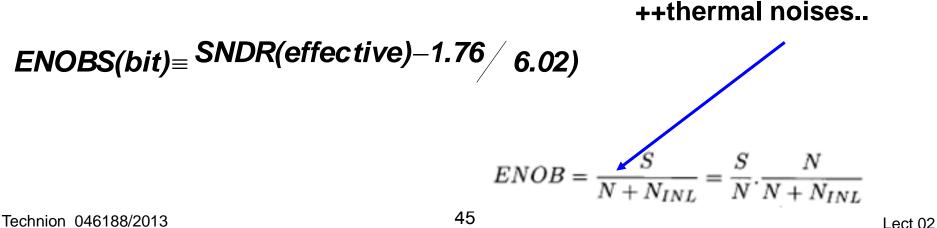
SNDR is the measured value

SNDR is measure of effective resolution ("real" of the converter N- Quantization **D-Harmonics**

DFINITION OF ENOBS

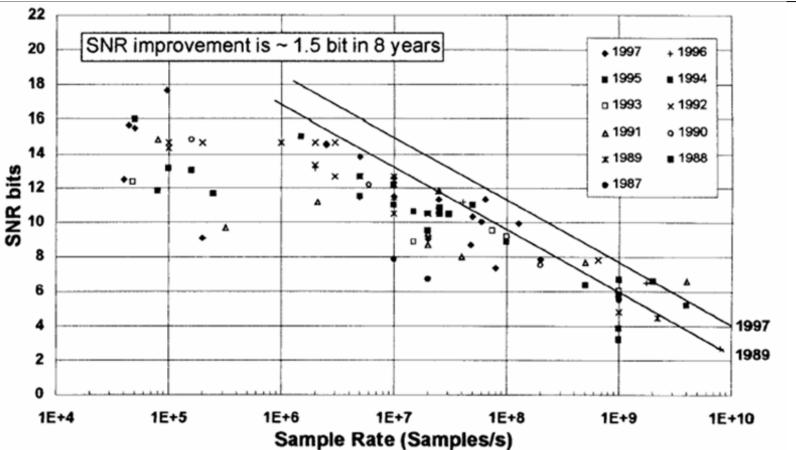
Linearity test: 1. With a Line set by end points (on occasion is best fit)- DC measure – can we extend to AC?

1.FFT the output – will tell it all. **ENOB** is the effective number of bits





ENOBS improvmrnts..



R.H. Walden, "Analog-to-digital converter survey and analysis," IEEE Journal on Selected Areas in Communications, vol. 17, no. 4, pp. 539-550, April 1999.

1.5bit/8yrs – slow improvement..

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Definition of SFDR

Spurious Free Dynamic Range of a converter.

Is the ratio of the largest Harmonic component to the signal compo

It's a good measure for differential structures and to evaluate mism CAN BE DONE AC TO BE EVEN CLOSER TO REALITY (MAX B

 $i_{o}(t) = \alpha_{1}v_{i}(t) + \alpha_{3}v_{i}^{3}(t) + \alpha_{5}v_{i}^{5}(t) + \alpha_{7}v_{i}^{7}(t) + \dots$ (1)

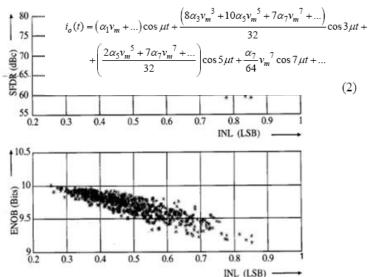
where the α_i parameters are determined from the particular circuit implementation. For a harmonic input of the type: $v_i(t) = v_m \cos \mu t$, and after grouping of the frequency components, (1) can be rewritten in the form:

$$i_{o}(t) = (\alpha_{1}v_{m} + ...)\cos\mu t + \frac{(8\alpha_{3}v_{m}^{3} + 10\alpha_{5}v_{m}^{5} + 7\alpha_{7}v_{m}^{7} + ...)}{32}\cos 3\mu t + \left(\frac{2\alpha_{5}v_{m}^{5} + 7\alpha_{7}v_{m}^{7} + ...}{32}\right)\cos 5\mu t + \frac{\alpha_{7}}{64}v_{m}^{7}\cos 7\mu t + ...$$

gated via a Taylor expansion of the $i_o = f(v_i)$ function in the equilibrium point:

$$i_{o}(t) = \alpha_{1}v_{i}(t) + \alpha_{3}v_{i}^{3}(t) + \alpha_{5}v_{i}^{5}(t) + \alpha_{7}v_{i}^{7}(t) + \dots$$
(1)

where the α_i parameters are determined from the particular circuit implementation. For a harmonic input of the type: $v_i(t) = v_m \cos \mu t$, and after grouping of the frequency components, (1) can be rewritten in the form:



Source: R.V. Plassche

$$SFDR(dB) = -20\log(|INL| 2^{-N_{bits}} + 2^{-1.5N_{bits}})$$

Remember: The 1.5 comes from the "perfect" converter.

In general we will try to keep all mismatches to below +/-1/2LSB Technion 046188/2013 47





HOW TO DEFINE A GOOD ADC? Figure of Merit (F.O.M) It combines "all" parameters in one. !

FOM

Energy per conversion step! (Pico joules/conversion) Definition 1 How to measure how good is a converter Or the inverse (usually for DACs) Definition 2.

$$FoM = \frac{P}{2^{ENOB} \times 2 \times ERBW}$$
 Energy/Decision = $\frac{Power}{SamplingRate \cdot 2^{Nbit}}$

Energy per conversion step! (Pico joules/conversion)

- P = Power (does Added element included PLL?)
- ENOB = Effective number of bits but at full BW or DC?
- No Area? (Sometime you multiply by Vcc)
- Grain of salt: Because of technology and specs are different factor

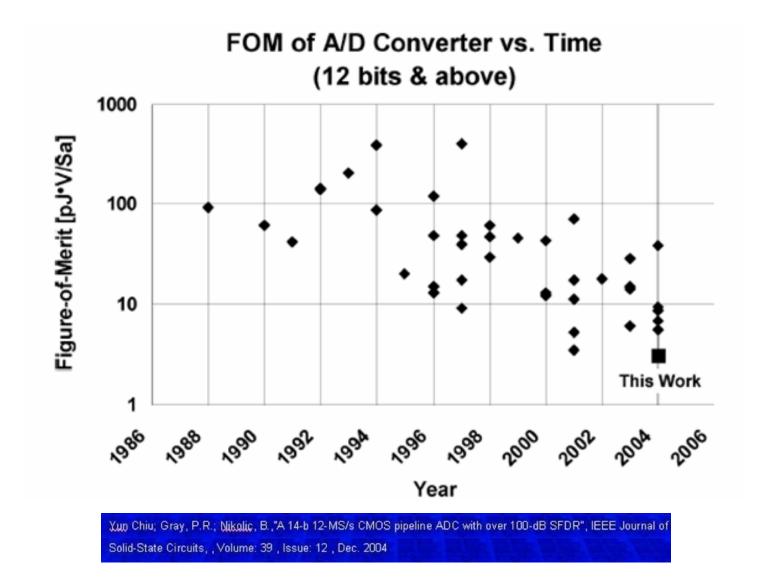
Number below 1 are good! (..12b/40Mw/5MHz)

	are	All designs		High Frequency ((above 500 MHz	
)		Averag e	Media n	Averag e	Median
	Energy per [decision [pJ	1.65	0.84	1.71	1.73
	Figure of [Merit [pJ*V	7.40	5.48	5.55	5.58

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Key: Linearity (INL) reduction on SNRD(ENOBs)

ENOB SFDR Vs. INL model

In reality since the converter is not accurate the INL/DNL can be inside the +/- 0.5 Isb but the converter is not n bit converter !

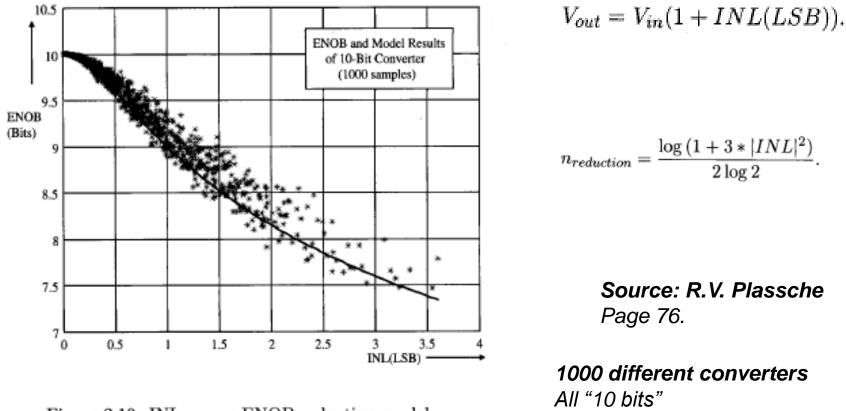
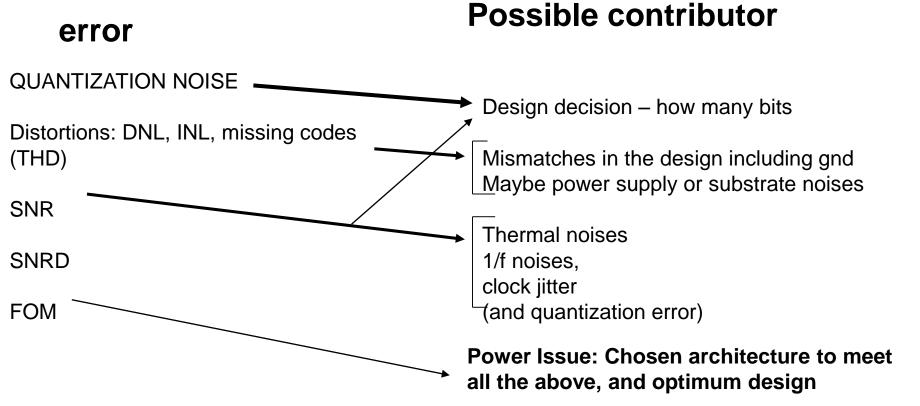


Figure 2.19: INL versus ENOB reduction model

In reality INL of LSB does not means the converter in n bit but more like ~ n-1. 51

Summary



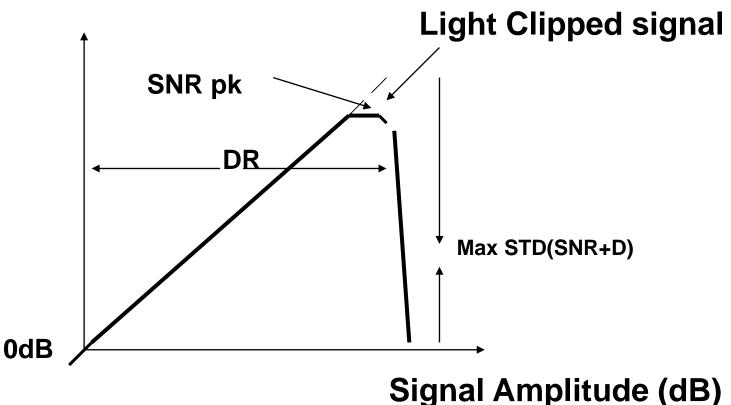




Misc, Added Notes

DR definition = maximum signal/min signal(were its berried in noise) in power.

SNR+D



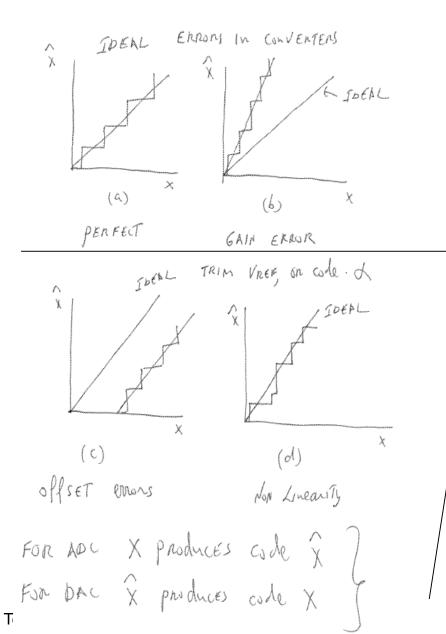
DR may be bigger than SNR Pk DR \ SNRpk

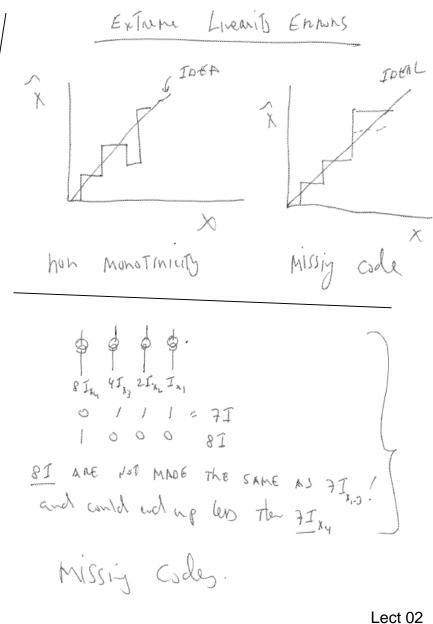
SAMPLING WITH A DELTA FUNCTION



LOOK AT SOME ERROR GRAPHICALY



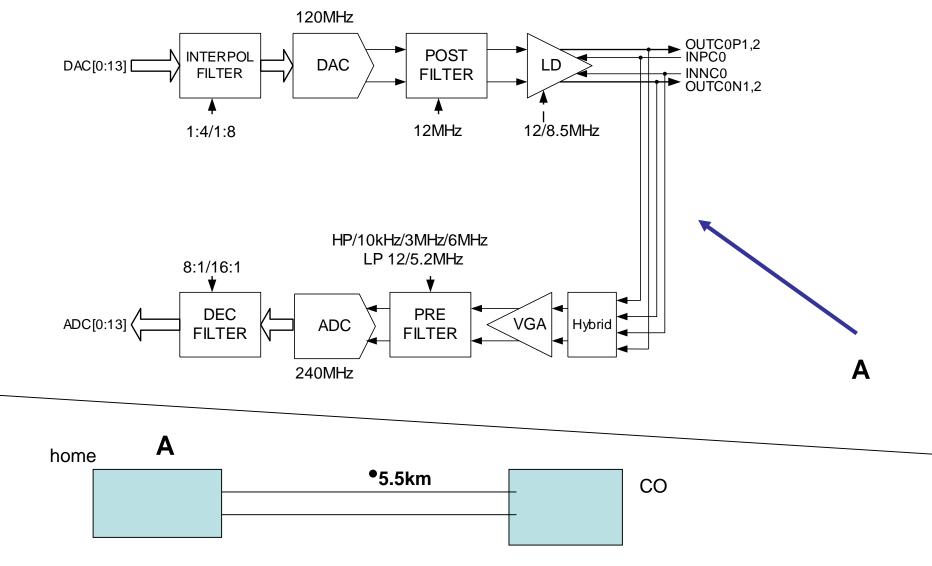


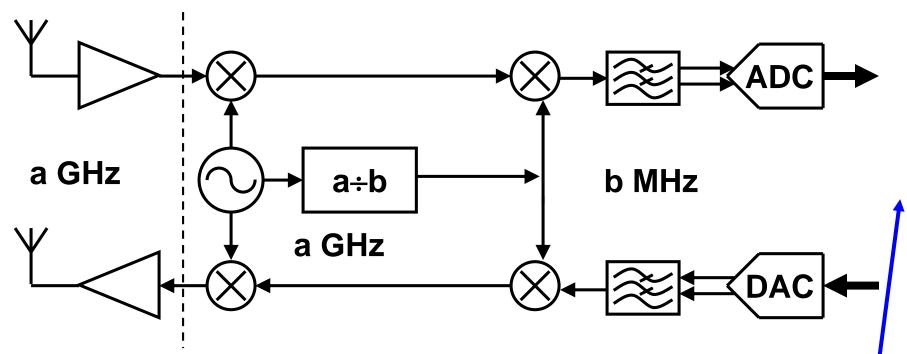


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Example: xDSL AFE Architecture







•Antenna length forces high frequency mod.

Old codecs, voice music.. DSL front ends – multi bit , one bit(CDRs) Wirless ADCs Sensing : X ray detection ultrasounds..

DSP



End lecture 2 (and part of 3)

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