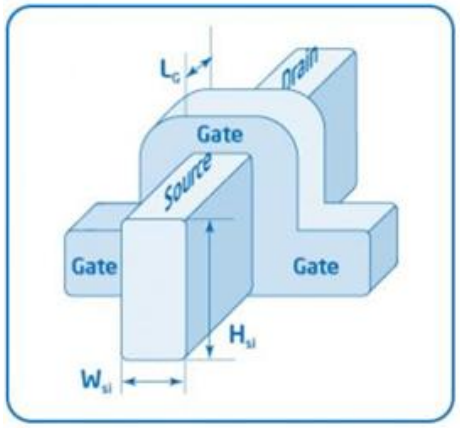

Welcome to

046188 Winter semester 2013

Mixed Signal Electronic Circuits

Instructor: Dr. M. Moyal Room: Meyer 351

Lecture 01

1. Course Overview and Requirements

2. Review of CMOS Transistors Basics

www.gigalogchip.com

You can always find lectures in

www.gigalogchip.com and at the university site.

I will add interesting papers discussions etc..

What will you get out of this course

1. Mixed Signal design – almost all emphasis on Conversion from Digital to Analog and Analog to Digital domains this time – I will add PLLs

2. Basic to detail of Analog circuit (transistor level) design of selected Analog blocks

Understanding of problem flavors and solution/s to mixed signal design

Course lectures

Lecture 1: Overview - Analog Transistors Basics
Lecture 2: ADCs- Basic Theory and Definitions, Jitter
***Lecture 3: Mismatches and noises in Mixed signal IC** circuits.*
Lecture 4: DAC Architectures
Lecture 5: Over sampling Techniques in DACs
Lecture 6: ADC- Flash Architectures
Lecture 7: SAR ADC and Circuit Design of Comparator for ADCs
Lecture 8: High Speed: Pipe lines Just on line lecture.
Lecture 9: Circuit Design of Sample and Hold
Lecture 10: Over Sampling ADCs : Sigma Delta - Loops and Architectures
Lecture 11: Sigma delta Switch capacitors ADCs
Lecture 12: Sigma delta design examples
Lecture 13: Advance topics: PLL Basics or Time interleaved architecture
Lecture 14: PLL design fundamentals

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Home » TextBooks » 046* » 046188 - Mixed Signal Electronic Circuits

046188 - Mixed Signal Electronic Circuits

046188	
Mixed Signal Electronic Circuits	מעגלים אלקטרוניים לאותות מעורבים

1. Plassche, Rudy J. van de. CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters. 2nd ed. Kluwer Academic Publishers, 2003. s.n. 2279785.
2. Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation. Edited by Candy, James C., Temes, Gabor, C. IEEE Press, 1992. s.n. 2117420.
3. Delta-Sigma Data Converters: Theory, Design, and Simulation. IEEE Press, 1997. s.n. 2192320
4. Laker, K. R., Sansen, Willy M. C. Design of Analog Integrated Circuits and Systems. McGraw-Hill, 1994. s.n. 2319855

Course Overview- BOOKS

Perquisite:
Knowledge in Linear Circuits design and Feedbacks systems.

Book Listing: The link below lists the recommended textbooks for your course in the upcoming academic year.
http://libee.technion.ac.il/apage/49599.php

1) CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters by Rudy van de Plassche, 2nd Edition 2003 Kluwer Academic Publishers

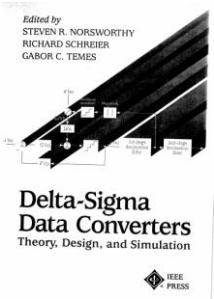
.

2) Oversampling Delta-Sigma Data Converters Theory Design and Simulations. James C. Candy and Gabor C. Temes, 1992 IEEE press Order num. PC0274-1

Book Listing - Option

Design of Analog Integrated Circuits and Systems, Kenner R. Laker and Willy M.C. Sansen, 1994 McGraw-Hill Series in Electrical and Computer Engineering

Recommended Supplemental Material:
IEEE Journal of Solid State Circuits and ISSCC from 1990-2013, and Lecture's notes.



Grading/Site

Course Grading:

Project: 80%

Homework(lab) + Lab 20%

Project Delivery will include 20 min presentation of your work – "oral" exam/presentation

Class Hours:

Room 768 is available for office hrs.

Thursdays. 09:30-11:30., 10 min break.

E-mail: **miki@gigalogchip.com**

The lectures will go on our web site. And the university one

Look at: www.gigalogchip.com

For info on class, class lectures, notes, project papers, etc..

Requirements: Project

I will choose few projects ideas for you to work on. You may, under special case bring your idea but it will need to be approved by me.

Area Topics Area Suggestions:

Design of : ADC: (Sigma Delta, Flash, SAR,PLL)

I will define “spec” : Bits/frequency/Process/voltage range/Power

..and in LAB: Per Danniel → Design a DAC.

Project Detail: Choose A to E

You will deliver: (detail on a separate doc)

a) Paper Search: What exists today – at least 3 paper listing.

b) Architecture Analysis (can be Matlab/AnaLib sim.) – show that it works

c) Mismatch Analysis add imperfections ---show that it works.

d) Circuit Simulation/design: Transistor Simulation one block contain transistors

A) 5 bits 1GS/s FLASH ADC → ENOBS=4.4bit

B) 12 Bits 2MS/s Sigma Delta ADC → ENOB=11bit

C) 6 bit 8GS/s Interleaving ADC → ENOB=4.8bit

D) 12 bits 1MS/s SAR ADC → ENOB=11bit

E) 4GHz PLL bw=2MHz refin=25MHz
Sim vco phase noise
Propose all elements of filter and phase detector and charge pump.

details : next lecture….

Cadence issues: to do simulations

At the university we have a workstation with Cadence and a general 90nm PDK.

You can open accounts on that machine and connect using VNC.

Danniel is also coordinating the dates for Cadence instructions on basic operation of Cadence (schematics, layout, simulation).

Students without Cadence background should be encouraged to participate but we need to know in advance.

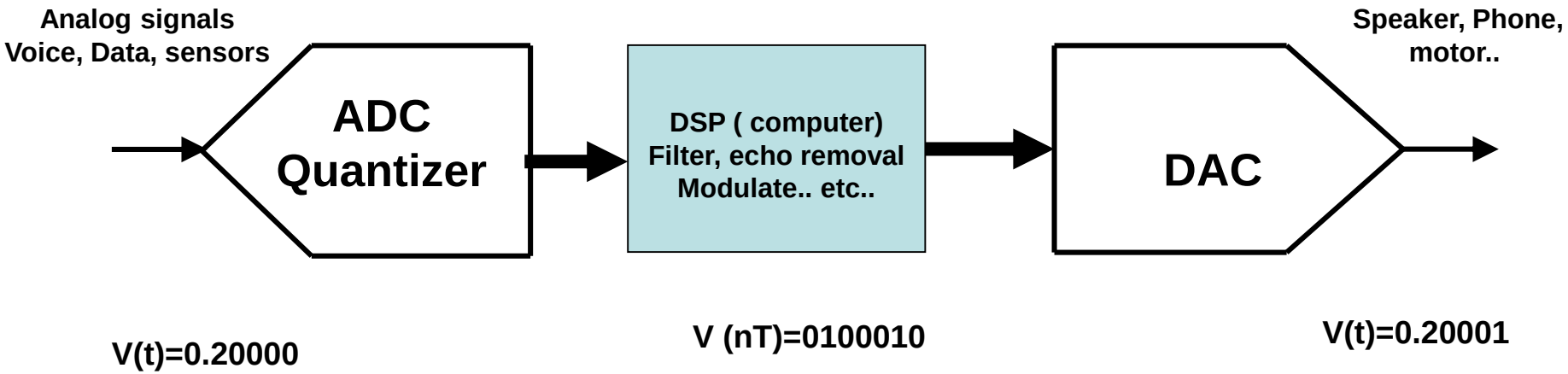
We also have Matlab liscence. :

Review

Example of Mixed Signal Systems

Review of CMOS Transistor Basics

Converters



ADC –> DSP –> DAC

It's a "Language" translator to do work. With fixed known boundary conditions **Vinmax and Minmin, clock, maximum frequencies of through put,**

The process burn power, produces inaccuracies, creates bad artifacts- Folding, distortions - but allow communications to exists and to be stored.

In this course we will learn how converters operate and how those errors are generated. And more precisely why/when we can let the error exists.

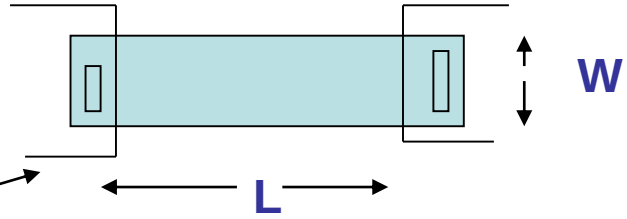
1. Quick Review of Silicon based passives elements

2. Review of CMOS Transistor Basics

Silicon Resistors:

In Silicon **R** = Sheet resistance x Number of square. ~ 6 ohm-1 Khom/square

$$R = Rs \bullet squares(1+\alpha T/To)$$



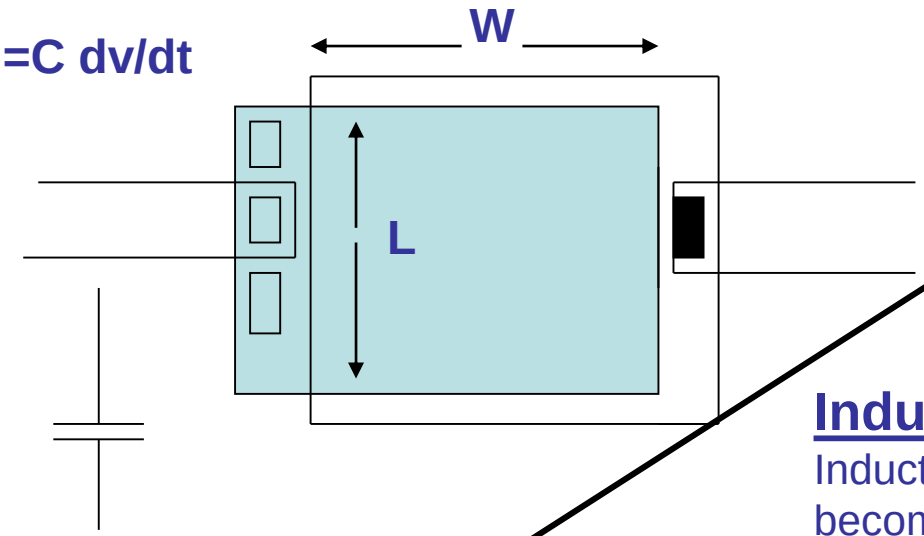
Si Top view

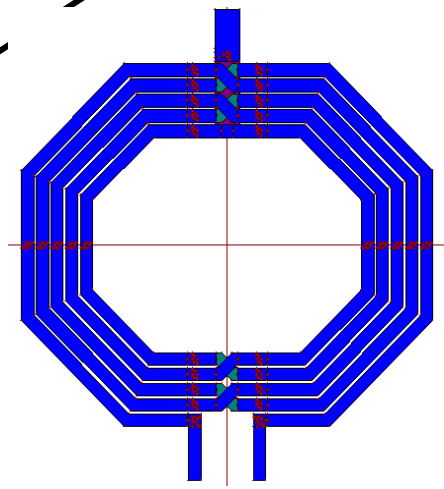
R=v/i

Capacitors

C= Ca x Area = Ca x W x L (W and L are dimension of plates)0.1-4 ff/uu

i=C dv/dt





Inductors

Inductors are also becoming a elements-

$$L_{self} = \frac{\mu_0}{2\pi}\left[l \ln\left(\frac{2l}{w+t}\right) + \frac{l}{2} + 0.2235(w+t)\right] \quad (1)$$

Transistors : (CMOS in this example)

4 terminal device, mostly 3 terminals are used, the 4th is default connection - not always.

CMOS works so nice because it is possible to build and repeat it: It is an efficient and dense element (~**1.6million/mmsquare in 45nm tech**.)

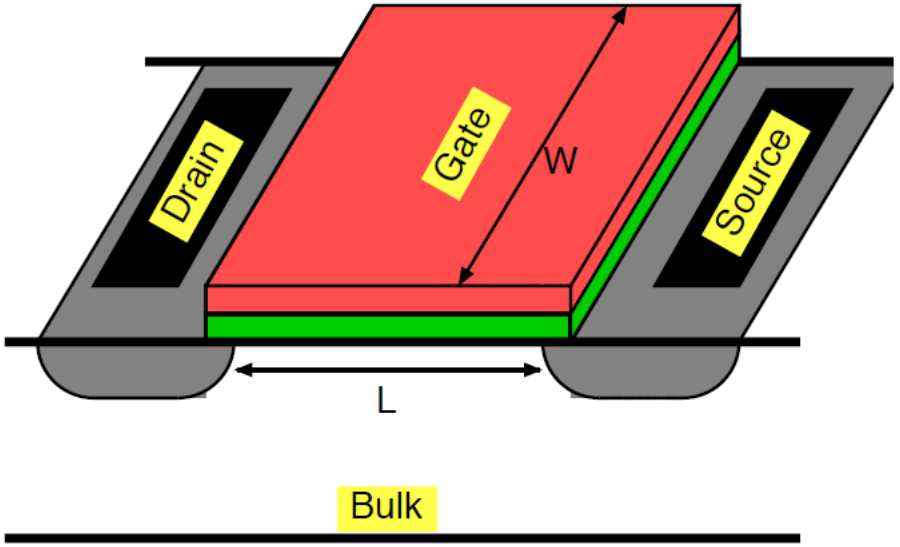
Transistor can change its “function” and become R , C , or a voltage controlled current source(VCCS). Applying mostly the control voltage to the gate to source voltage.

Key is to understand which control does what !

ids=f(Vgs,Vds,W,L,Vt,U,Cox)+noise

CMOS Transistor Basics

- General MOS structure
  - W: channel width
  - L: channel length
    - G=Gate; D=Drain; S=Source, B=Bulk
  - S & D are doped p or n
  - B is oppositely doped (n or p)
    - doped p: excess of holes, positive charges;
    - doped n: excess of electrons, negative charges;

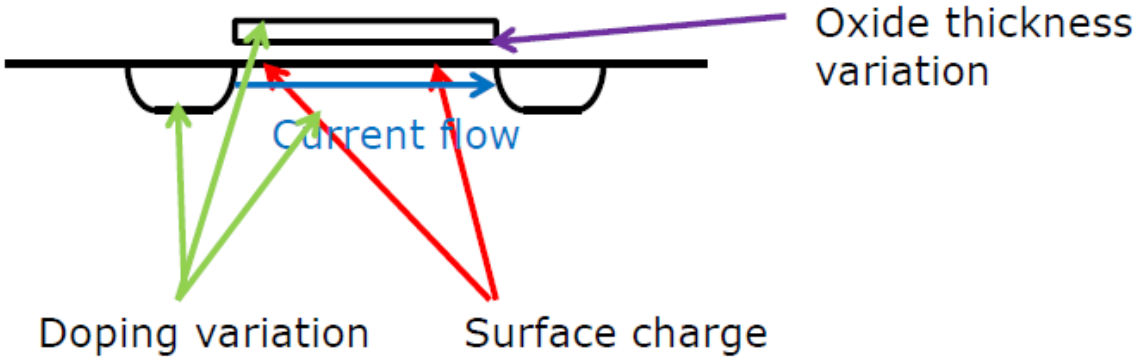


- ➔ S/D with n doping, B with p doping == NMOS device
- ➔ S/D with p doping, B with n doping == PMOS device

A Baschirotto LV analog design 2011

In most case…nothing happen until you (VGS) pass the "Vt"

CMOS device characteristics



- $V_{T0}=kT/q(\ln(N_D*N_A/n_i^2)+\ln(N_A/n_i)-Q_b/C_{ox}-Q_{ox}/C_{ox}$
- $V_T=V_{T0}+\gamma*\mathrm{sqrt}(V_{sb}+2\Phi_F)-\mathrm{sqrt}(2\Phi_F)$
- V_T depends to first order on doping and oxide thickness, both of which have tolerances.
- The larger the area the more consistent the value, the less variation -> inverse proportional to root of gate area

CMOS Transistor Now and Future look

smaller and smaller L < 25nm: New transistors L is a " Figure of Merit" not really 25nm

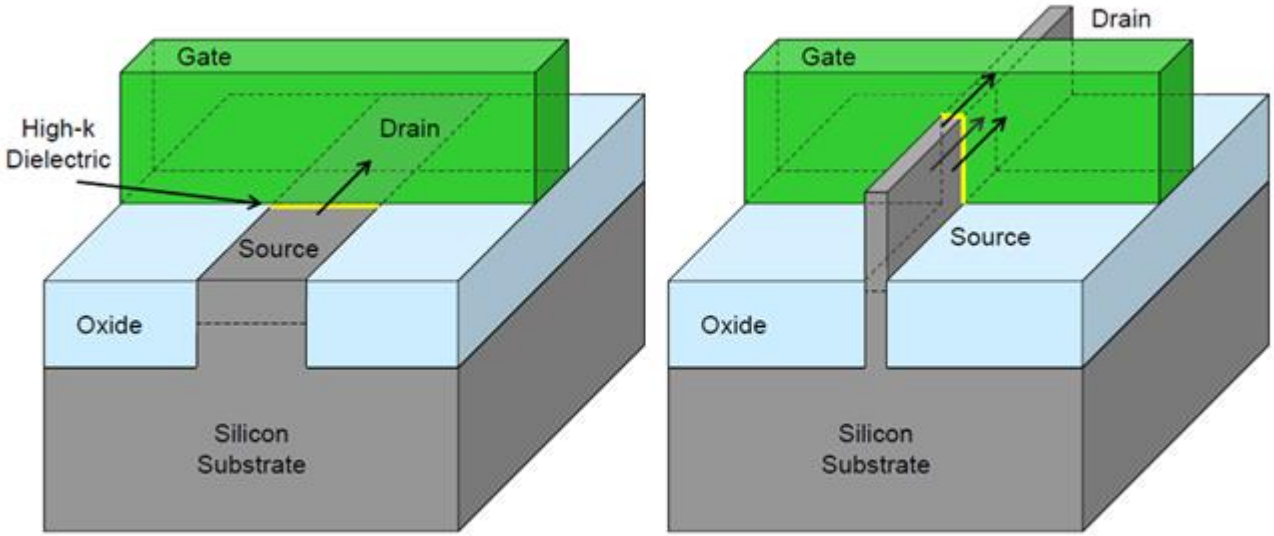


Figure 1 – Planar and Tri-Gate FinFETs, courtsey of Intel

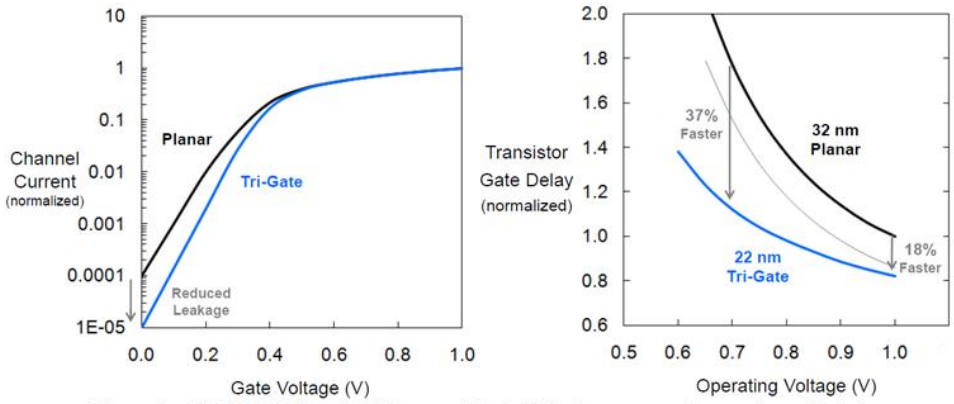
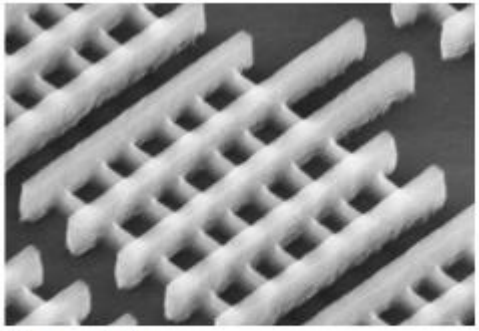


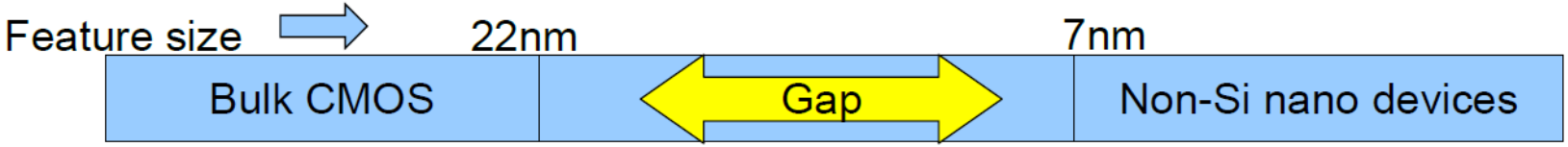
Figure 2 – FinFET Sub-threshold Slope and Gate Delay Improvements, courtsey of Intel



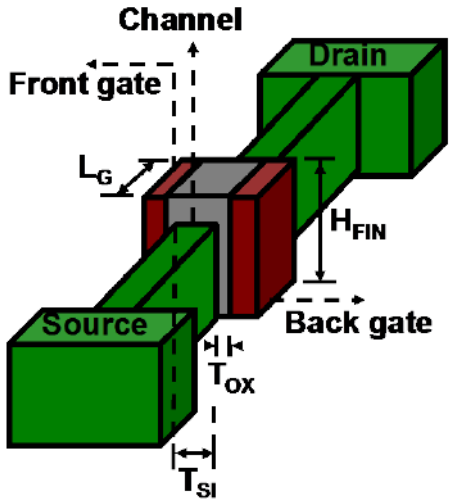
Source: Intel

http://www.realworldtech.com/intel-22nm-finfet/

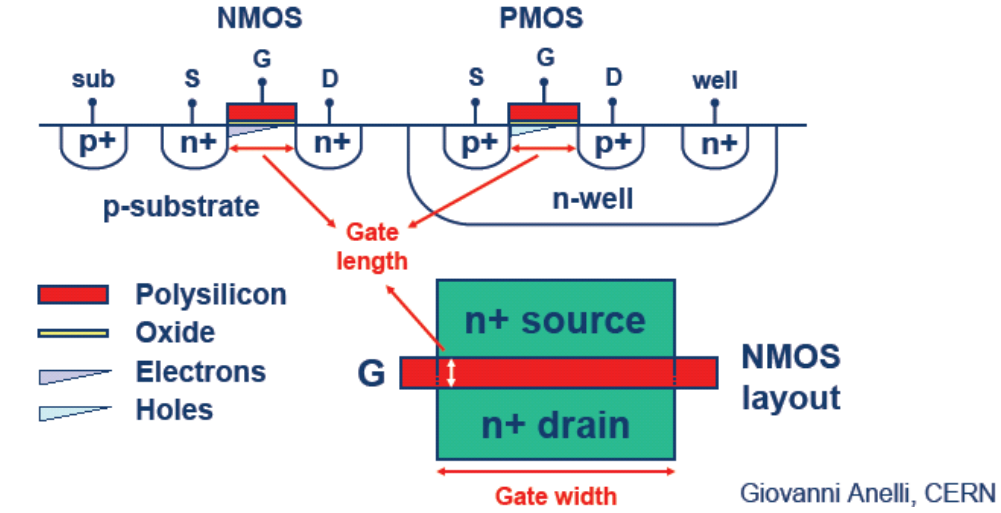
Why FinFETs?

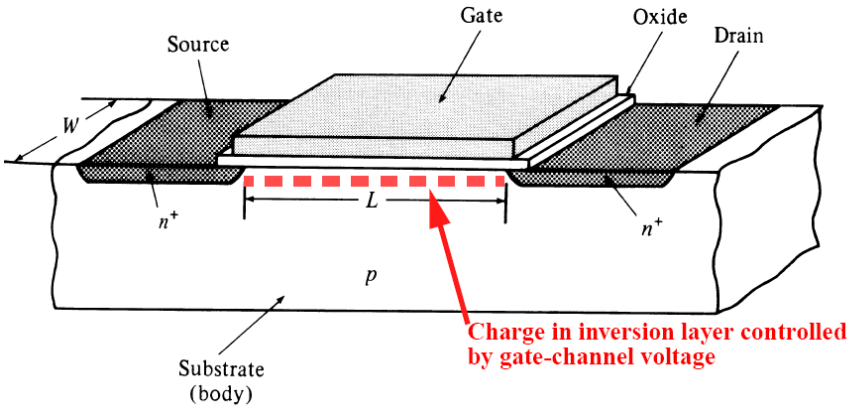


- FinFETs expected to continue transistor scaling to 7nm
  - FinFET fabrication compatible with CMOS process
  - FinFETs address scaling challenges faced by bulk CMOS
    - Better channel control with double gates ➔ reduced short-channel effects
    - Improved subthreshold slope
    - Better Ion/Ioff
  - Different styles
    - Shorted-gate (SG)
    - Independent-gate (IG)
    - Asymmetric-workfunction SG (ASG)



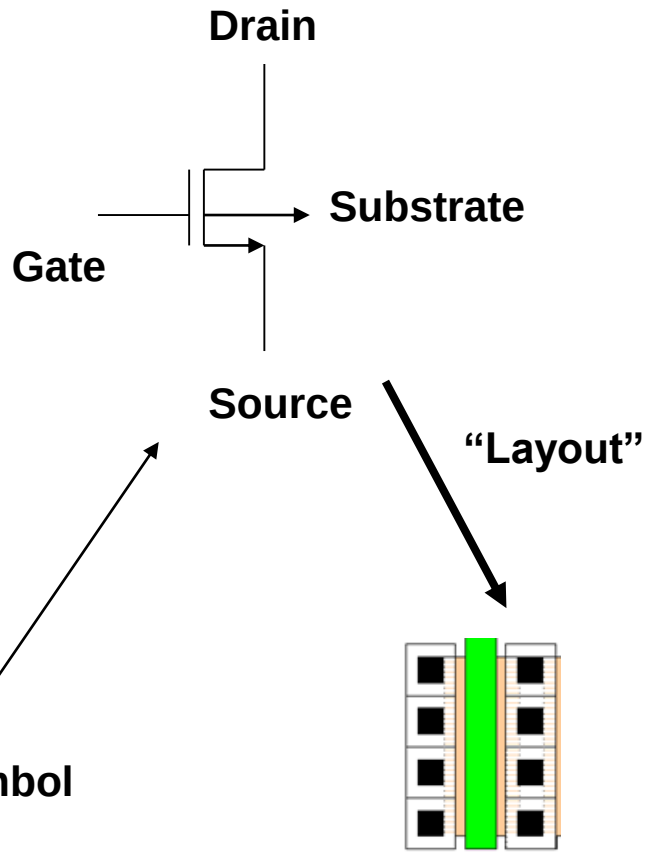
Physical Structure of Nmos / Pmos transistor





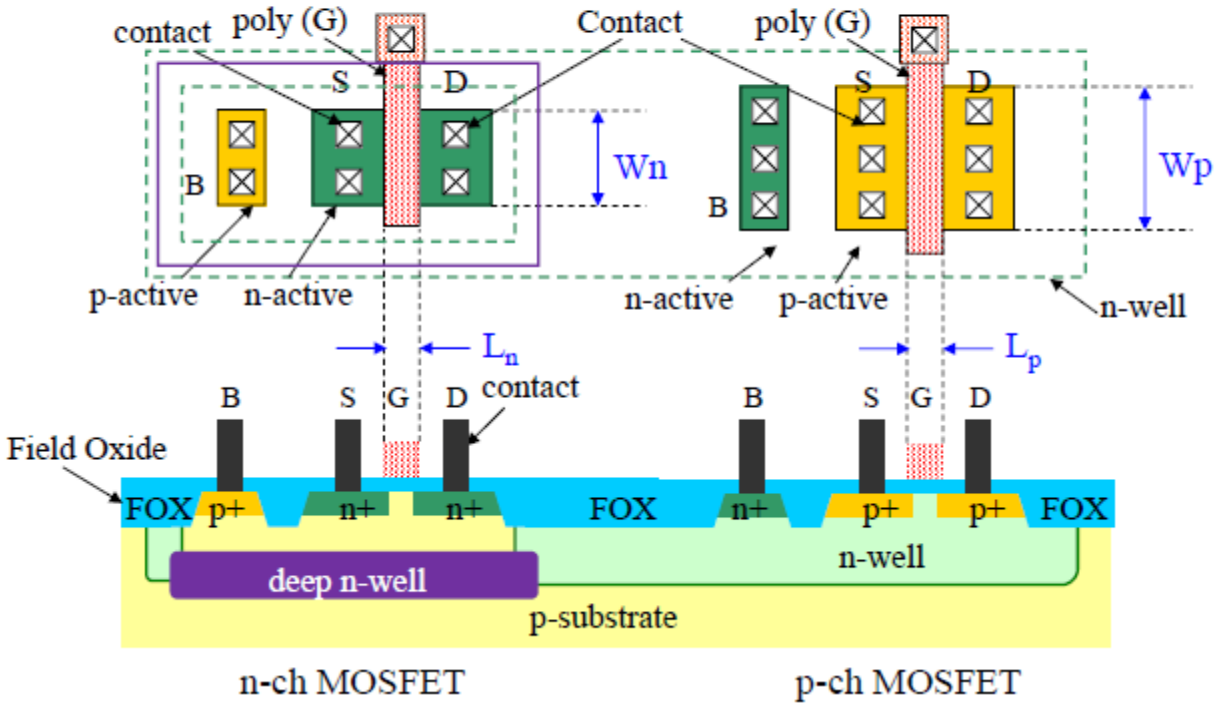
Source: IEEE & T.H. Lee.

How do we define
W , L , Multiplier, Finger..



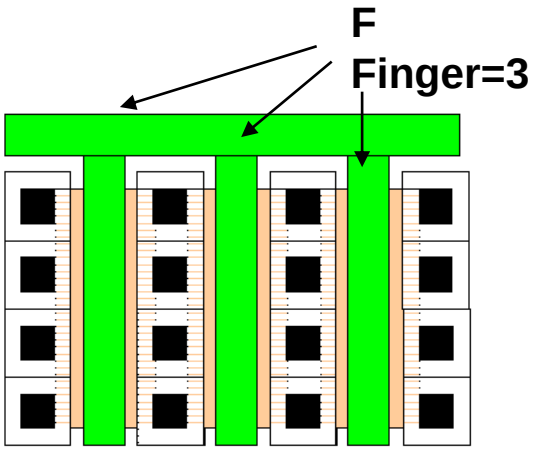
Possible to add n channel floating..

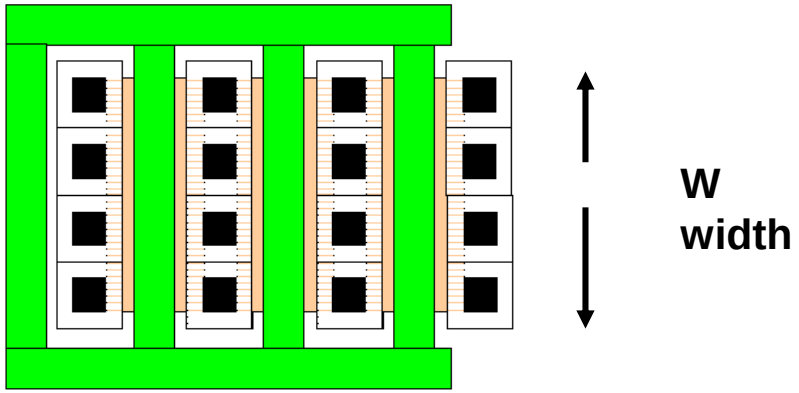
Layout and cross section (Triple well)



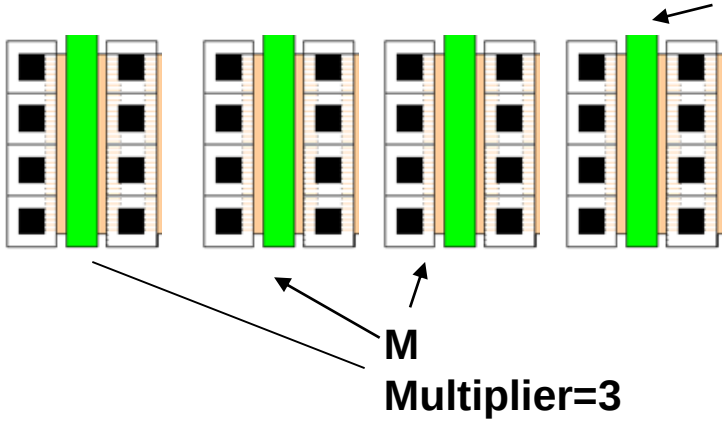
Transistor Placement → layout

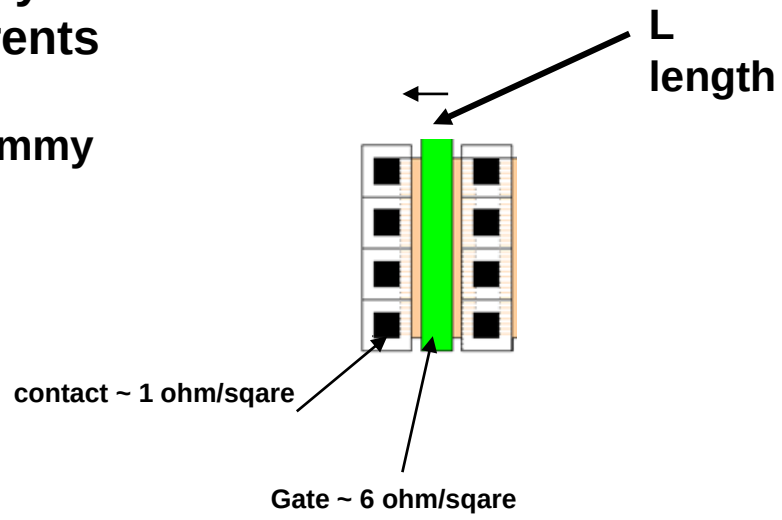
a very important part of mixed signal is placement and layout of the elements.



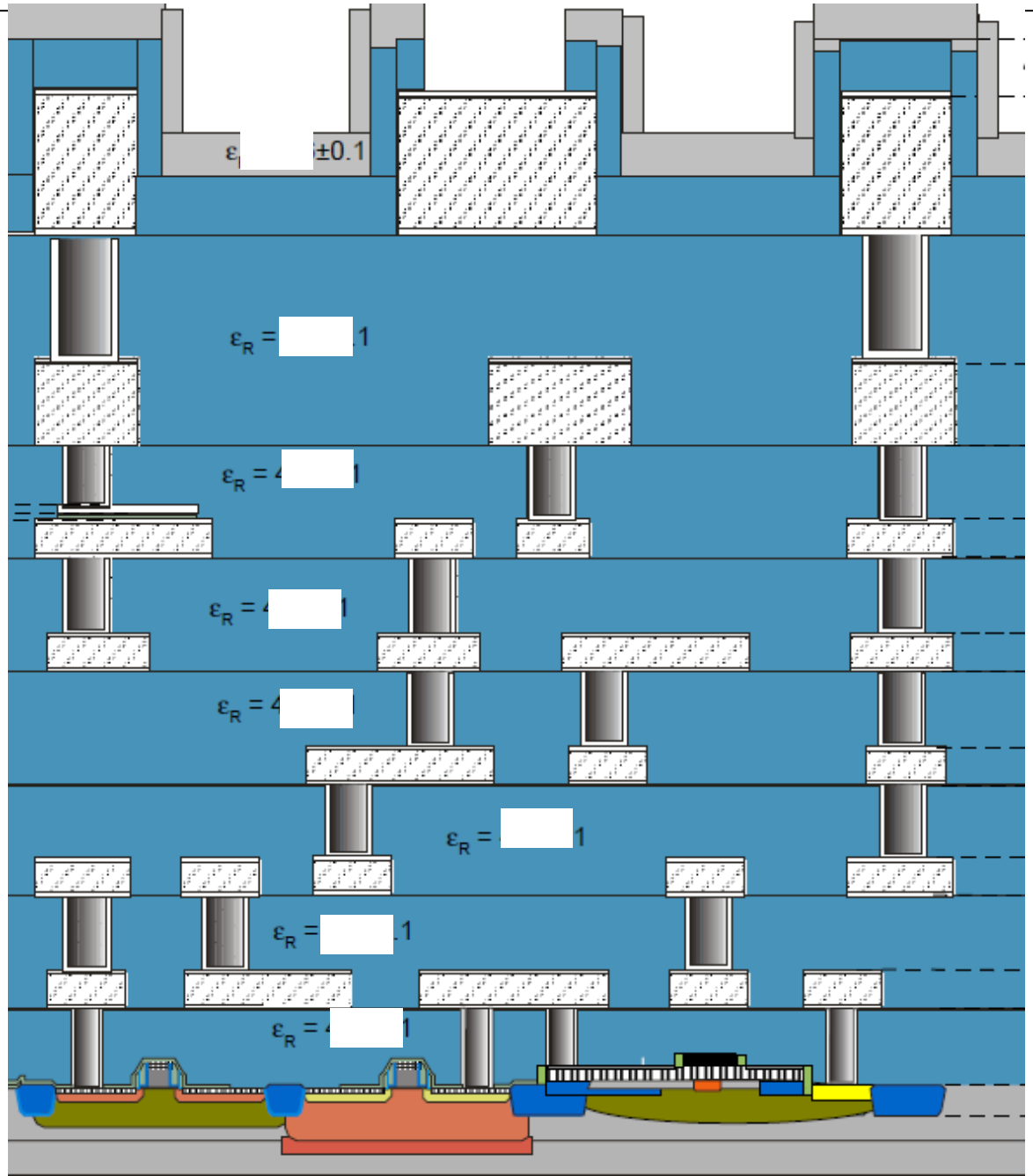


now we have added errors: contacts resistance, metal routings and capacitance they can make difference at high frequency and at high currents





Example: Metallization placement in Silicon



Large Signal Equations for Nmos/Pmos transistor

Linear Region - A “resistors”

Strong Inversion - A current source (v-c-c-s)

Moderate Inversion – “transition region”

Weak Inversion - A “bipolar device” (Exponential i/v)

Off (Accumulation) - Open Switch

Velocity saturation, and Breakdown regions ! –important in sub um logic devices..!

Example:
A “digital cell” transistors could switch through all those regions

Linear Region

Linear Region the drain current is mobility time electric field (surface)

$$I_D = -WQ_n(y)\mu_n E$$

$$\int_0^L I_D dy = I_D L = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{GS} - V(y) - V_t] dV$$

Source: IEEE & T.H. Lee.

$$Ids = \mu Cox(W/L)[(Vgs-Vth)\cdot Vds - 1/2Vds\cdot Vds] \qquad Vgs-Vth > Vds$$

In this region electron are attached to the surface creating a conductive surface R Which is Vds dependent (for small Vds)

Mobility: how a charge carriers responds to an induced electric field, the mobility in Silicon MOSFET is roughly 400 cm2/Vs

Saturation Region

IF ***Vgs -Vth<Vds*** and ***Vgs -Vth>3KT/q~78mV***

Then: $$I_D = \frac{\mu \cdot Cox}{2} \cdot \frac{W}{L}(V_{GS} - V_T)^2 = \frac{\beta}{2}(V_{GS} - V_T)^2$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L}$$

Or we can define ***Vgs -Vth≡Vdsat***

Strong Inversion region
The inversion channel does not extend all the way to the end
"pinched off"

Key: Keep Vdsat ~130mv or more

Strong Inversion, large Vds, transistor do not respond to drain movement – Great place to make a current element or to make an amplification… or an ADC, DACs

$$V_{TH} = V_{THo} + \gamma \cdot \left[\sqrt{|-2 \cdot \Phi_F + V_{SB}|} - \sqrt{2 \cdot \Phi_F}\right]$$

$$\gamma = \frac{\sqrt{2 \cdot q \cdot \varepsilon \cdot N_A}}{C_{OX}}$$

Vt= Threshold voltage require to produce conducting channel at Drain Source.

In most design, to keep the transistor in saturation we always watch for Vdsat, and keep in mind that Vdsat is sould be lower than Vds.

Summary table

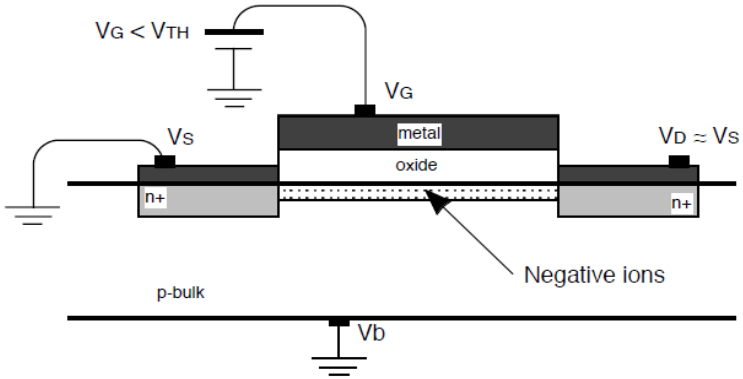
Linear region	$V_{GS} > V_{TH}$	$V_{DS} < V_{GS} - V_{TH}$
	$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right]$	
Saturation region	$V_{GS} > V_{TH}$	$V_{DS} > V_{GS} - V_{TH}$
	$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$	

Weak Inversion (sub threshold) Region

IFF $Vgs - Vth < 3KT/q \sim 78mV$ $Vds > 4KT/q$

Then:

$$Ids = Ido(W/L)e^{Vgs/(nKT/q)}$$



Key: when-→Vgs~Vth

Can happen at any Vds (above ~ 100mv)

Transistor is Very large or has very small current !

Slope: ~70mV per decade of current

n (sometime k) is called kappa around 0.7 and represents the coupling of gate to source potential

n = cox/(cox+cdepl)

Other Regions

Moderate Inversion Vgs-Vth ~30-50mV (same as Sub threshold)
(transition place)

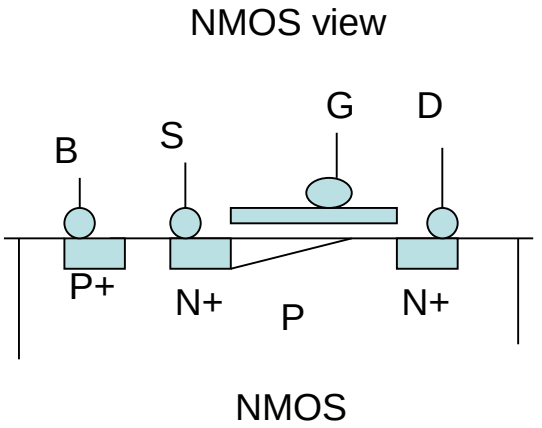
Off region: Vgs~0 (leaky region) Idss, and Igate

Mobility saturation: Large Vgs-Vth ~V supply or more.

Snap back: Very large Vds exceed supply, a bipolar action

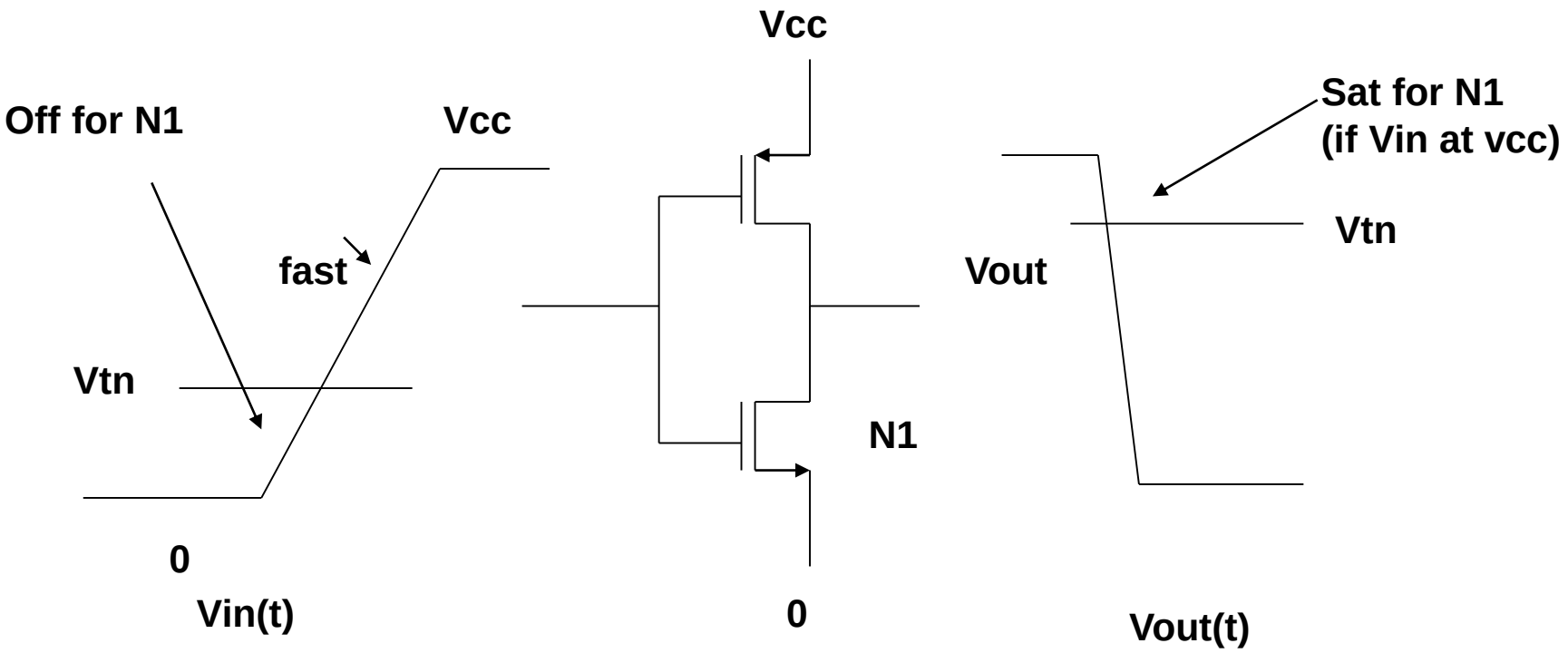
Off region is interesting design parameter

it's a function of how big is Vth ! And all leakages of all parasitic diodes



Source: IEEE & T.H. Lee.

Inverter example



Example: In class analysis..
An inverter will switch through all those regions

But in most Analog/Mixed signals most transistors will stay in one region or will switch from Off to one of those region.

CMOS: the small signal model

To convert the transistor to passive and active elements.

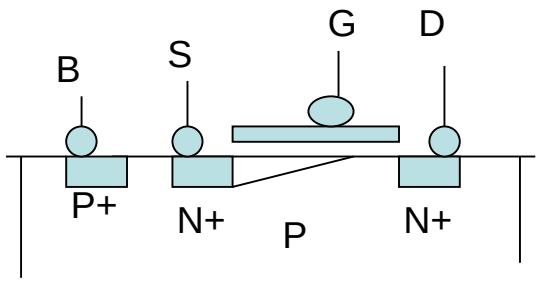
Mathematically :
Use “differentiation” to model it into another linear region.. CMOS , Bipolar any….type..

$$gm \equiv \partial Ids / \partial Vgs$$

$$gds \equiv \partial Ids / \partial Vds$$

$$gmsb \equiv \partial Ids / \partial Vsb = \eta \bullet gm)$$

NMOS view



Small Signal Transistor Parameters: Gm

Lets take the saturation region and assume the transistor Vgs-Vth does not change a lot. The current is set DC - but fluctuate as we 'slightly' (small signal) move the Gate voltage.

Its important because the "quality" of the transistor in term of amplifications and output impedance is measured. (ignoring gmsb)

$$Vgs - Vth < Vds$$

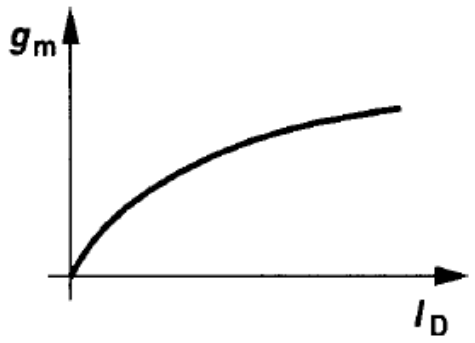
$$Ids = \mu Cox(W/2L)(Vgs - Vth)^2$$

$$gm = \partial Ids/\partial Vgs = \mu Cox(W/L)(Vgs - Vth)$$

$$\boxed{gm = \sqrt{2\mu Cox(W/L)Ids}}$$

$$\boxed{\Delta Ids = gm \bullet \Delta Vgs}$$

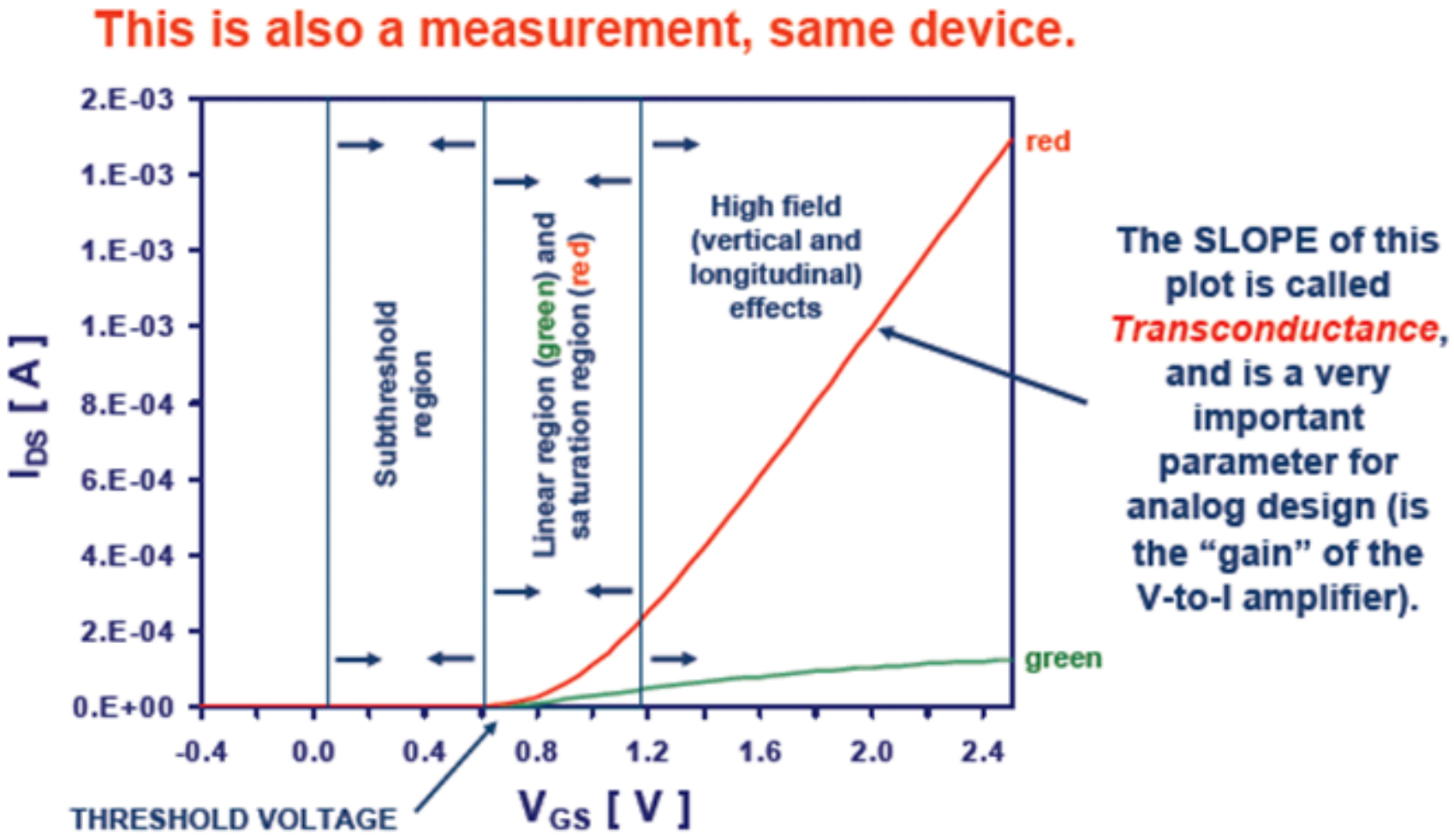
we want large gm but it cost: Squaring the Ids. W up and small L helps



W/L Constant

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}.$$

Example: IDS Vs. VGS



gm ~ 400e-6 is a typ number..

Small Signal Transistor Parameters: Gds

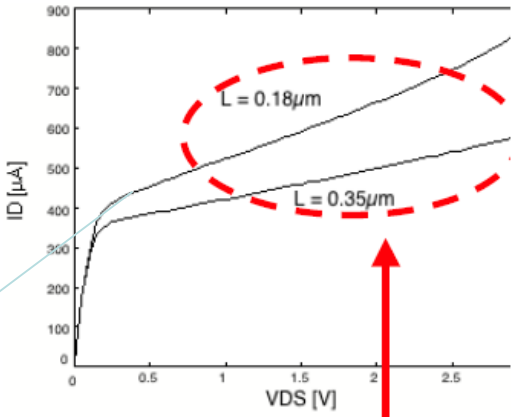
Vgs -Vth<Vds

At a fixed Vgs, Ids is not constant in term of Vds (replace sat current equation with- channel modulation

$$Ids = \mu Cox(W/2L)(Vgs-Vth)^2(1+\lambda Vds)$$

$$gds = \partial Ids/\partial Vds \equiv 1/ro$$

$$gds = \lambda \bullet \mu Cox(W/2L)(Vgs-Vth)^2 = \lambda \bullet Ids$$



- High-impedance
  - Gain stages

Key: $V_A, r_o \propto L$ for long-channel devices

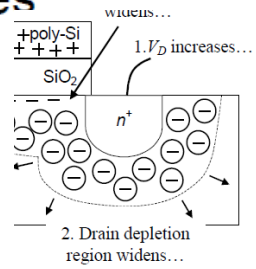
ro proportional to L ! And 1/Ids

Slope: 1/ro ! Lambda ~ empirical…(proces $r_{ds} = \frac{L}{\lambda' \cdot I}$

Make long L if you like big ro !

Large ro means current is unaffected w. vds changes

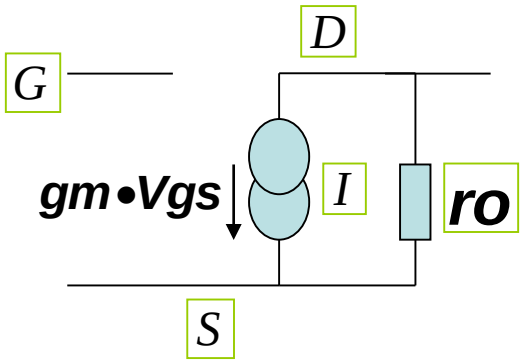
and..**Low I good (high) ro..**



$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}).$$

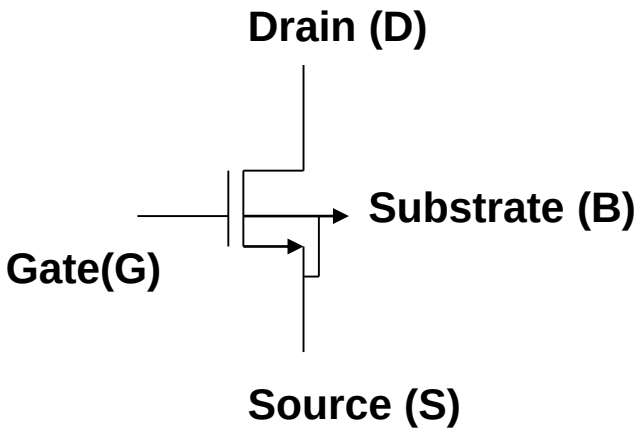
$$= \sqrt{\frac{2\mu_n C_{ox}(W/L) I_D}{1 + \lambda V_{DS}}},$$

in Sat-Model for small signal (no capacitors-DC)



Model

in small signal model Vgs, ids, ro, gm all are derivatives.. saturation



$$gm \equiv \partial Ids / \partial Vgs$$

$$ids \equiv gm \bullet vgs$$

$$gds \equiv \partial Ids / \partial Vds$$

$$ro = 1/(\lambda \bullet ids)$$

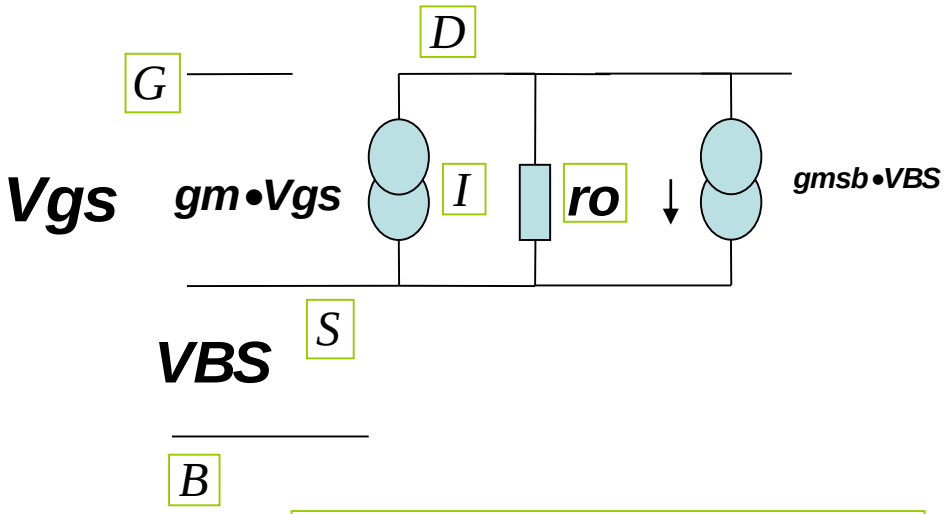
Small Signal Transistor Parameters: Gmsb

gmsb (an additional gain path)
Because Vt changes as a function
of source to baulk:
(See Vth equation)

In many cases to avoid this gain path it is good to tie source to baulk !

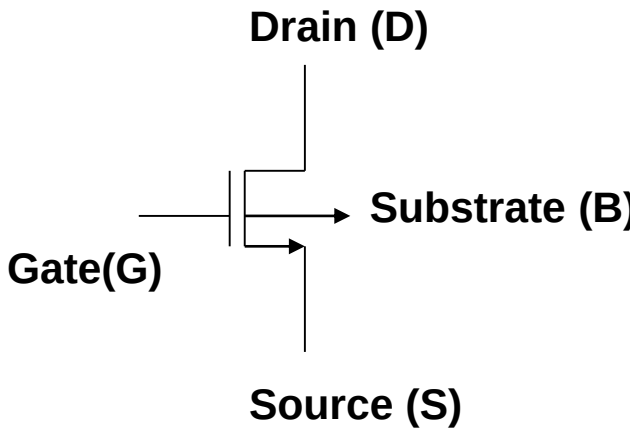
$$V_t = V_{t0} + \gamma \cdot \left(\sqrt{2 \cdot \phi_f + V_{SB}} - \sqrt{2 \cdot \phi_f} \right)$$

$$\frac{gmb}{gm} = \frac{\gamma}{2 \cdot \sqrt{2 \cdot \phi_f + V_{SB}}} = \chi$$



Model – with _baulk

$$gmsb \equiv \partial Ids / \partial Vsb = \eta \bullet gm)$$



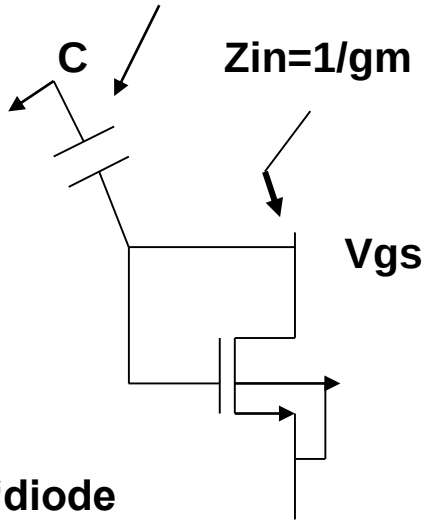
η

is In the range of 0.2 gm (every technology has an n)

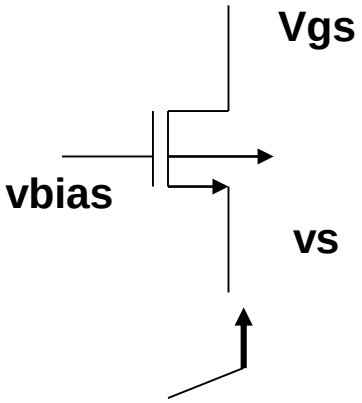
Convince yourself..

Use the small signal model derive the impedance of n channel transistors below.

And what about C



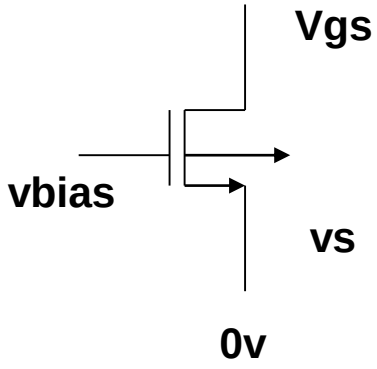
“low Z”

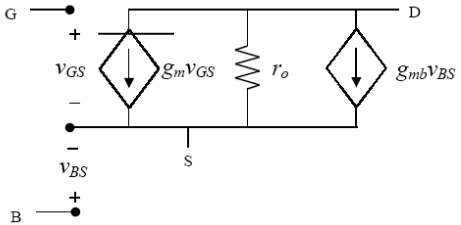


Zin=1/(gm+gmsb)

“high Z”

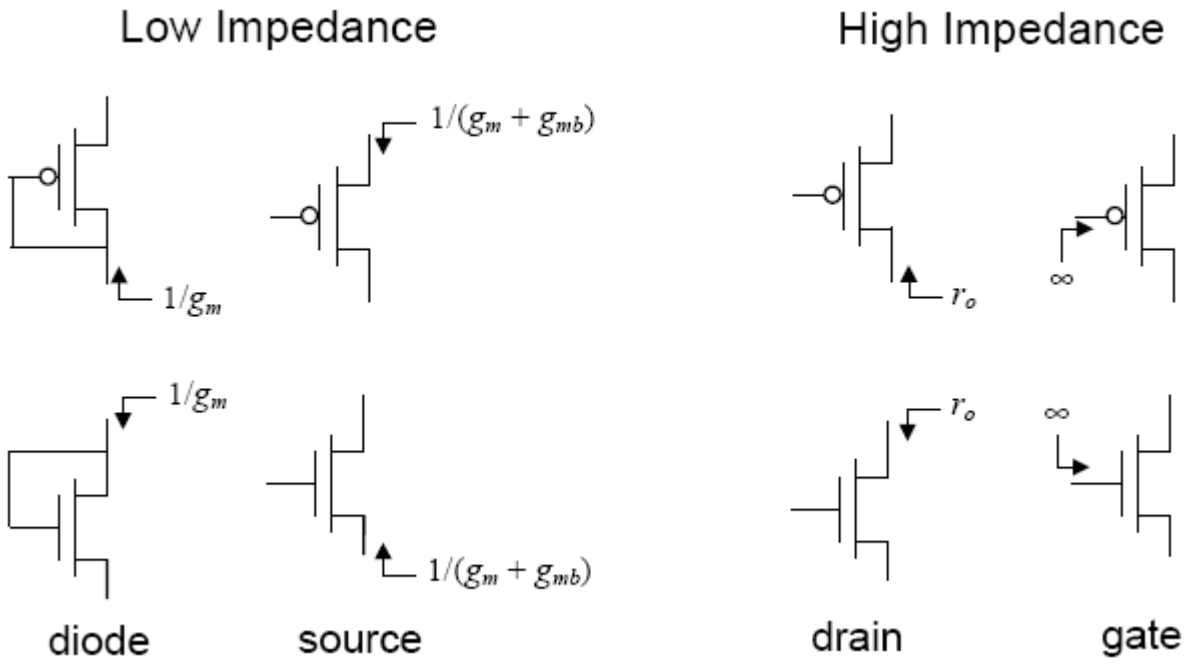
Zin=1/(gds)





Example : Transistor impedances:

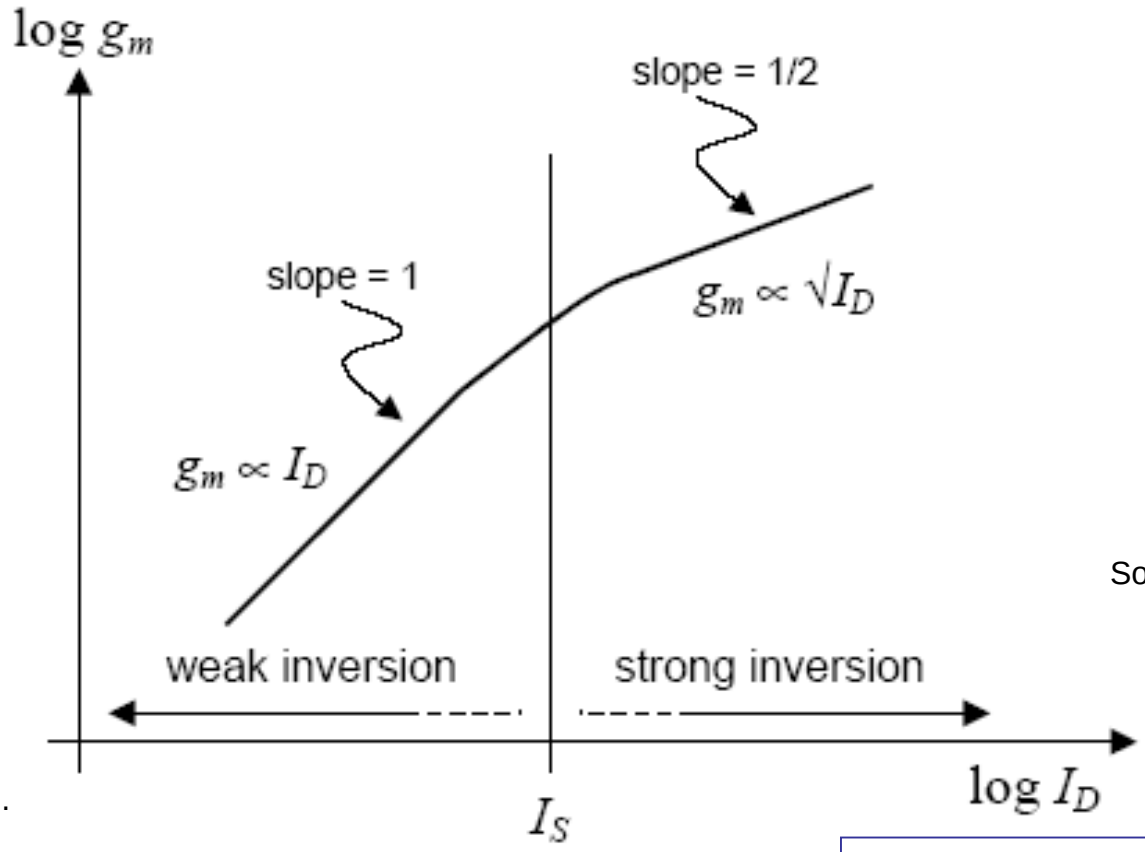
MOS is a source device you move the drain nothing happen at the source but once you move the source the drain follow with gain!
In Nmos source potential is lower than the drain
And.. You can exchange source and drains- symmetrically.



Source: IEEE & T.H. Lee.

Gate impedance in thin gates is not infinite
Ig is becoming significant for L below ~ 65nm. (thin oxide) conventional CMOS

How gm behaves with at different regions



Source: R Harrison, Uof Utah

Source: R. Harrison.

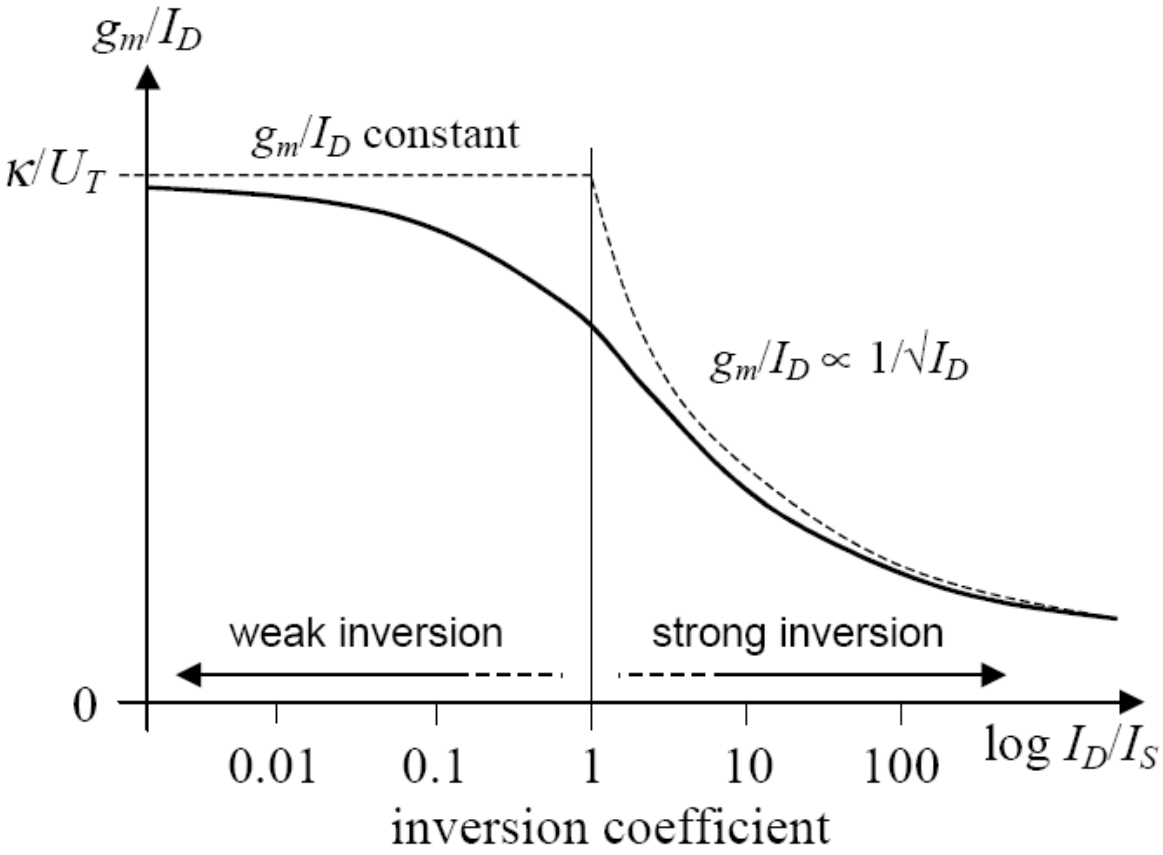
Key:
Gm increases faster in weak inversion
In moderate Vds=30-80mv – gm = ~ Ids
Small absolute gm -.slow device

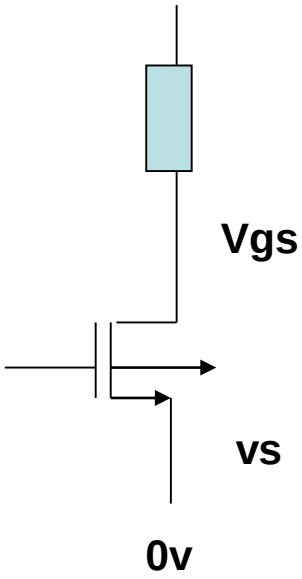
$$gmsat = \sqrt{2\mu Cox(W/L)Ids}$$

$$gmwk\_inv = Ids/(KT/q)$$

Gain => gm x ro

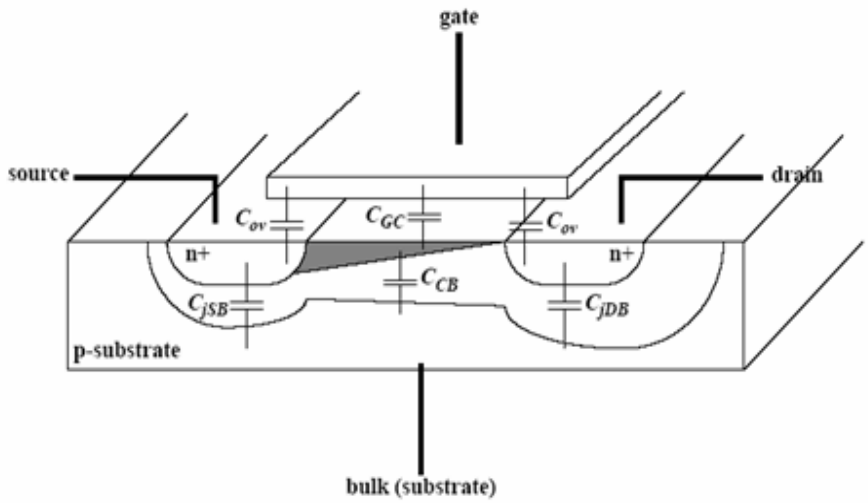
Another look is relative gm defined as gm/Ids (for low I design)
But also the “gain” is **gm ro = ~gm/Ids**

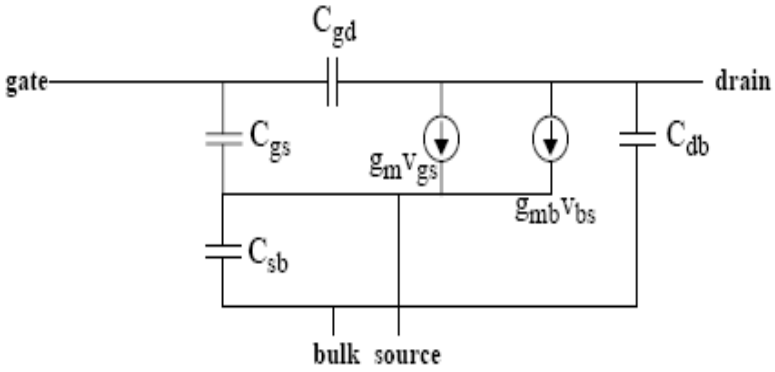




Source: R Harrison, Uof Utah

Capacitor of CMOS





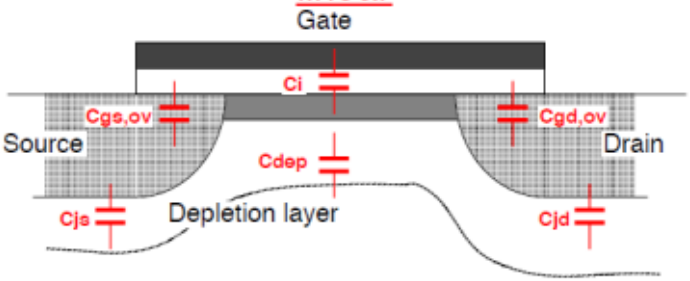
capacitors	Saturation	Linear	Off	
C gate to S	2/3Cox+Cov	1/2Cox+Cov	Cov	
C gate to D	Cov	1/2Cox+Cov	Cov	
C gate to B	0	0	Cox//Ccb+..	
C drain to B C source B	Cj(diode) CJ	Cj Cj	Cj CJ	Voltage dependance

Source: IEEE & T.H. Lee.

Basic MOS Transistor operation

Small Signal Equivalent Circuit –Capacitances

linear



$$C_i = C_{ox}\,WL$$

$$C_{dep} = \frac{\varepsilon_{si}}{x_{dep}}\,WL$$

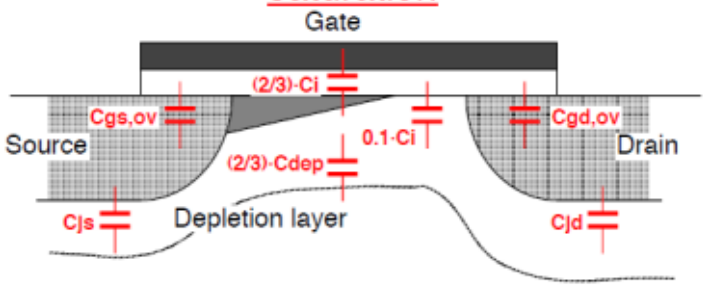
$$C_{gs} = C_{gs,ov} + \frac{C_i}{2}$$

$$C_{gd} = C_{gd,ov} + \frac{C_i}{2}$$

$$C_{sb} = C_{js} + \frac{C_{dep}}{2}$$

$$C_{db} = C_{jd} + \frac{C_{dep}}{2}$$

saturation



$$C_{gs} = C_{gs,ov} + \frac{2}{3}\,C_i; \qquad C_{gd} \cong C_{gd,ov}$$

$$C_{sb} = C_{js} + \frac{2}{3}\,C_{dep}; \qquad C_{db} = C_{jd}$$

$$C_{gb} \cong \frac{1}{10}\,C_i$$

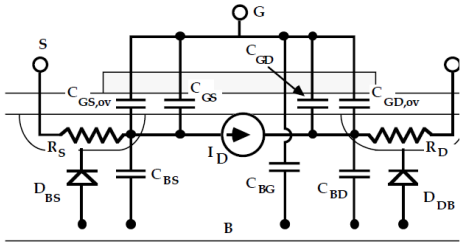
$$C_j \cong \frac{C_{j0}}{\sqrt{1 - \frac{V}{\Phi_T}}}$$

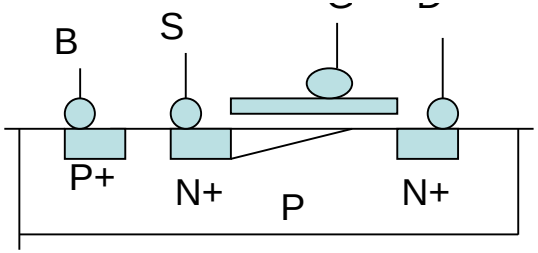
$$\Phi_T = \frac{kT}{q}\,\ln\left(\frac{N_D\,N_A}{n_i^2}\right)$$

CMOS Model – never forget the Parasitic Bipolar/diodes !

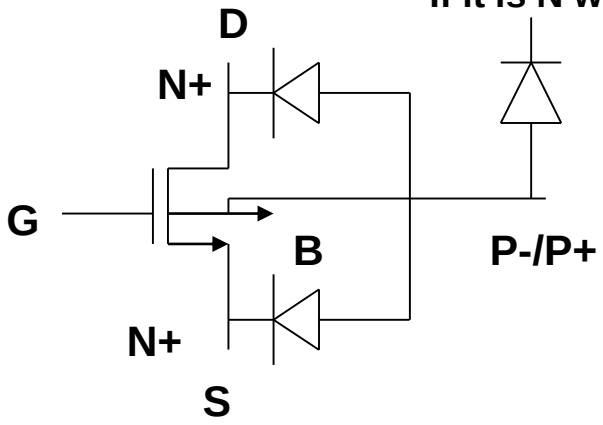
$$I_{GR} = A \cdot \frac{Q \cdot n_i \cdot x_j}{2 \cdot \tau_o}$$

- A : area of the junction
- x_j : depletion region width
- τ_0 : mean lifetime for minority carriers
- I_{GR} doubles for an increase of ≈10K
- At room temperature $I_{GR}/A=10^{-15}A/\mu m^2$

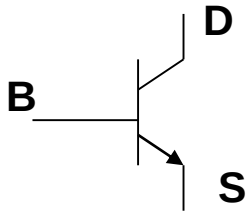




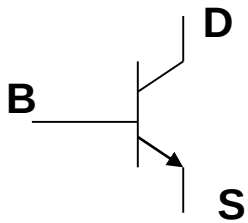
May exist
For sure in Pch
If it is N well process



Lateral



Vertical

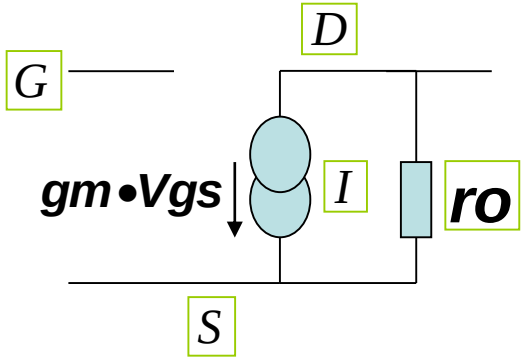


May exist
For sure in Pch
If it is N well process

Summary

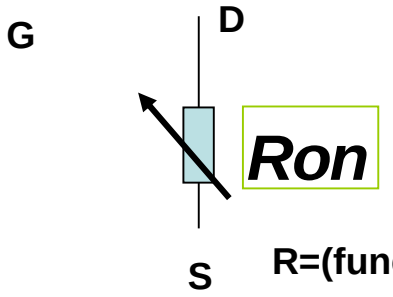
Saturation

$$Ids = \mu Cox(W/2L)(Vgs-Vth)^2(1+\lambda Vds)$$



Linear

$$Ids = \mu Cox(W/L)[(Vgs-Vth)\cdot Vds-1/2Vds\cdot Vds]$$



R=(function of vgs,vds)

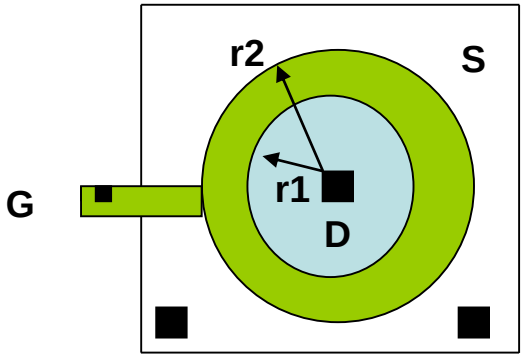
Sub Threshold

$$Ids = Ido(W/L)e^{Vgs/(nKT/q)}$$

"Rule of thumb" : 70mv/dedade of I

Now add capacitance according to
Mode of operation on table provided

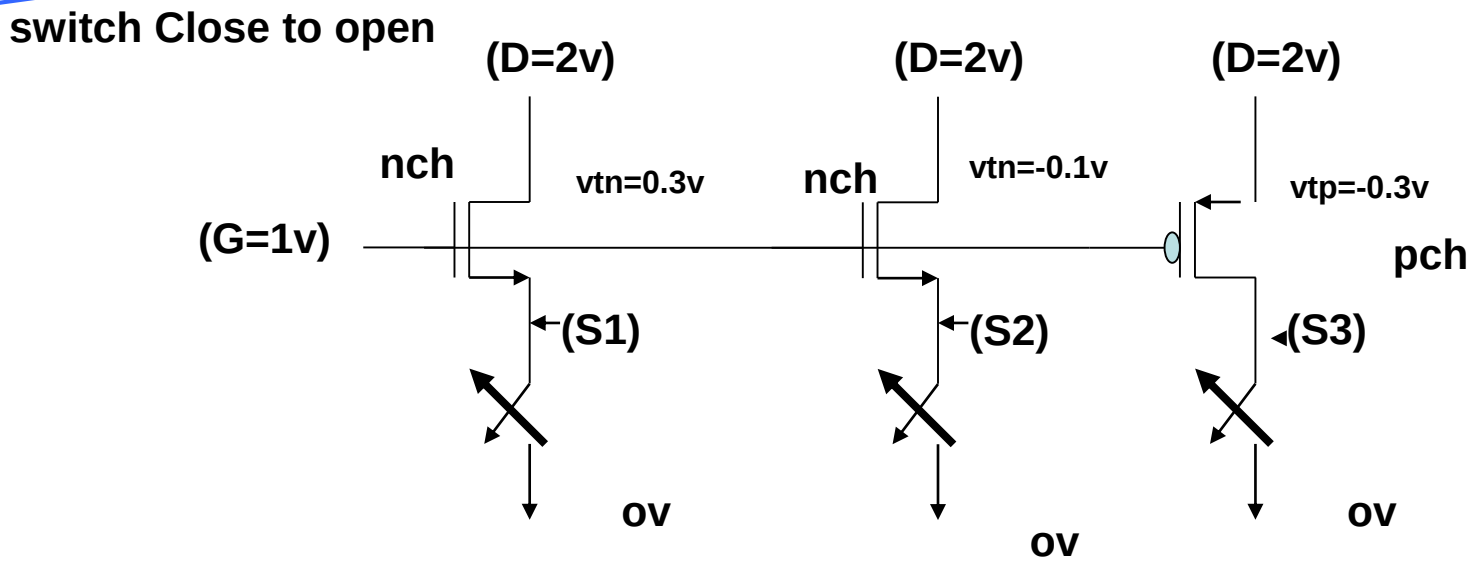
Assignment 1 - optional



1. What is w/l of a donut shape transistor ?
2. Can you derive it ?
3. What is it good for ?

Assignment 2

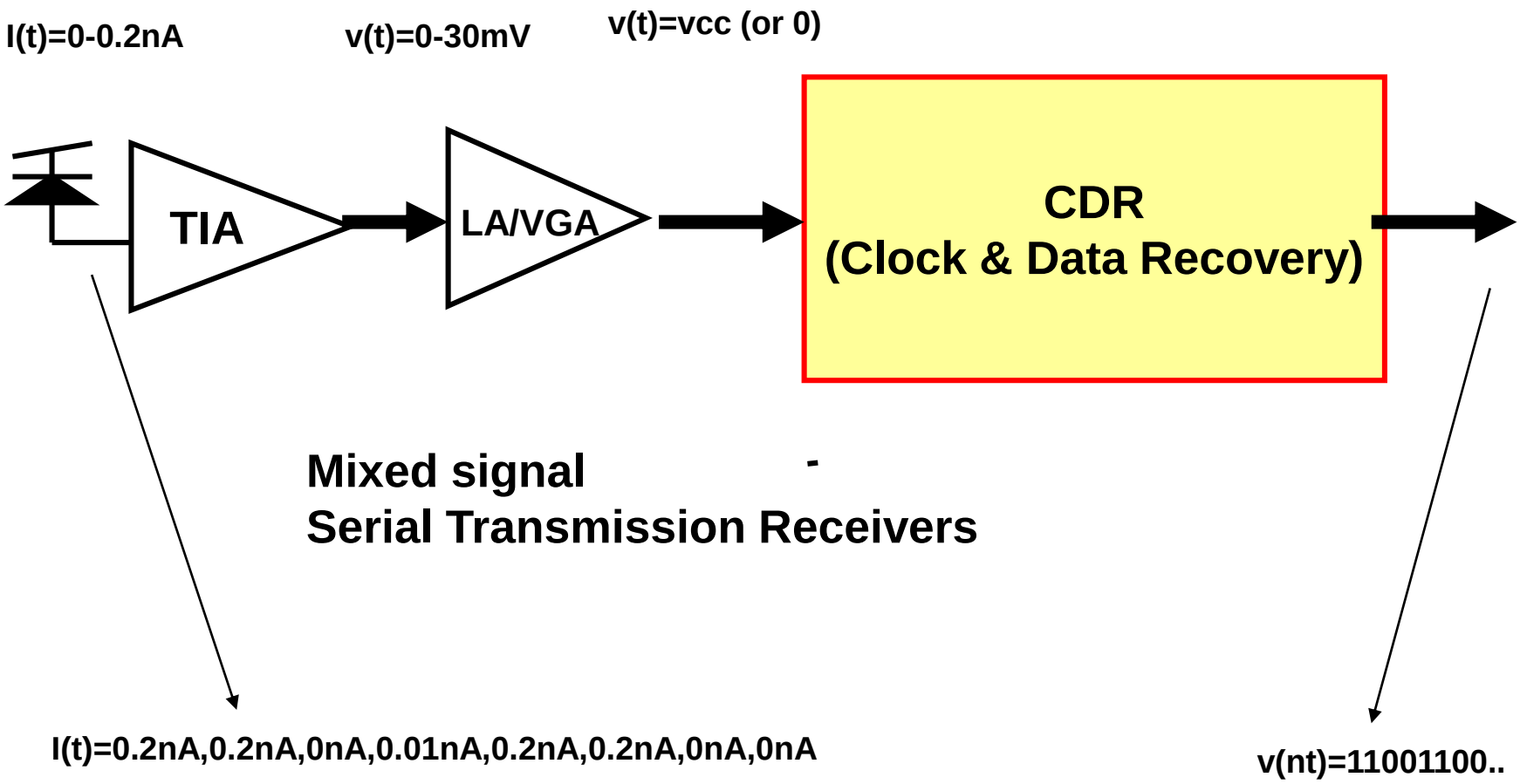
4. If at t=0 the switch is closed then at t=1ns it open what is the final voltage at the three sources (S1,2,3) ?



END lect. 01

added slides for lect. 01

Example of Mixed Signal systems



Example: ADC / DAC LOCATION IN WiFI system…