ENOB calculation for ADC's

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For:
0510772001 2nd semester 09
Advanced Topics in Analog and Mixed Signal Design

General:
In this document a general method for ENOB calculation will be presented. This calculation can be done with MATLAB or with a post processing viewer such as CADENCES WAVESCAN running on the spice simulation results. In CADENCE VIRTUOSO simple SKILL programs can be written to do the entire post processing.

Theory:
In order to calculate the ENOB of an ADC the next steps will be used.

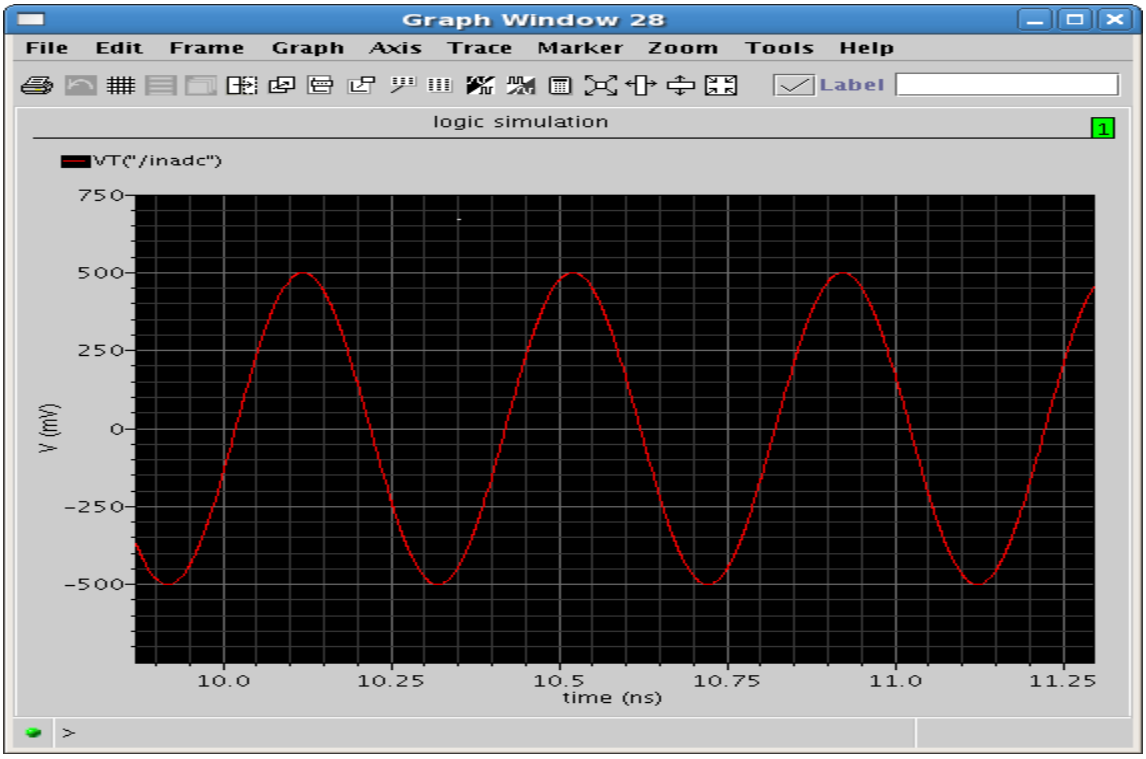
1) Input the ADC with a perfect sinus signal. In order to use the FFT method of generating a DFT transformation the length of the sampled output file should be 2^N samples. It is recommend to use at least N=number of ADC conversion bits + 2 for a total of 4 samples per code. If using a SPICE program a simple method to generate these samples is to feed the digital output to an ideal DAC. The resulting signal should be sampled just before the next step occurs. Using MATLAB program a direct mapping between the digital state and an analog number can be used.
2) In order to generate a perfect DFT result, the inputted signal should be a perfect cyclic sinus otherwise the cyclic extension of this signal will not be a sinus and a wrong measurement will result. In order to generate a perfect cyclic input signal the input signal frequency should be a natural number division of the sample rate used. In order to estimate the entire code set of the ADC a natural prime number should be used. Hence for example if N=11 for a total of 2048 samples Fin=Fsample*D/2048. For this example the next D's can be used in order to evaluate the entire spectrum: 31,63,127,255,511,757,1023. It is recommended to use at least 6 frequencies to obtain a correct frequency dependence function of the ENOB.
3) Make sure the collected data does not contain transient effects and that the ADC is in its optimal work mode. Once all the analog level samples are generated a DFT transform should be done. In this DFT each result will account for 1/(2^N) of the spectrum. Make sure the spectrum expands from zero to Nyquist freq of the ADC. If the DFT results with the full spectrum truncate the second half of the mirrored spectrum. Using Parsaval's theorem we can state that the Voltage RMS of the incoming signal is Vin(RMS)=sqrt(integral(0.5*(|F|^2)(1:(2^N)))). Noticing that the entire power of the incoming signal is contained in one frequency domain bin

we can write: SNR=SigPwr/NoisePwr=(0.5*|F(Z)|^2)/(0.5*(|F|^2)(1:Z-1)(Z+1:(2^N)). Where Z is the bin containing the power of the inputted signal.

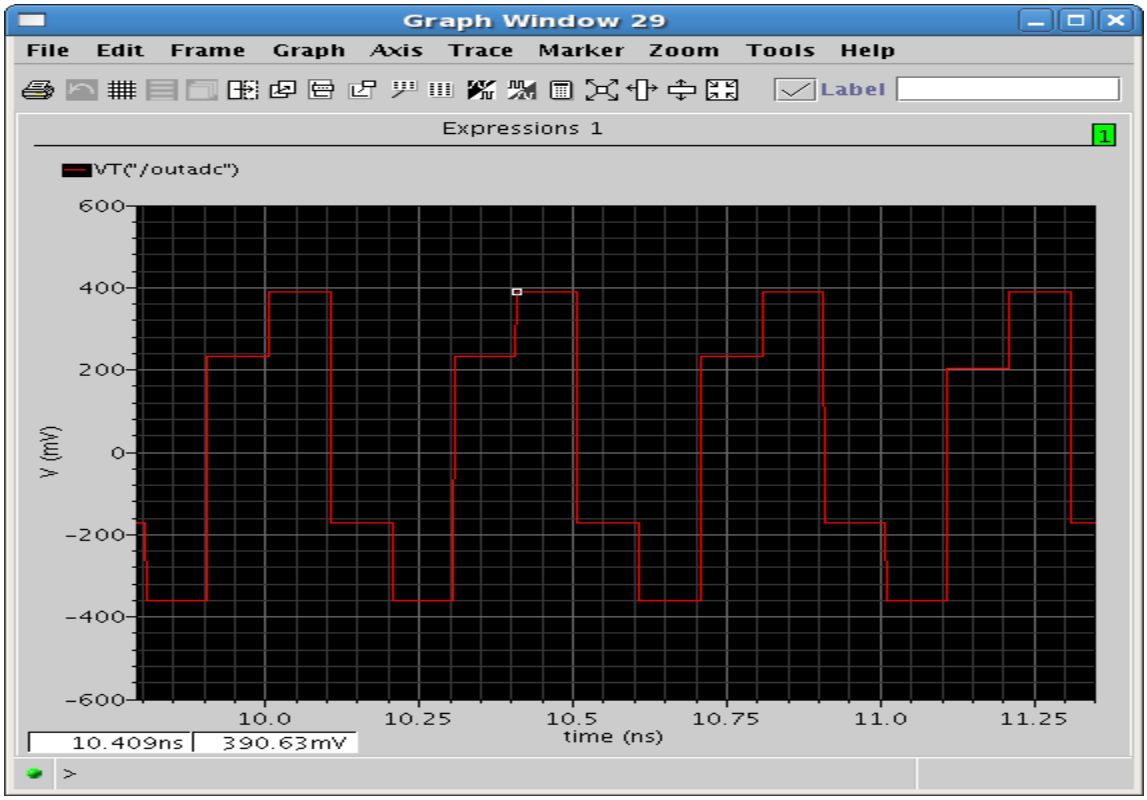
4) Using the ENOB formula we get: ENOB=(10*log10(SNR)-1.76)/6.02

Example:

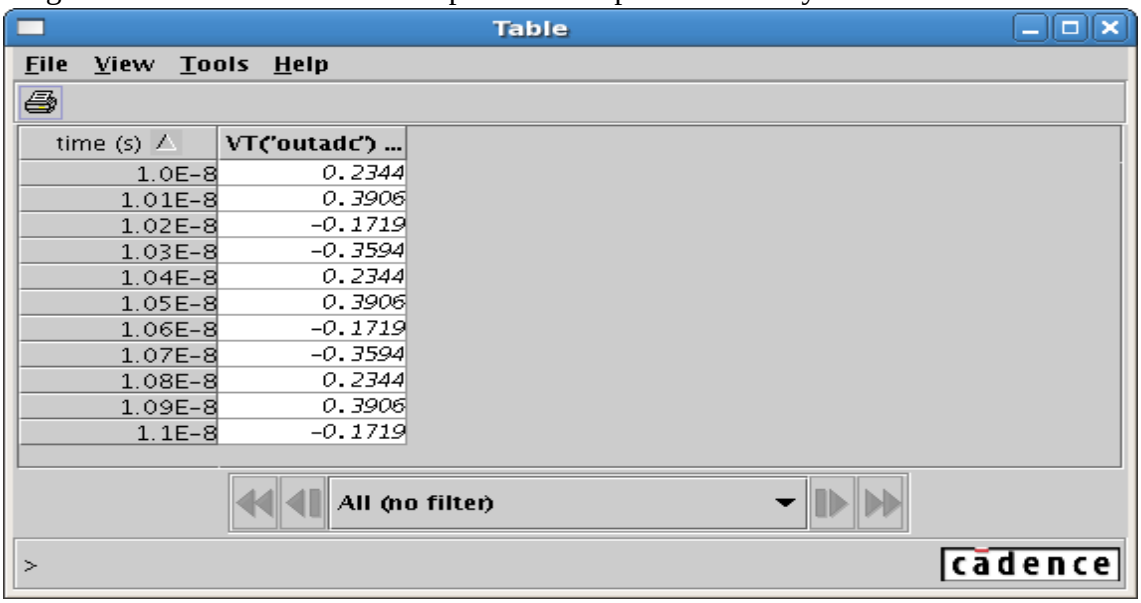
10GbS sampling rate of a 4Bit ADC:
Choosing N=11 for ample samples per code and simulating with D=511 results in the next input sinus:
freq=511/2048*10Gbs=2.495Ghz



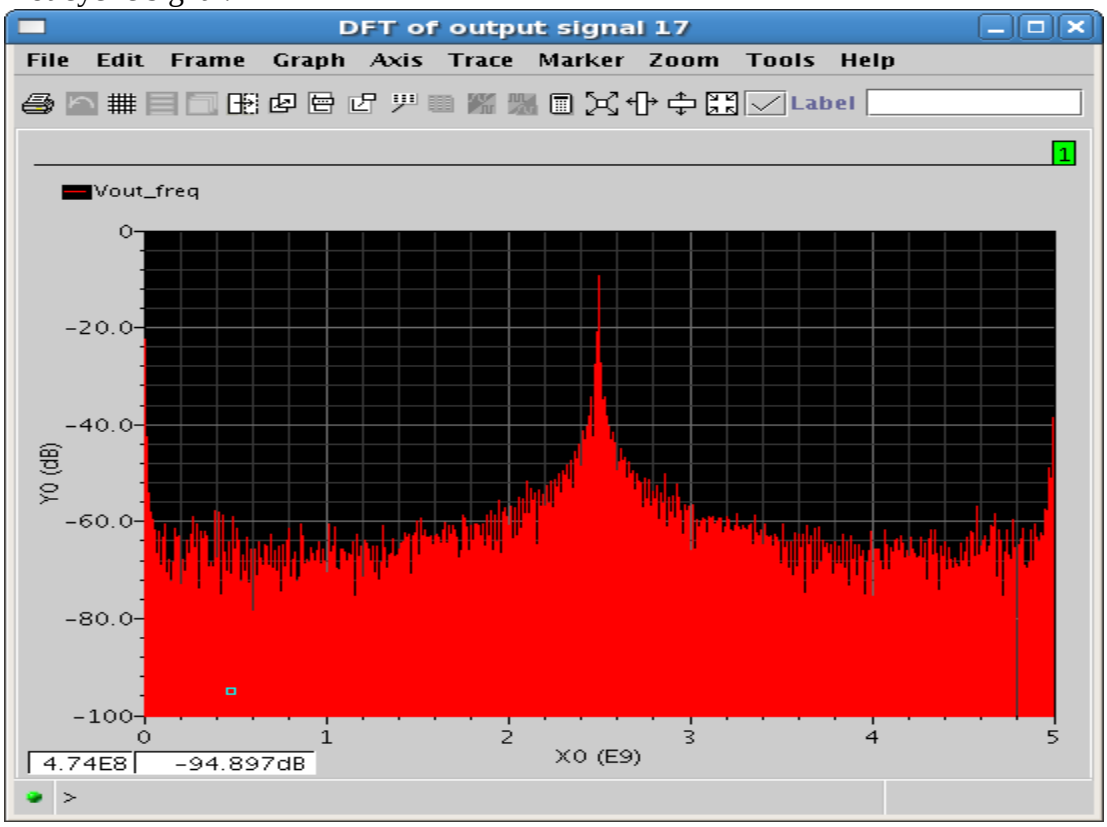
Using an ideal DAC to reconstruct the signal



Sampled signal: using the WAVESCAN calculator a tabular representation of the signal is extracted. If post processing is to be continued with DFT function of WAVESCAN this is not needed as the DFT function samples the signal. Note the sample points where chosen just before the transient occurs. When using SPECTRE use of the strobe option can help with accuracy of results.



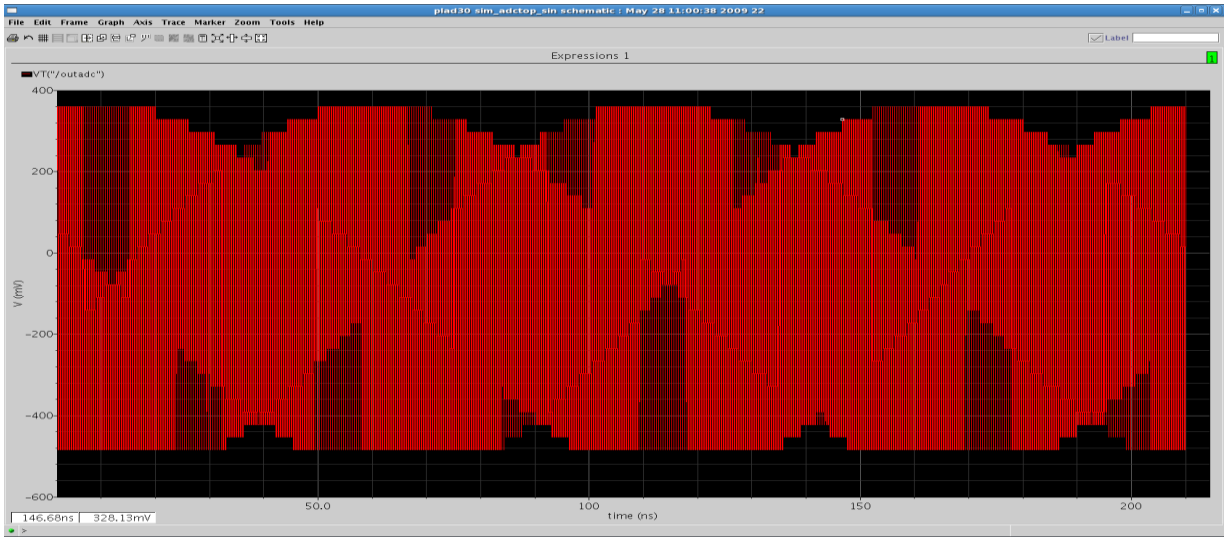
DFT of a not cyclic signal:



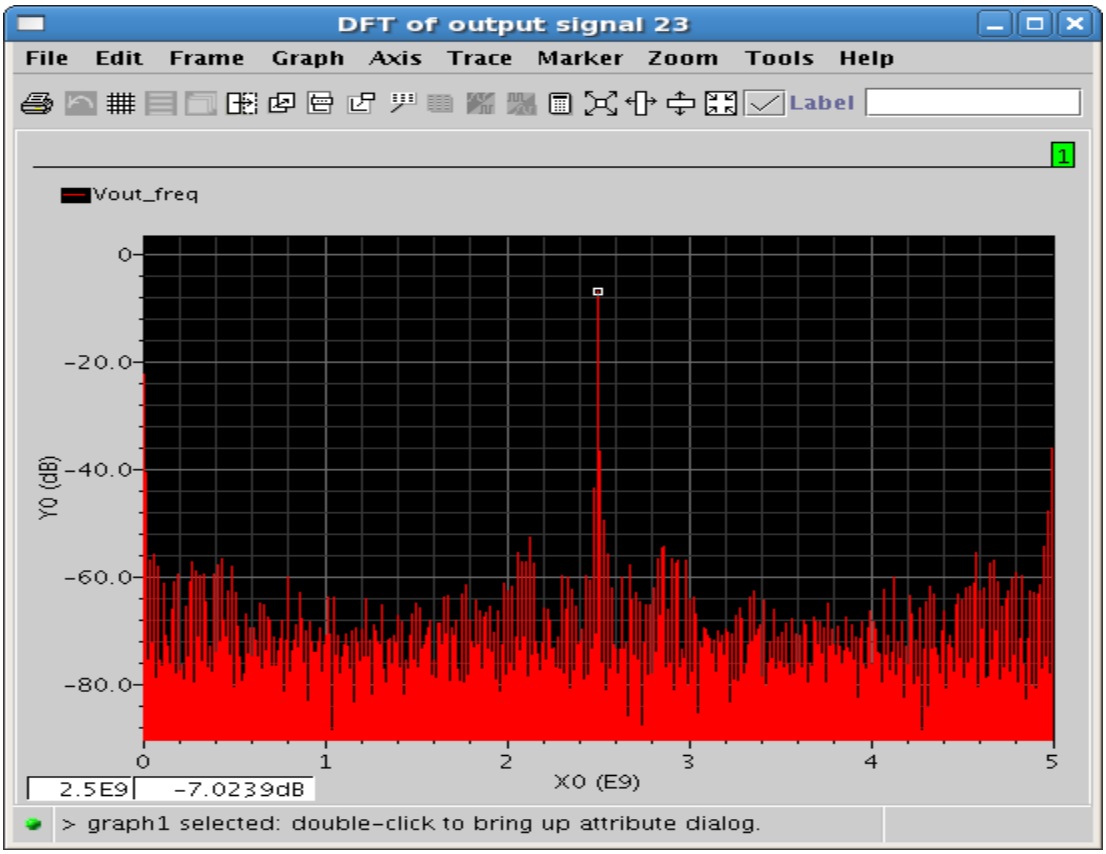
Above is a DFT graphical representation of an acyclic signal. Due to this the signal energy is spaced over multiple bins suggesting an un pure sinus signal. If this happens check the simulation/DFT

conditions to make sure you get a pure single tone.

A graphical representation of a signal generated with 2048 clock cycles. These samples are represented as a stair graph. Note the beating effect of the signal; this is due to the pass of the sampled signal over all the codes of the ADC. As a result full performance of the ADC is evaluated.



DFT of a correct cyclic signal:
After correctly sampling the signal and correctly applying the DFT the next transform is achieved.



The very low noise is due to quantization noise with small disturbances which are the result of a not ideal comparator used for this simulation. In the case of an ideal comparator the noise floor would be

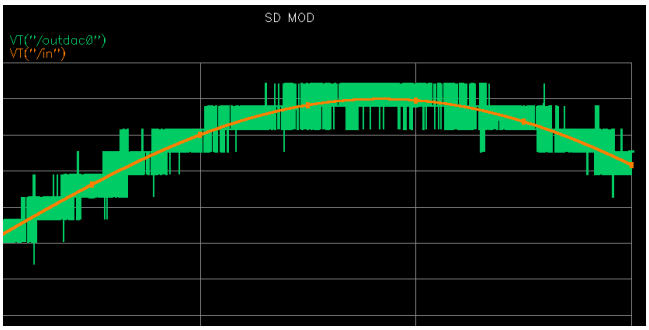
completely even. Using Parsavals theorem in order to calculate the SNR and then the ENOB results in:

SNR of this signal: 24dB

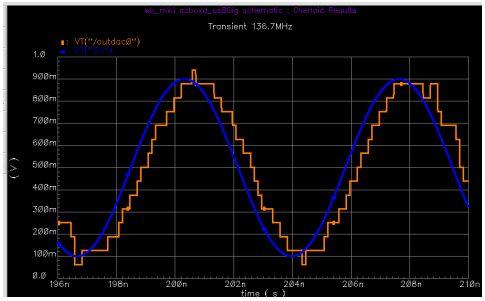
ENOB of this signal: 3.71780 bits.

These results are very good for such an ADC. (Ideal clock with no jitter etc….)

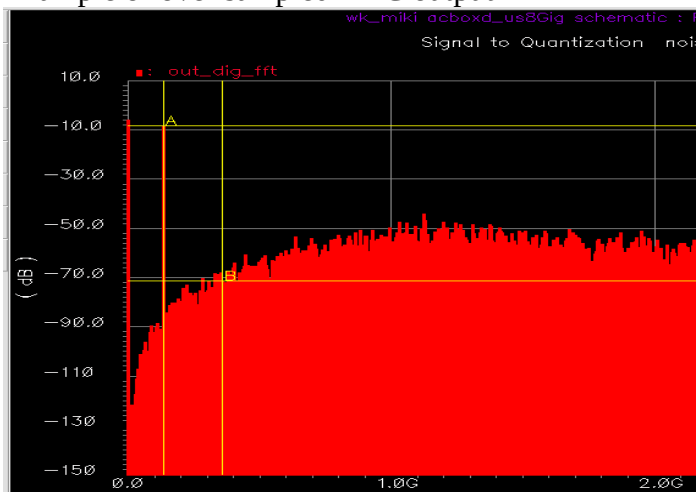
Sigma Delta ADC example:



Example of over sampled ADC output



Example of Low OSR SD. ADC



FFT of Low OSR SD ADC- Noise overshaping